ALCT Spartan-6 Mezzanines

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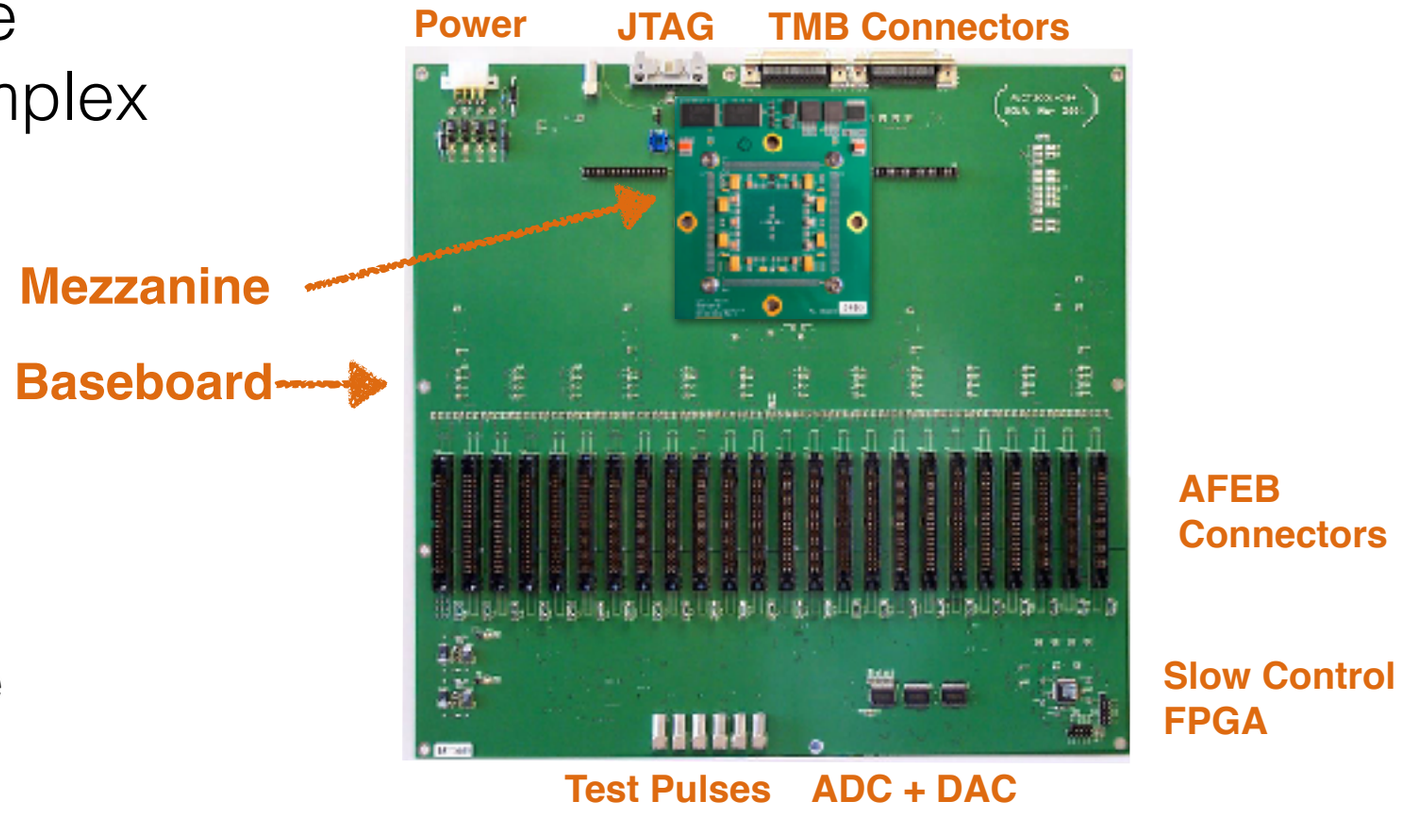
9 April 2018

ALCT Upgrade

ALCT logic implemented in plug-in FPGA mezzanine card

- Allows upgrade of programmable electronics without replacing complex and expensive baseboard



Upgrade Motivations:

- Latency: the current FPGAs cannot handle Phase-2 trigger latency of up to 12.5 us
  - Not enough block RAM in Virtex-E FPGAs (circa 2000)
  - Solution is to replace with more modern Spartan-6 FPGAs on all CSC stations
    - ✦ Spartan-6 is radiation tested; reliability proven already in ME1/1, ME4/2. Zero failures in Run II
- Bandwidth: in the stations with highest rates, copper cables cannot carry data to DMB fast enough
  - Two new mezzanines increase bandwidth from 0.64 Gb/s (on copper) to about 4.5 Gb/s (on fiber)

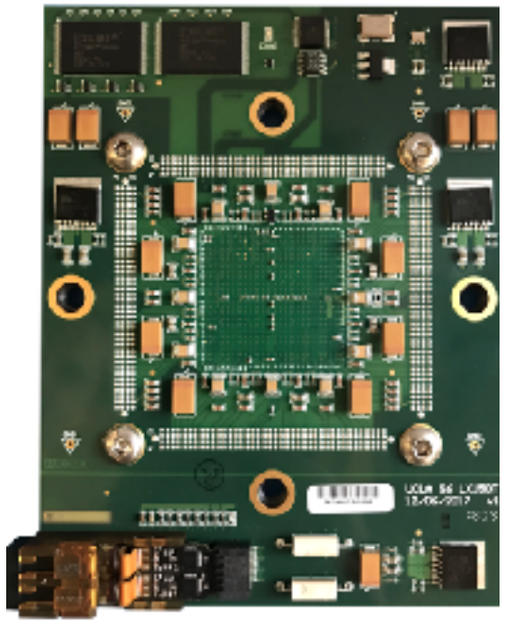
ALCT Mezzanine Upgrade

Two new designs for LS2 installation:

LX150T

- LX150T boards have larger FPGA for large ALCT 672 boards (ME234/1)
  - Requires more IO pins + logic and ALCT 288 and 384 boards
- Two transmitters running at 3.2 Gbps each provide optical DAQ link
  - Utilizes CERN radiation-hard VTTX twin-transmitter
  - 8b10b encoding, 80 MHz commercial reference clock

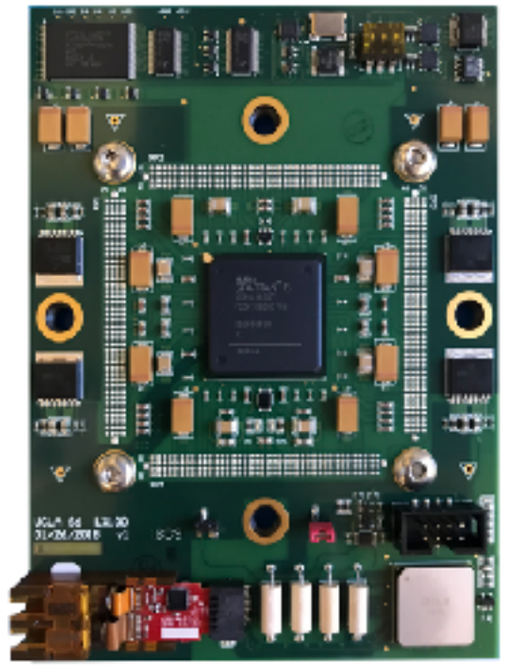
LX150T



LX100

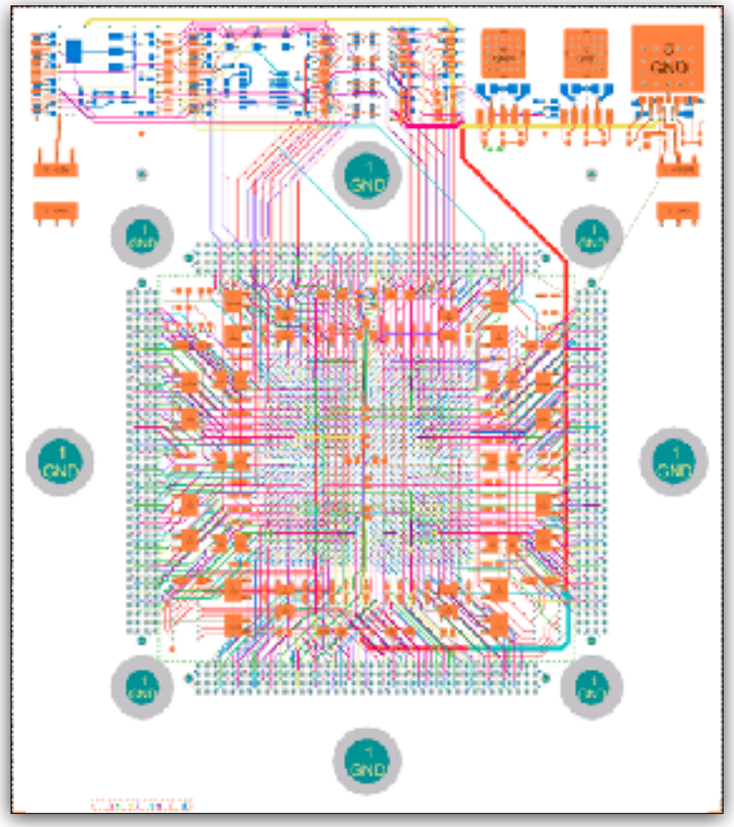
- LX100 boards have a smaller FPGA and reduced pinout
  - Drops compatibility with ALCT672 boards to reduce cost and complexity
- GBTx chip provides EEPROM-less programming and optical DAQ link
  - 4.8 Gpbs link, with 4.48 Gbps of user bandwidth
    - (after overhead, w/ optional wide-frame mode)
  - Utilizes CERN radiation hard VTRX transmitter/receiver
  - Plug-in optics will remain unstuffed in non-ME1/1 stations

LX100



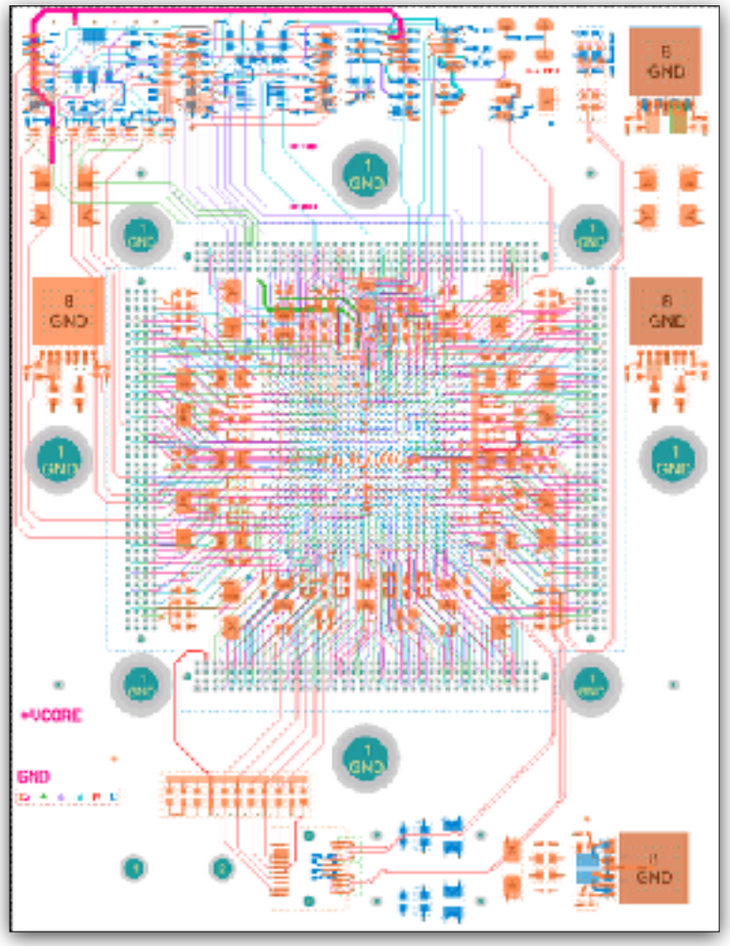
ALCT Spartan-6 Family

(images to scale)



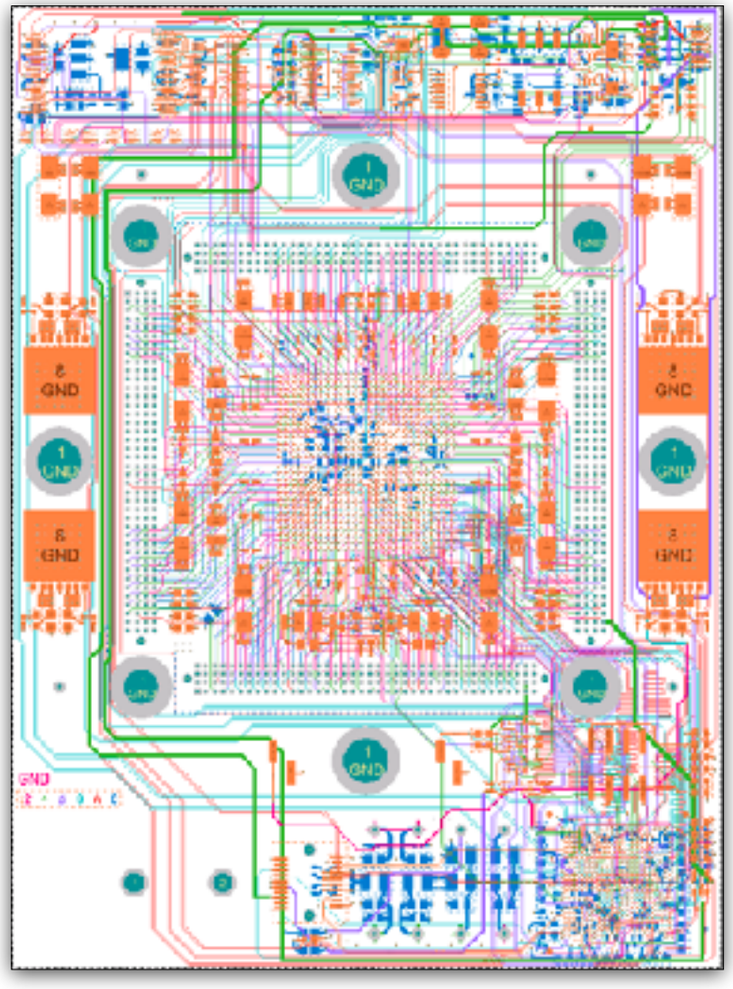
S6-LX150

- 144 cards + spares
- Supports all ALCT types + TMB
- Existing 2011 design
  Currently on ME1/1, ME4/2
- ME4/2, ME1/3



S6-LX150T

- 108 cards + spares
- Supports all ALCT types
- 5.12 Gbps optical user bandwidth
- ME2/1, 3/1, 4/1



S6-LX100

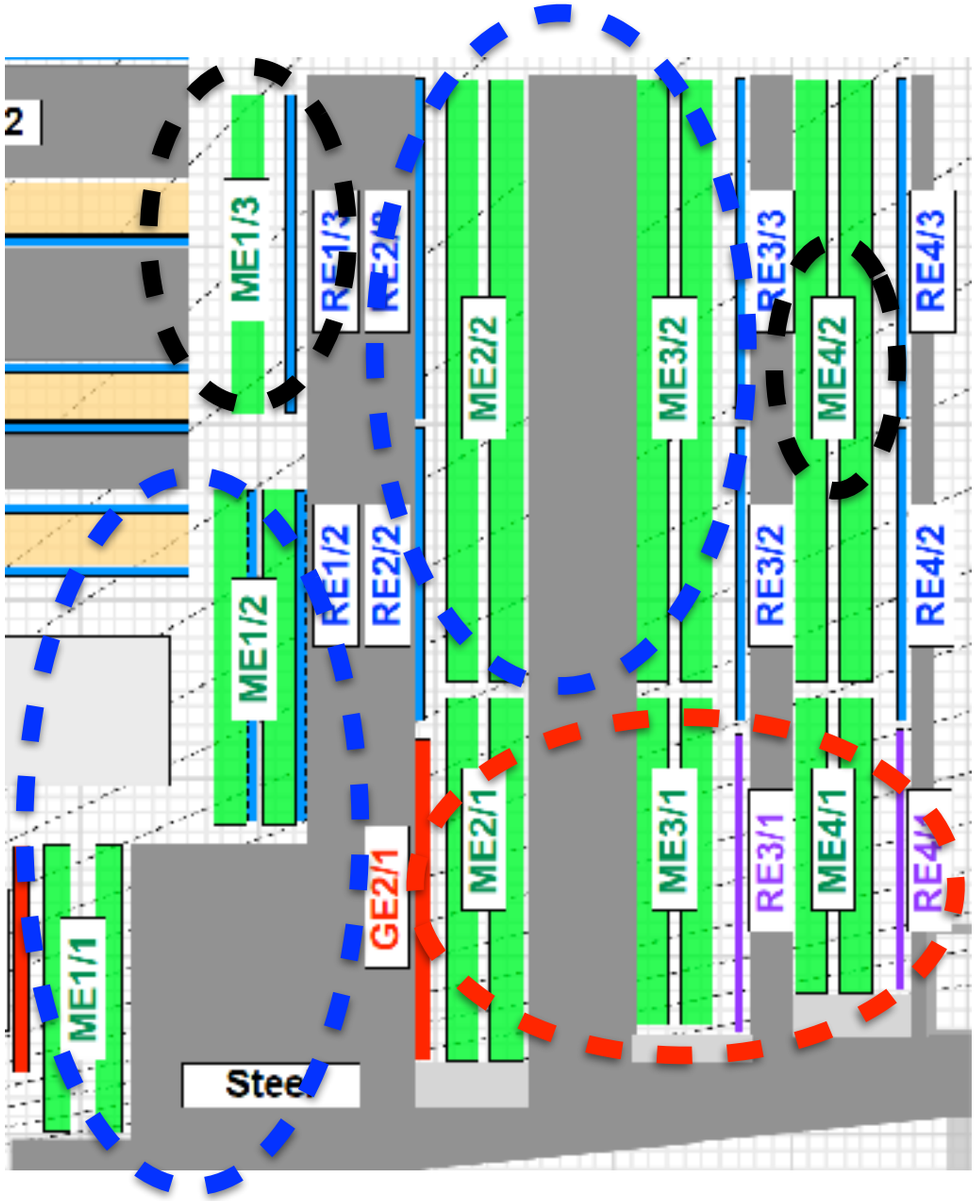
- 288 cards + spares
- Supports ALCT288 + 384
- 4.48 Gbps optical user bandwidth
- PROMless Programming (GBTx)
- ME1/1, 1/2, 2/2, 3/2

ALCT Usage

- **LX150** boards retained (ME4/2) or moved from ME1/1 to low-rate location (ME1/3)
  - 72 cards in ME4/2
  - 72 cards in ME1/3

- **LX150T** boards have larger FPGA for large ALCT672 base boards used in ME2/1, 3/1, 4/1 and twin optical links for DAQ
  - 108 cards in ME234/1

- **LX100** boards have GBTX capability to support PROM-less programming and optical links
  - 72 cards in ME1/1 (w/ optics)
  - 216 cards in ME1/2, 2/2, 3/2 (w/o optics)



ALCT Mezzanine Timeline

Month	LX150T	LX100
08/2017	**start project**	**start project**
02/2018	**fabricate boards**	**fabricate boards**
03/2018	**test boards**	**test boards**
04/2018	get bids on parts	
05/2018	ESR	ESR
06/2018	pre-series production	
07/2018	production & testing	
08/2018	production & testing	
09/2018	production & testing	
10/2018	production & testing	
11/2018	production & testing	
12/2018	production & testing	get bids on parts
01/2019	finish shipping	ready for production
02/2019		pre-series production
03/2019		testing
04/2019		production & testing
05/2019		production & testing
06/2019		production & testing
07/2019		production & testing
08/2019		finish shipping

- Current production and testing is on track for meeting goals
- Biggest uncertainty and probable source of delays is funding availability
- This month:
  - Thorough testing of boards in prep for ESR. Date?
  - Collect quotes

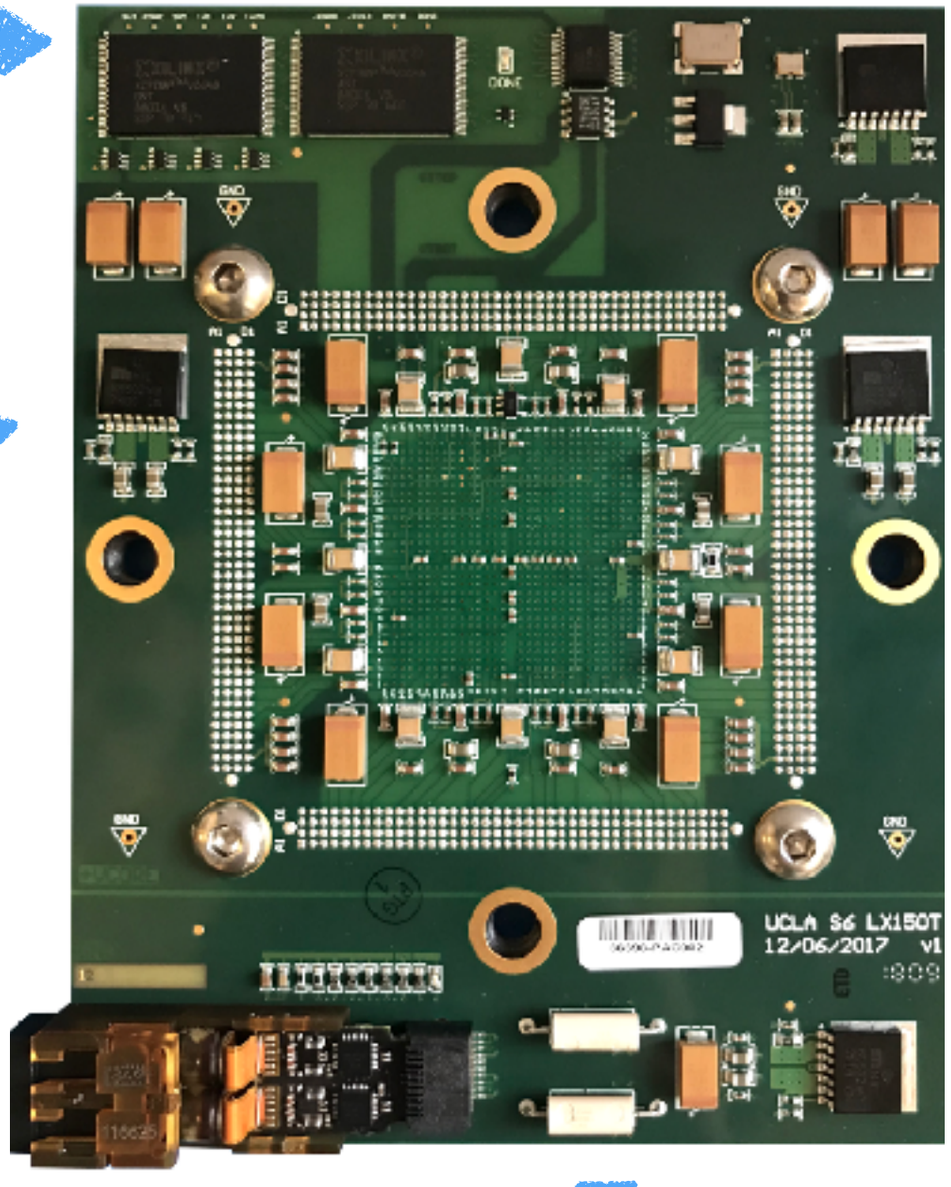
Possibility of sooner ME1/1 LX100 if funding is available

LX150T Mezzanine

ADC

Oscillators

XCF08P + XCF32P
EEPROMs



Voltage
Regulator
(MIC69502WR)

Voltage
Regulators
(MIC69502WR)

CERN VTTX

VTTX Power Filtering

LX150T Test Summary

LX150T Mezzanines received on 6 April 2018

- alct_sctest (single cable loopback) Software / firmware updated
  - ✦All tests passed, no issues
- alct672 (cms) firmware updated for Spartan-6 and w/ new pinouts
  - ✦Tx/Rx scan tentatively good.. still investigating some peculiarities
- Optical link tests are in progress…
  - ✦Link established.. transmits mostly ok… but there seems to be a bug in channel bonding firmware (on my hacked up ODMB firmware)
    - Not a big surprise
    - Will debug when I get back
- Cosmics test at B904 ME2/1 test stand
  - ✦ Will need help

LX150T Test Results

	Card #1	Card #2	Card #3
Voltages Check	**PASS**	**PASS**	**PASS**
JTAG Program FPGA	**PASS**	**PASS**	**PASS**
EEPROM Program FPGA	**PASS**	**PASS**	**PASS**
Mezzanine ADC Voltage Self Check	**PASS**	**PASS**	**PASS**
Single Cable Loopback	**PASS**	**PASS**	**PASS**
Delay Chip r/w	**PASS**	**PASS**	**PASS**
TMB Tx/Rx Scan	**PASS**	**PASS**	**PASS**
ODMB PRBS Test	**work-in-progress**	**work-in-progress**	**work-in-progress**
Cosmics test @ 904	**work-in-progress**	**work-in-progress**	**work-in-progress**

+1.8V current = 0.2A
+3.3V current = 2.9A

LX150T ALCT672 TMB tx/rx scan

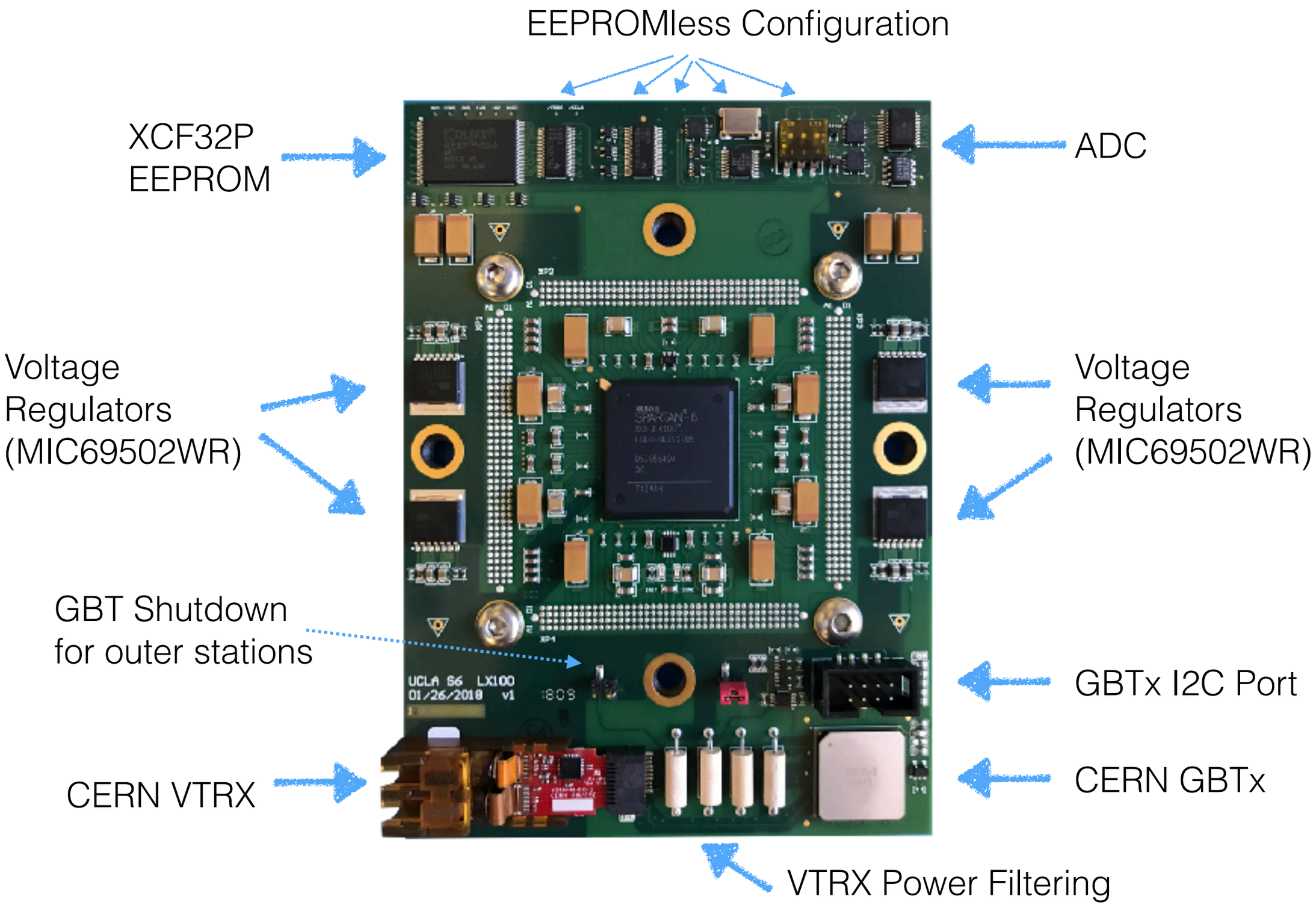
- With regular IO settings (copied from ALCT 384 boards)
  - Very narrow window on TX scan. Uh oh… but changing the pin drive settings fixes it
  - Should experiment w/ other combinations of settings to optimize window
    - Should check on other boards (a288, a384) as well

12mA SLOW → 4mA FAST

```
 0     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 1     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 2     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 3     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 4     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 5     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 6     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 7     19507 19.5070 FF |xxxxxxxxxxxxxxxxxx
 8     10182 10.1820 FF |xxxxxxxxxx
 9     10000 10.0000 FF |xxxxxxxxxx
10         0  0.0000 PP |
11         0  0.0000 PP |
12         0  0.0000 PP |
13         0  0.0000 PP |
14         0  0.0000 PP |
15      1000  1.0000 PF |x
16      1000  1.0000 PF |x
17      2000  2.0000 FF |xx
18      3446  3.4460 FF |xxx
19      6000  6.0000 FF |xxxxxx
20     15305 15.3050 FF |xxxxxxxxxxxxxx
21     18024 18.0240 FF |xxxxxxxxxxxxxxxxx
22     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
23     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
24     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
25     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
```

```
 0     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 1     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 2     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 3     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 4     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 5     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 6     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 7     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 8     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
 9     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
10     16876 16.8760 FF |xxxxxxxxxxxxxxx
11         0  0.0000 PP |
12         0  0.0000 PP |
13         0  0.0000 PP |
14         0  0.0000 PP |
15         0  0.0000 PP |
16         0  0.0000 PP |
17         0  0.0000 PP |
18         0  0.0000 PP |
19         0  0.0000 PP |
20         0  0.0000 PP |
21         0  0.0000 PP |
22     10000 10.0000 FF |xxxxxxxxxx
23     18003 18.0030 FF |xxxxxxxxxxxxxxxxx
24     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
25     20000 20.0000 FF |xxxxxxxxxxxxxxxxxxx
```

LX100 Mezzanine



LX100 Test Summary

LX100 Mezzanines received on 26 March 2018

- alct_sctest (loopback) Software / firmware updated
  - ✦All tests passed, no issues
- alct384 (cms) firmware updated w/ new pinouts
  - ✦TMB tx/rx communications tests passed, no issues
- PROMless Programming
  - ✦Basic functionality established
  - ✦Working with Evaldas on programming
- E-links (DAQ data out)
  - ✦Not yet tested
  - ✦Hardware bug identified :(
- Cosmics test at B904 ME2/1 test stand
  - ✦ Will need help

LX100 Test Results

	Card #1	Card #2	Card #3
Supply Voltages Check	**PASS**	**PASS**	**PASS**
JTAG Program FPGA	**PASS**	**PASS**	**PASS**
EEPROM Program FPGA	**PASS**	**PASS**	**PASS**
Mezzanine Voltage Self Check	**PASS**	**PASS**	**PASS**
Single Cable Loopback	**PASS**	**PASS**	**PASS**
Delay Chip r/w	**PASS**	**PASS**	**PASS**
TMB Tx/Rx Scan	**PASS**	**PASS**	**PASS**
CTP7 IBERT	**PASS**	**PASS**	**PASS**
EEPROMless Programming	**work-in-progress**	**work-in-progress**	**work-in-progress**
FPGA Elinks Test	**work-in-progress**	**work-in-progress**	**work-in-progress**
Cosmics test @ 904	**work-in-progress**	**work-in-progress**	**work-in-progress**

w/ CMS firmware, configured GBTx
output elinks not running in firmware

+1.8V current = 0.1A
+3.3V current = 2.6A

GBTx → FPGA

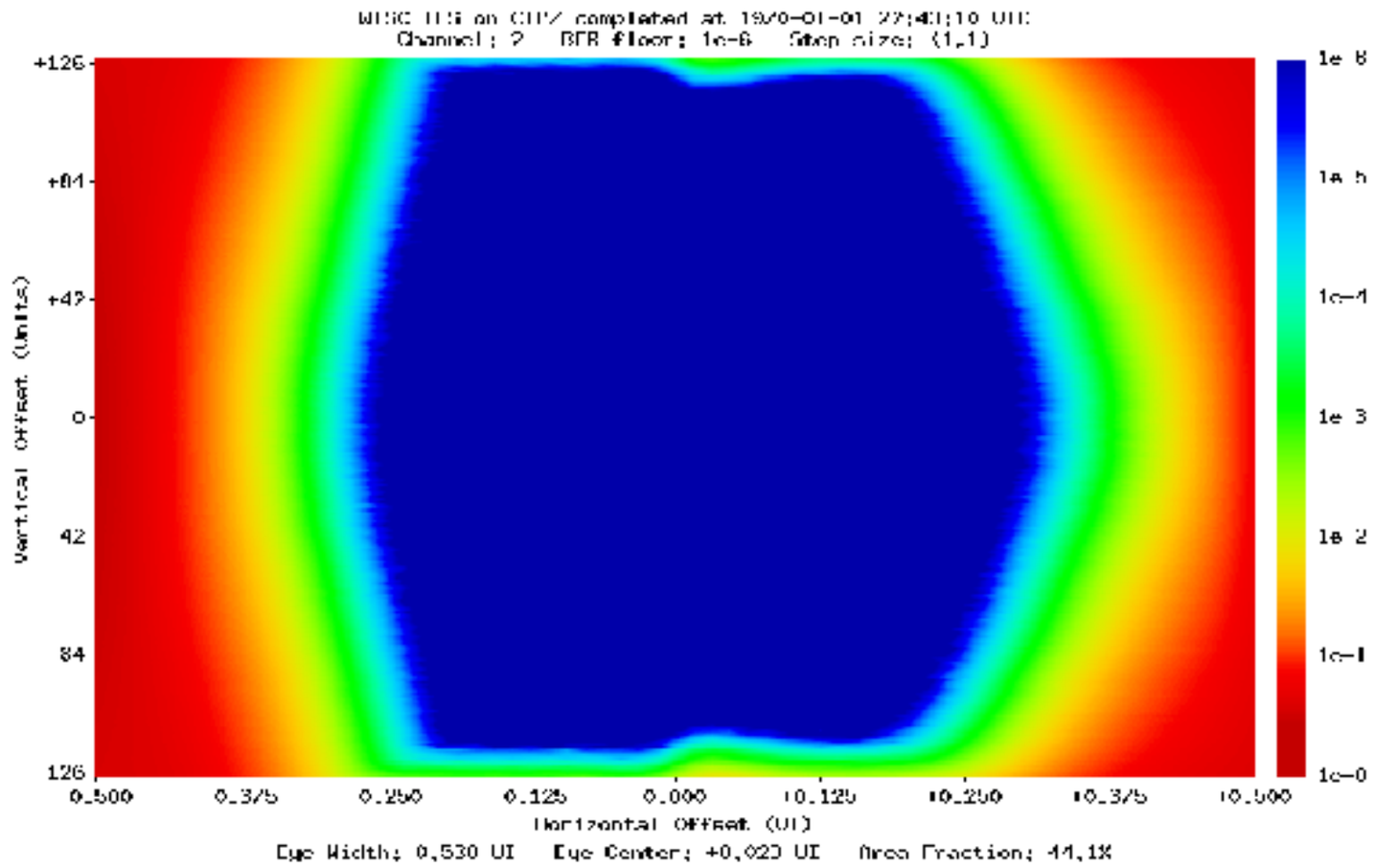
- Backend → GBT path has been tested for basic functionality
  - No errors on link
  - Can toggle PROMless programming and control bits
  - Discovered very minor bug in hardware for PROMless control
    - ✦BOM had the wrong variant of a part (Identical pinout— just needed to change the part)
    - ✦Had to change a connection (Soldered a wire… *very* easy to fix on final design)

- Working with Evaldas on getting PROMless programming working
  - "Virtual input/output" gives manual control over PROMless programming bits
    - ✦ All work as expected after fixes above
  - Everything seems to work on the hardware.. but the FPGA fails to configure… CRC errors
    - ✦ Limited time to debug so far. Will work on it next week.. (hook up logic analyzer?)

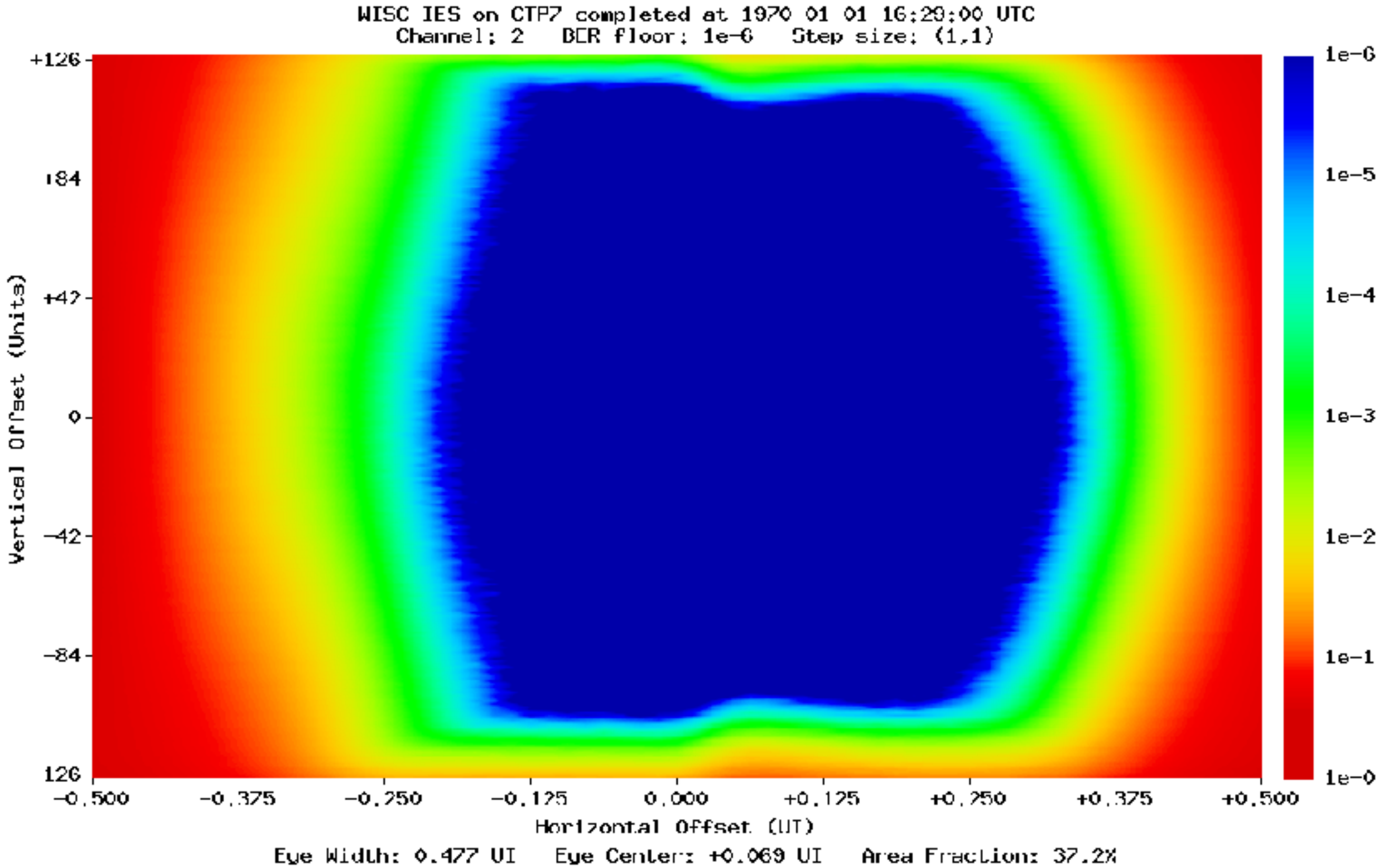
FPGA → GBTx

- Have not yet tested FPGA → GBTx → Backend path
  - But it has Wide open IBERT “eyes” (good link quality)
  - Need to finish firmware
  - But there is an issue with e-link assignments on FPGA
    - ✦(details in subsequent slide)

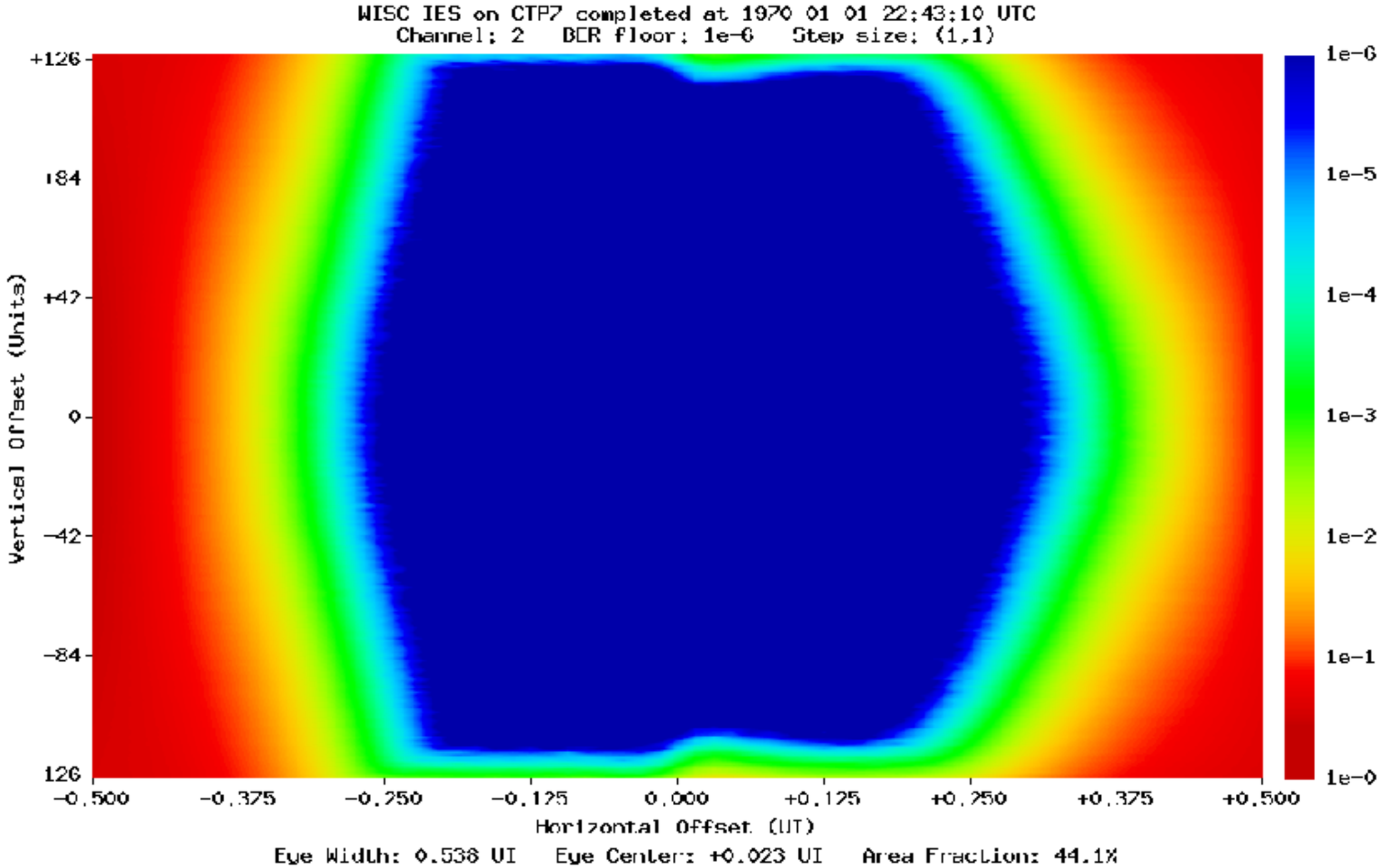
Example
IBERT Eye



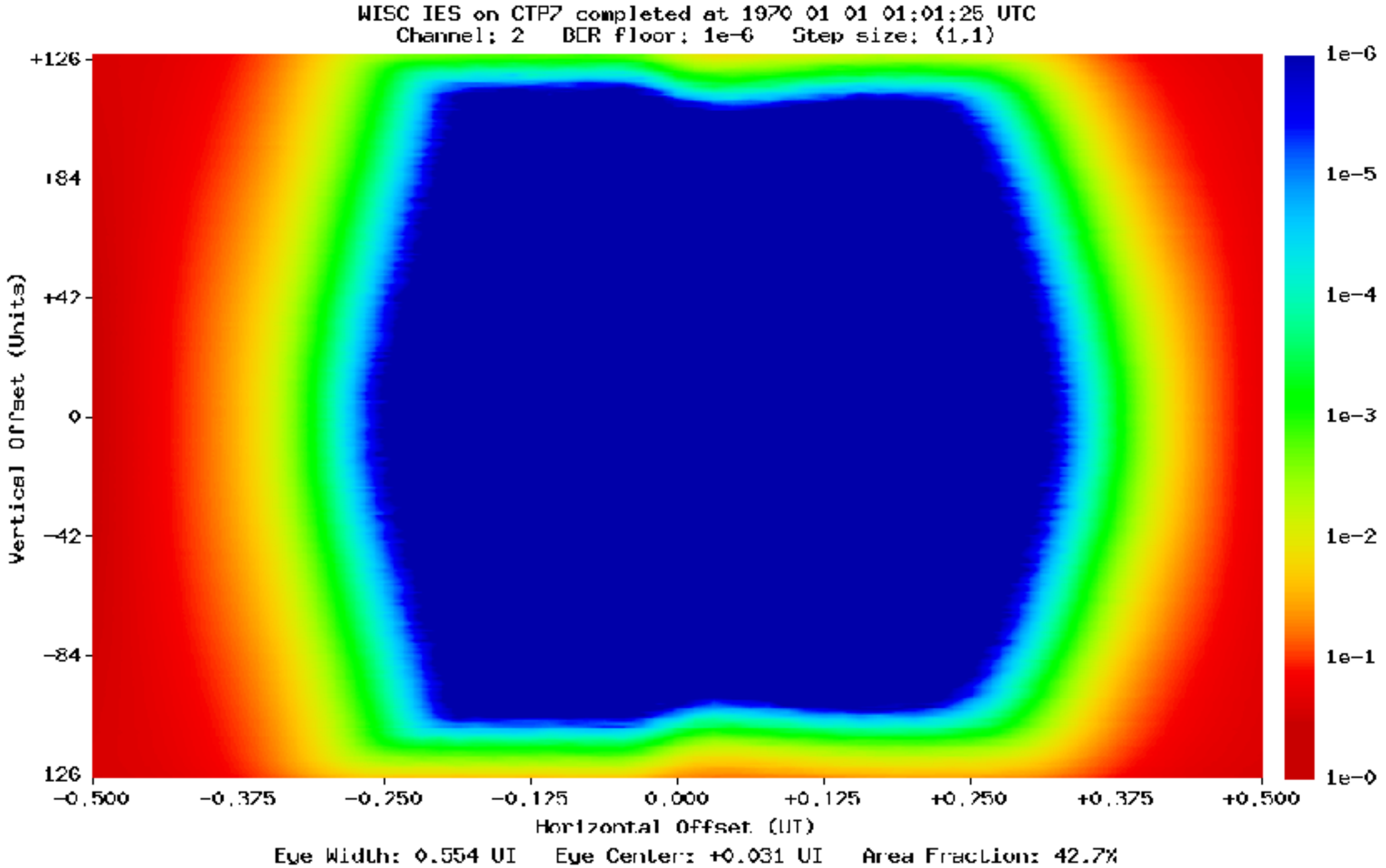
IBERT Mezz #10001



IBERT Mezz #10002



IBERT Mezz #10003



LX100 E-Links & IO Standards

- Big oversight in LVDS pin assignments :(
  - **Not all pairs are bi-directional**

LVDS_33—Low Voltage Differential Signal

LVDS_33 is used to drive TIA/EIA644 LVDS levels in a bank powered with 3.3V V_{CCO}. Electrically the same as LVDS_25. LVDS inputs require a parallel termination resistor, either through the use of a discrete resistor on the PCB, or the use of the DIFF_TERM attribute to enable internal termination. LVDS inputs can be placed on any I/O bank, while LVDS outputs are only available on I/O banks 0 and 2.

  - Most e-links not usable as outputs in current design
    - Only get 960 Mb/s of uplink bandwidth :(
  - Can still validate remainder of design and test optical link w/ partial bandwidth
    - **Or test all e-links in the opposite direction (use as INPUTS)**
  - Next design needs minor pin swapping to rearrange e-links
    - Finished updates already for next design…

  - **Go to ESR with this (well understood) issue? or is a new prototype needed before then?**

GBTx in DAQ

- GBTx data is scrambled during transmission
  - Processing in the FPGA first requires unscrambling in logic with the GBT-FPGA core

- Where will GBTx data get unscrambled? ODMB or FED?
  - If unpacked in ODMB:
    - ✦ Simple… use GBT-FPGA, process resulting datastream as usual, send on to FED
    - ✦ GBT-FPGA core will reside in ODMB← subject to SEU
    - ✦ Artix-7 does not and will not have a GBT-FPGA core. Need to adapt it ourselves
  - If unpacked in FED:
    - ✦ ODMB needs to still be aware of the ALCT datastream
      - (to know when to include in the packet to FED)
    - ✦ Could use a copper DAV bit in parallel with the optics for sync

- Unpacking in ODMB seems simpler, ok if:
  - SEU concerns are minor enough, and logic fits okay in the new ODMB FPGA, and we can successfully port the GBT-FPGA firmware

Next Steps

LX100

- Get PROMless programming working
- Test optical link (operate as prbs-rx?)
- Correct PCB and BOM issues
- GBTx auto-shutdown should be adapted from DCFEB
- Generate new design (ok for ESR with existing design?)
  - Changes are minor and straightforward

LX150T

- Test optical link
- Experiment with IO drive strength settings
- Get quotes and start production

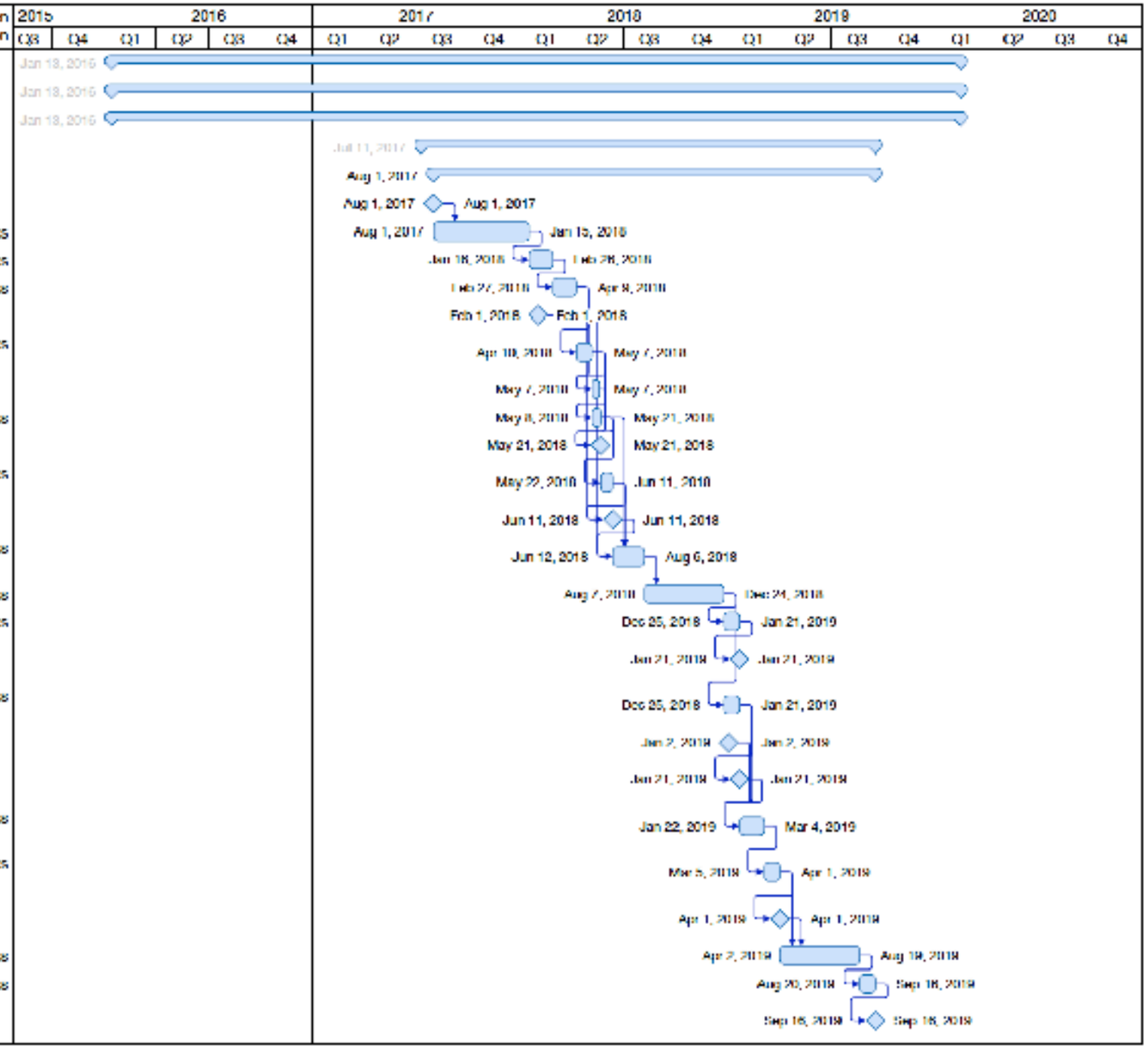
Both Cards

- Finish updates and refinements to automatic test software @ UCLA
- Test @ B904
  - w/ copper readout, should be easy
  - need help
- New ALCT firmware with optical links enabled for DAQ
- New ODMB firmware to include Optical ALCT in DAQ
- Write documentation for new boards
- Online software updates

Backup & References

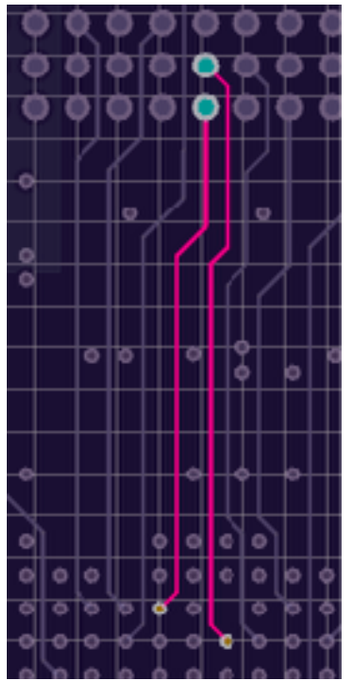
DRAFT Timeline

#	WBS Code	Title	Planned Start	Planned End	Given Duration
0	2.	CMSMuonUpgradeRLS CSC only 19Sep2017	1/13/16	Feb 13, 2020	
1	2.3	CSC electronics for LS2	1/13/16	Feb 13, 2020	
2	2.3.1	On-detector electronics	1/13/16	Feb 13, 2020	
3	2.3.1.1	**Electronics Boards**	Jul 11, 2017	Sep 16, 2019	
23	2.3.1.1.2	**CSC ALCT mezzanine boards**	**Aug 1, 2017**	**Sep 16, 2019**	
24	2.3.1.1.2.1	ALCT start project (LM)	Aug 1, 2017	Aug 1, 2017	
25	2.3.1.1.2.2	ALCT Desgin and Layout	Aug 1, 2017	Jan 15, 2018	24 weeks
26	2.3.1.1.2.3	ALCT Prototype production	Jan 16, 2018	Feb 26, 2018	6 weeks
27	2.3.1.1.2.4	ALCT prototype testing	2/27/18	April 9, 2018	6 weeks
28	2.3.1.1.2.8	Funding in place for ALCT (LM)	Feb 1, 2018	Feb 1, 2018	
29	2.3.1.1.2.6	ALCT obtain bids on parts, PCB, assembly	Apr 10, 2018	May 7, 2018	4 weeks
30	2.3.1.1.2.41	ALCT PRR begins	May 7, 2018	May 7, 2018	
31	2.3.1.1.2.31	ALCT PRR	May 8, 2018	May 21, 2018	2 weeks
32	2.3.1.1.2.7	ALCT ready for ESR	5/21/18	May 21, 2018	
33	2.3.1.1.2.5	Finalize order for ALCT 150T production	5/22/18	Jun 11, 2018	3 weeks
34	2.3.1.1.2.9	ALCT ready for production (LM)	6/11/18	Jun 11, 2018	
35	2.3.1.1.2.10	ALCT-150T pre-series boards produced	6/12/18	Aug 6, 2018	8 weeks
36	2.3.1.1.2.12	ALCT-150T production and testing	Aug 7, 2018	Dec 24, 2018	20 weeks
37	2.3.1.1.2.13	ALCT 150T shipping	12/25/18	Jan 21, 2019	4 weeks
38	2.3.1.1.2.15	ALCT 150T ready for installation in ME234/1 (LM)	Jan 21, 2019	Jan 21, 2019	
39	2.3.1.1.2.21	ALCT-LX100 obtain new bids on parts, PCB, assembly	12/25/18	Jan 21, 2019	4 weeks
40	2.3.1.1.2.35	Funding available for ALCT LX100	Jan 2, 2019	Jan 2, 2019	
41	2.3.1.1.2.23	ALCT-LX100 ready for production (LM)	Jan 21, 2019	Jan 21, 2019	
42	2.3.1.1.2.21	ALCT-LX100 pre-series samples produced	Jan 22, 2019	Mar 4, 2019	6 weeks
43	2.3.1.1.2.25	ALCT LX100 pre series samples tested	Mar 5, 2019	April 1, 2019	4 weeks
44	2.3.1.1.2.40	Full production of ALCT LX100 released	April 1, 2019	April 1, 2019	
45	2.3.1.1.2.26	ALCT-LX100 production and testing	April 2, 2019	Aug 19, 2019	20 weeks
46	2.3.1.1.2.27	ALCT-LX100 shipping	8/20/19	Sep 16, 2019	4 weeks
47	2.3.1.1.2.37	ALCT LX100 ready for installation on ME2/2,3/2	9/16/19	Sep 16, 2019	



ALCT672 TMB tx/rx scan

- Narrow window in tx clock delay scan
  - Most of the issue comes from two neighboring pairs
    - Crosstalk? Traces are very short… crosstalk may be more likely on the baseboard but layout is unknown



Cable Pair Errors vs alct_txd_clock Delay Step

delay	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
pair																										
tx[0]	1000	1000	1000	1000	1000	1000	1000	697	922	1000	0	0	0	0	0	0	0	0	0	0	0	11	1000	1000	1000	1000
tx[1]	1000	1000	1000	1000	1000	1000	1000	653	943	1000	0	0	0	0	0	0	0	0	0	0	0	17	1000	1000	1000	1000
tx[2]	1000	1000	1000	1000	1000	1000	1000	675	924	1000	0	0	0	0	0	0	0	0	0	1000	0	16	1000	1000	1000	1000
tx[3]	1000	1000	1000	1000	1000	1000	1000	664	943	1000	0	0	0	0	0	1000	1000	1000	1000	1000	0	27	1000	1000	1000	1000
tx[4]	1000	1000	1000	1000	1000	1000	1000	668	923	1000	0	0	0	0	0	0	0	1000	1000	1000	0	11	1000	1000	1000	1000
tx[5]	1000	1000	1000	1000	1000	1000	1000	666	943	1000	0	0	0	0	0	0	0	0	0	1000	0	19	1000	1000	1000	1000
tx[6]	1000	1000	1000	1000	1000	1000	1000	683	922	1000	0	0	0	0	0	0	0	0	0	0	0	14	1000	1000	1000	1000
tx[7]	1000	1000	1000	1000	1000	1000	1000	677	943	1000	0	0	0	0	0	0	0	0	446	1000	0	24	1000	1000	1000	1000
tx[8]	1000	1000	1000	1000	1000	1000	1000	676	921	1000	0	0	0	0	0	0	0	0	0	0	0	15	1000	1000	1000	1000
tx[9]	1000	1000	1000	1000	1000	1000	1000	649	943	1000	0	0	0	0	0	0	0	0	1000	1000	0	23	1000	1000	1000	1000
tx[10]	1000	1000	1000	1000	1000	1000	1000	1000	34	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[11]	1000	1000	1000	1000	1000	1000	1000	1000	33	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[12]	1000	1000	1000	1000	1000	1000	1000	1000	35	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[13]	1000	1000	1000	1000	1000	1000	1000	1000	30	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[14]	1000	1000	1000	1000	1000	1000	1000	1000	37	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[15]	1000	1000	1000	1000	1000	1000	1000	1000	26	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[16]	1000	1000	1000	1000	1000	1000	1000	1000	39	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[17]	1000	1000	1000	1000	1000	1000	1000	1000	29	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[18]	1000	1000	1000	1000	1000	1000	1000	1000	37	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[19]	1000	1000	1000	1000	1000	1000	1000	1000	23	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	1000	1000	1000
tx[20]	0	0	0	0	0	0	0	388	79	0	0	0	0	0	0	0	0	0	0	0	654	986	0	0	0	0
tx[21]	0	0	0	0	0	0	0	323	54	0	0	0	0	0	0	0	0	0	0	0	656	974	0	0	0	0
tx[22]	0	0	0	0	0	0	0	348	77	0	0	0	0	0	0	0	0	0	0	0	646	983	0	0	0	0
tx[23]	0	0	0	0	0	0	0	341	53	0	0	0	0	0	0	0	0	0	0	0	681	978	0	0	0	0
tx[24]	0	0	0	0	0	0	0	340	78	0	0	0	0	0	0	0	0	0	0	0	641	982	0	0	0	0
tx[25]	0	0	0	0	0	0	0	344	54	0	0	0	0	0	0	0	0	0	0	0	671	976	0	0	0	0
tx[26]	0	0	0	0	0	0	0	373	79	0	0	0	0	0	0	0	0	0	0	0	660	984	0	0	0	0
tx[27]	0	0	0	0	0	0	0	342	58	0	0	0	0	0	0	0	0	0	0	0	696	984	0	0	0	0

ALCT672 TMB tx/rx scan

- Changed UCF constraints setting
  - SLEW=SLOW ==> SLEW=FAST
  - DRIVE=12 ==> DRIVE=4
  - **Nice wide window now… should investigate further.. but tentatively OK**
    - **Rx window gets wider also… should investigate on 384 boards also**
    - **Should try other combinations of settings as well**

Cable Pair Errors vs alct_txd_clock Delay Step

delay	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
pair																										
tx[0]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	215	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[1]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	197	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[2]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	209	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[3]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	206	0	0	0	0	0	0	0	0	0	0	983	0	1000	1000	
tx[4]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	195	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[5]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	208	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[6]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	211	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[7]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	228	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[8]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	203	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[9]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	211	0	0	0	0	0	0	0	0	0	0	983	1	1000	1000	
tx[10]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	999	1000	1000	
tx[11]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[12]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	999	1000	1000	
tx[13]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	999	1000	1000	
tx[14]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[15]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[16]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[17]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[18]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[19]	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	1000	0	0	0	0	0	0	0	0	0	0	0	1000	1000	1000	
tx[20]	0	0	0	0	0	0	0	0	0	0	805	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[21]	0	0	0	0	0	0	0	0	0	0	793	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[22]	0	0	0	0	0	0	0	0	0	0	774	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[23]	0	0	0	0	0	0	0	0	0	0	811	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[24]	0	0	0	0	0	0	0	0	0	0	783	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[25]	0	0	0	0	0	0	0	0	0	0	804	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[26]	0	0	0	0	0	0	0	0	0	0	792	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	
tx[27]	0	0	0	0	0	0	0	0	0	0	810	0	0	0	0	0	0	0	0	0	0	0	1000	0	0	