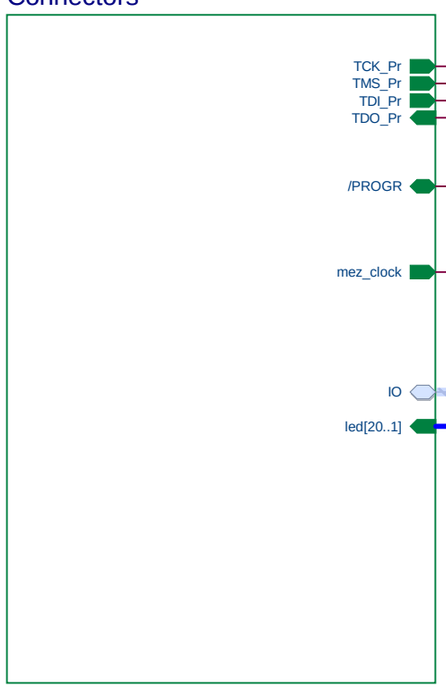
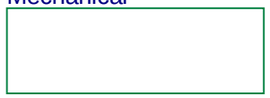
UCLA Spartan-6 LX100 Optical FPGA Mezzanine

Connectors



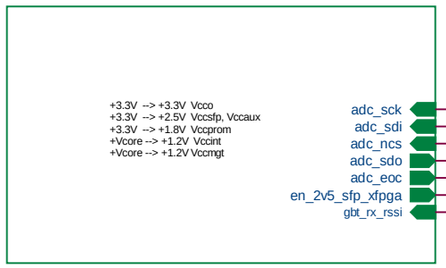
Connectors.SchDoc

Mechanical



Mechanical.SchDoc

POWER+ADC



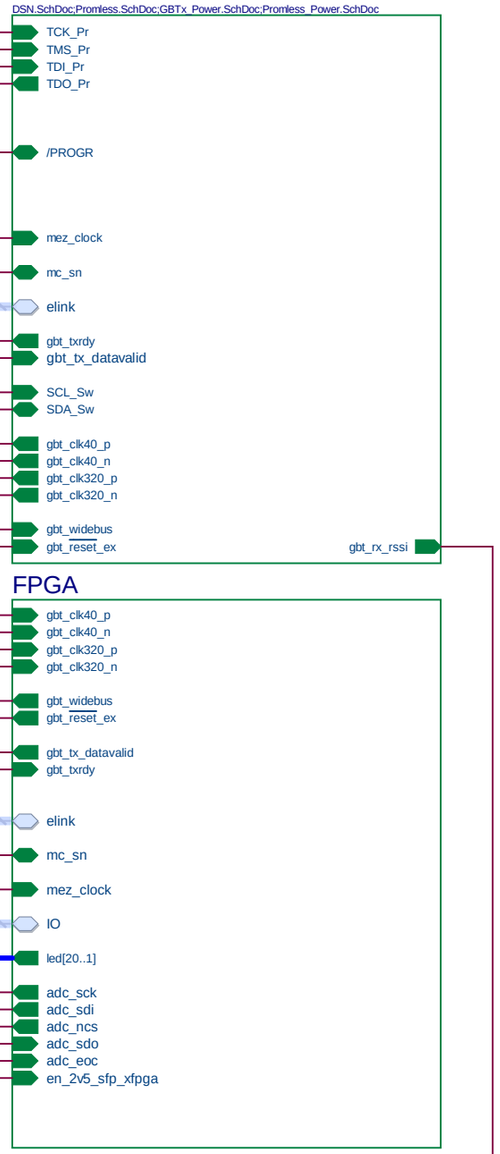
Power.SchDoc;ADC.SchDoc

Configuration

DSN.SchDoc;Promless.SchDoc;GBTx_Power.SchDoc;Promless_Power.SchDoc

TTC Clock

FPGA



FPGA_Power.SchDoc;FPGA_IO.SchDoc;FPGA_Ground.SchDoc

Overview		
ALCT S-6 LX100 Optical Mezzanine		
UCLA High Energy Physics		
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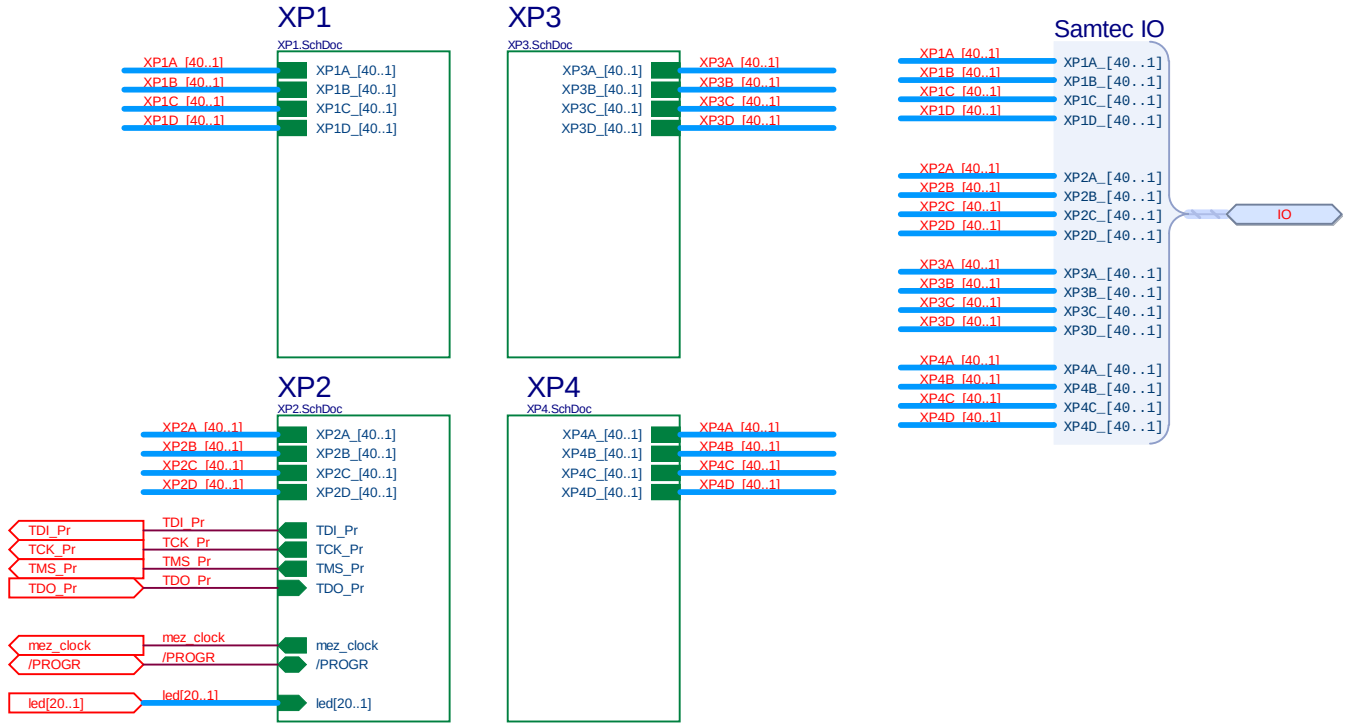
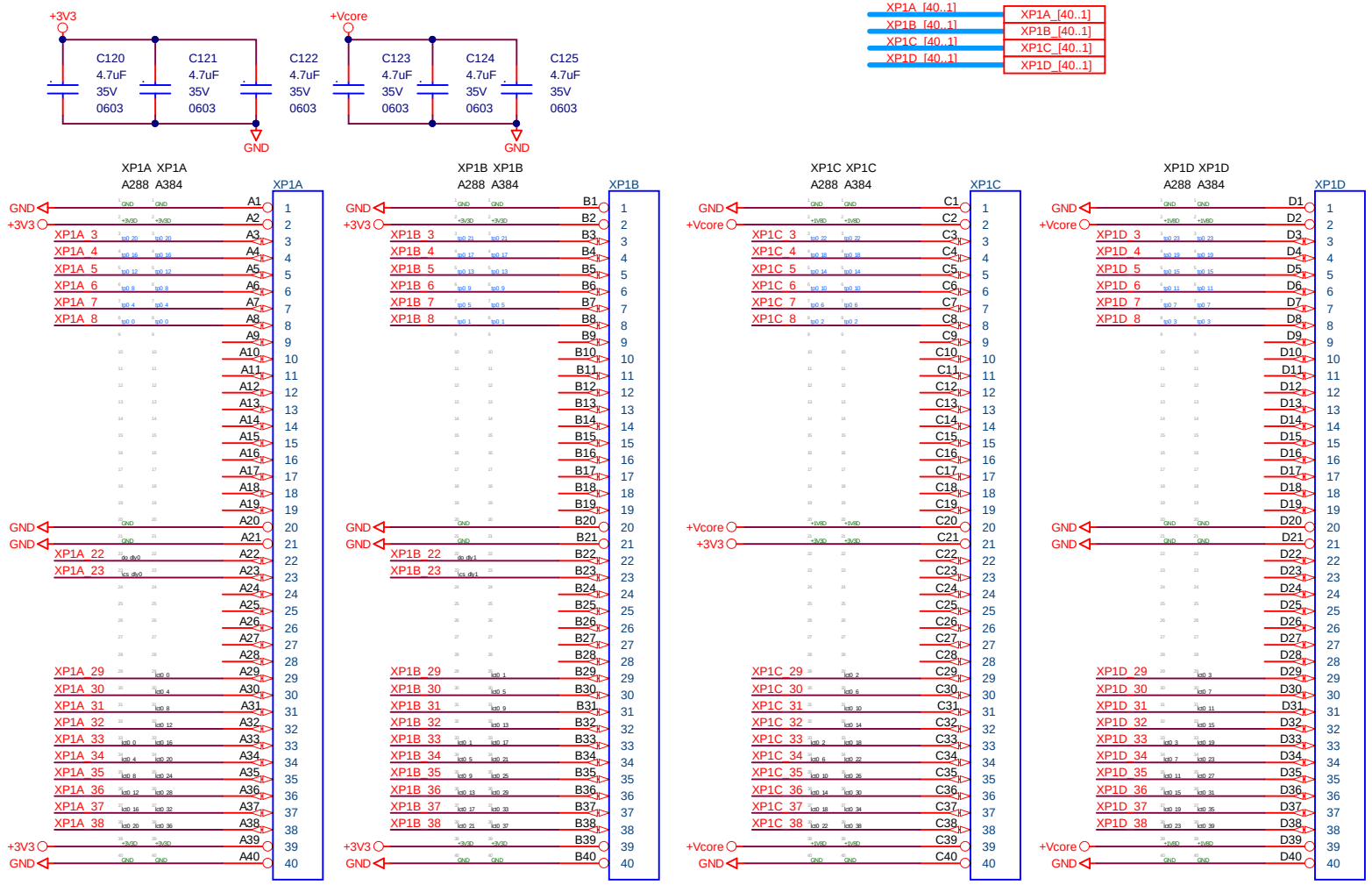


Mezzanine Connectors			
ALCT S-6 LX100 Optical Mezzanine			
UCLA High Energy Physics			
Date: 9/13/2018	Rev: 2.0	Sheet 2 of 23	



XP1 Connections

ALCT S-6 LX100 Optical Mezzanine

UCLA High Energy Physics

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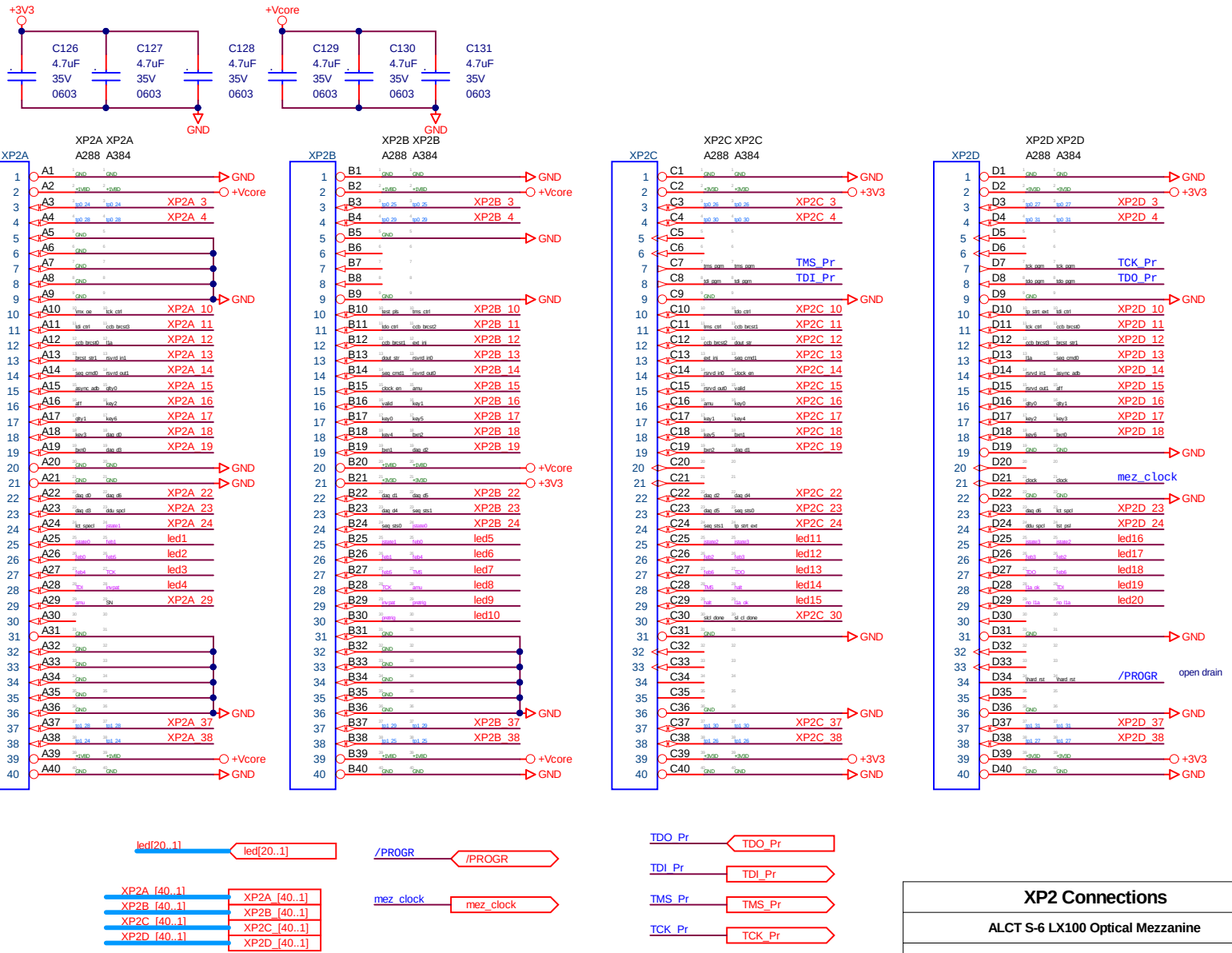

XP2 Connections

ALCT S-6 LX100 Optical Mezzanine

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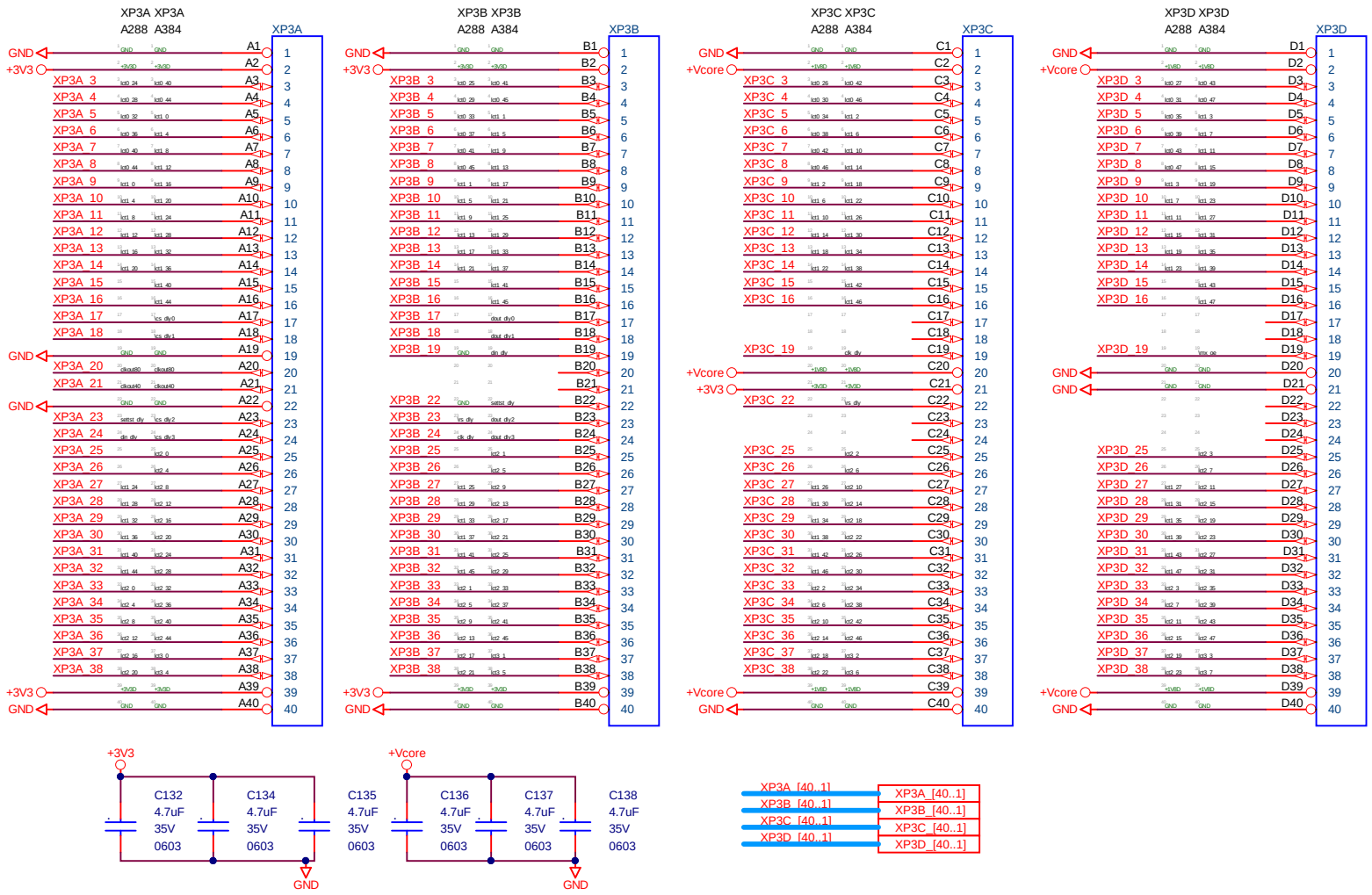

XP3 Connections

ALCT S-6 LX100 Optical Mezzanine

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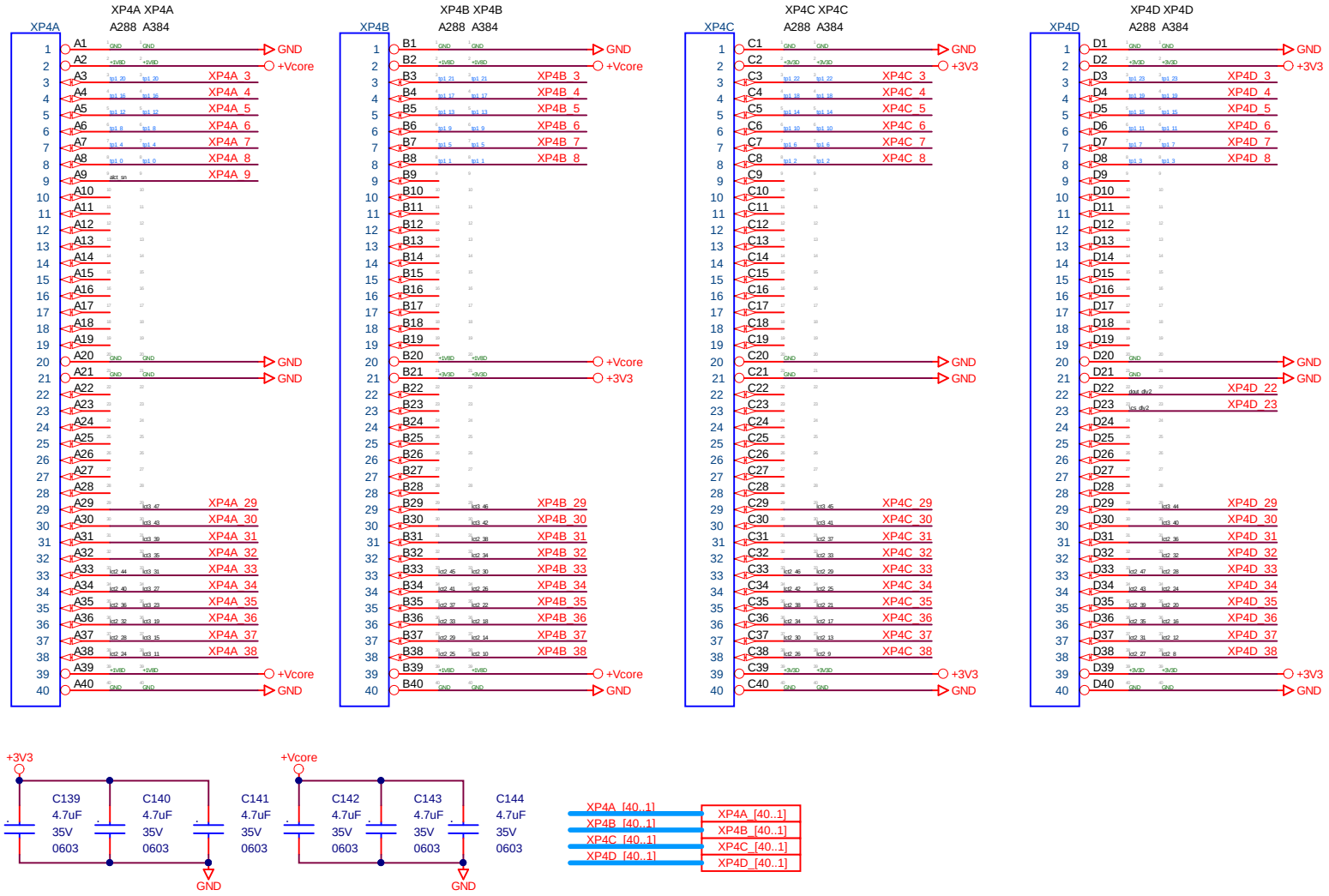

XP4 Connections

ALCT S-6 LX100 Optical Mezzanine

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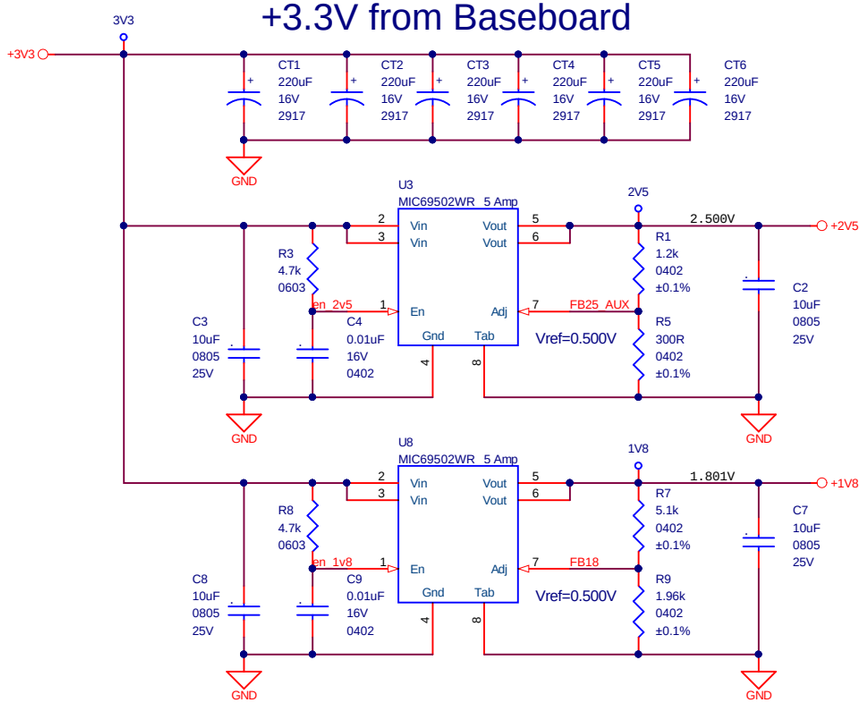
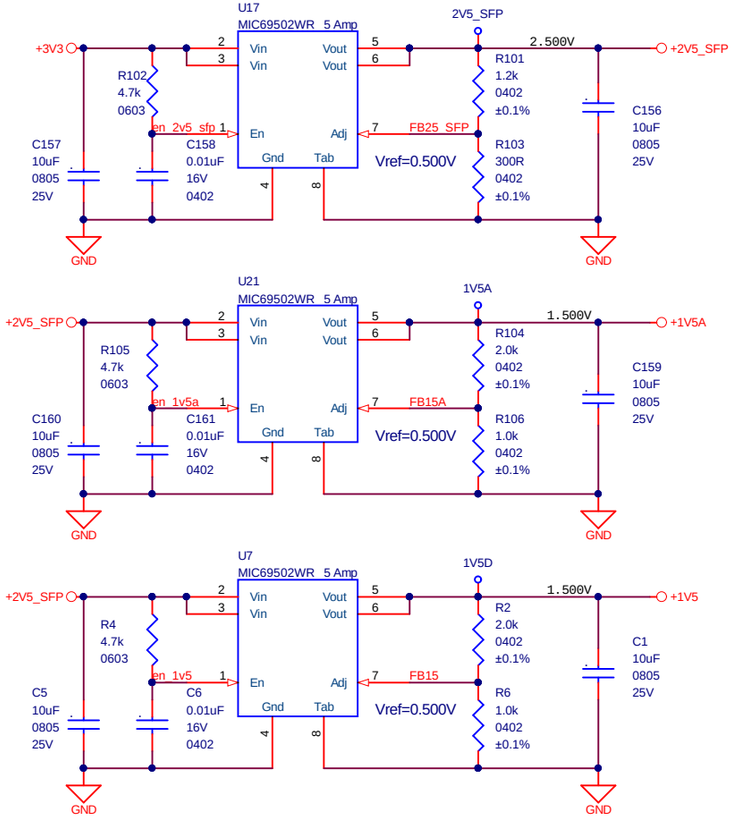


2.5V VCCAUX

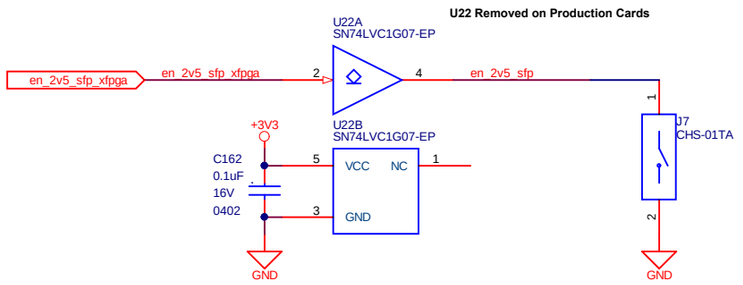
1.8V PROM

1.2V FPGA VCCINT



1.5V GBTA

1.5V GBTD



Power	
ALCT S-6 LX100 Optical Mezzanine	
UCLA High Energy Physics	
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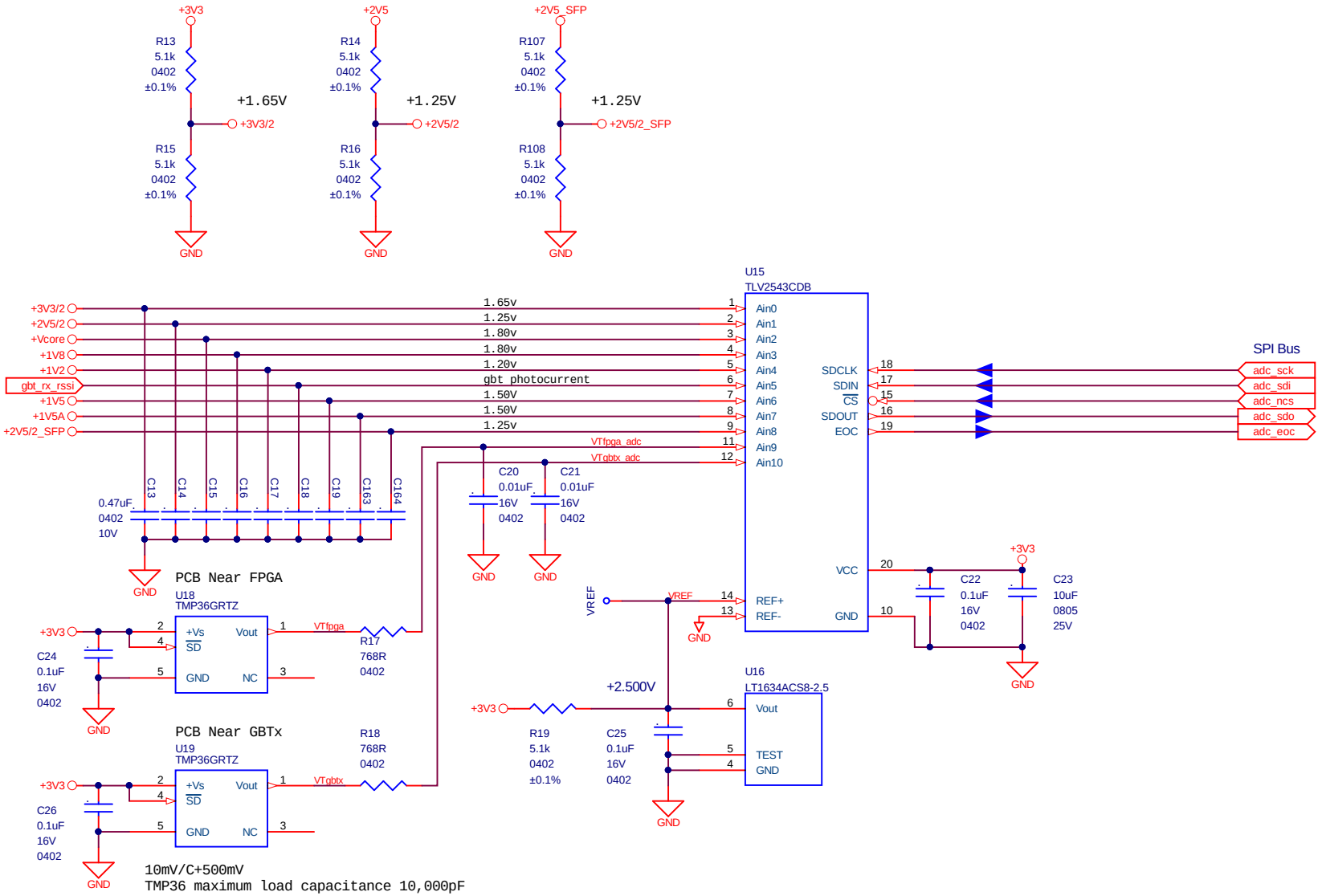
Divide voltages greater than 2.5V to fit in VREF range



ADC	
ALCT S-6 LX100 Optical Mezzanine	
UCLA High Energy Physics	
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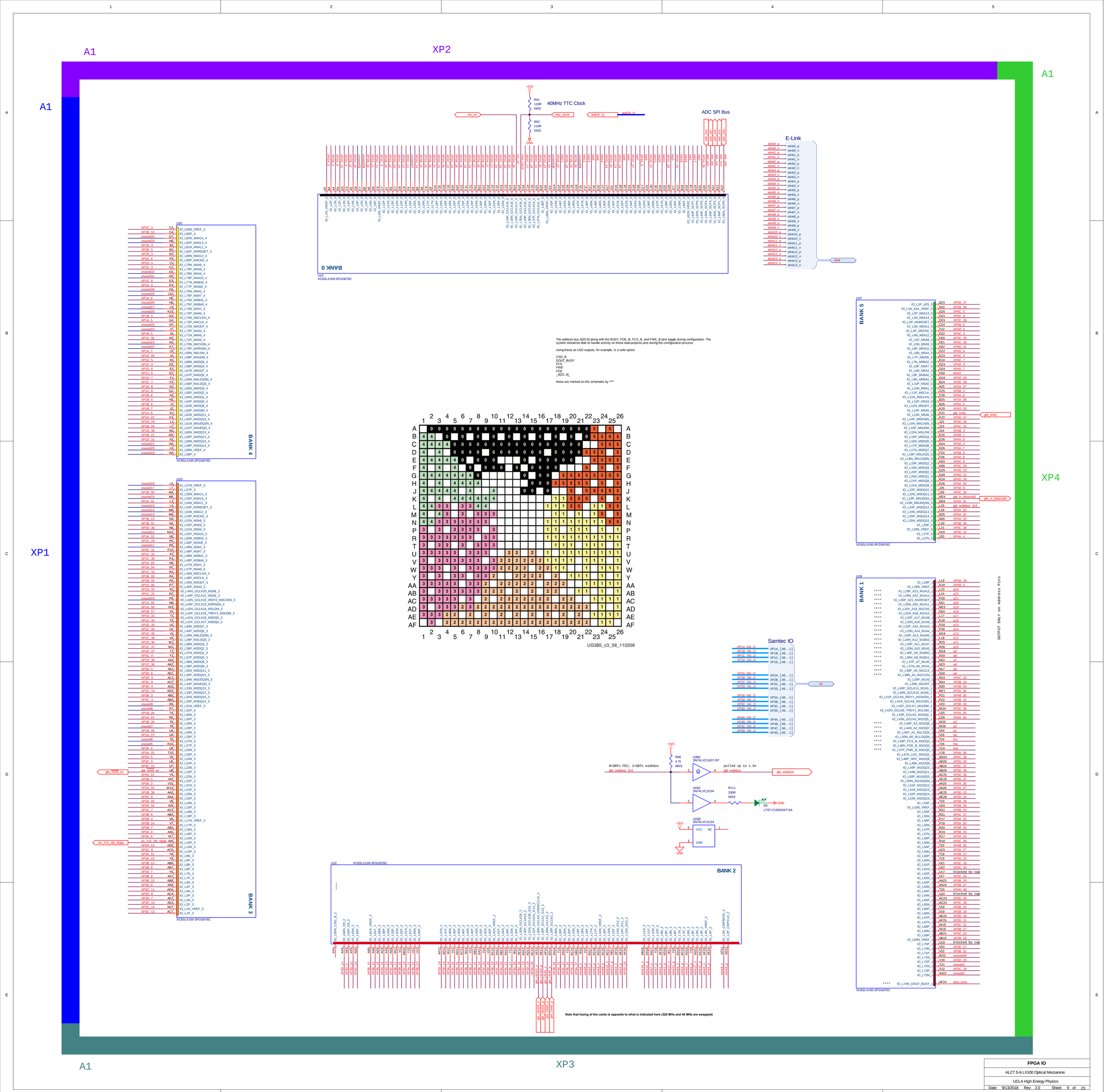
A1
XP2
A1
XP1
XP4
XP3
40MHz TTC Clock
R91
110R
0402
R92
110R
0402
+3V3
GND
mc_sn
mez_clock
led[20..1]
led[20..1]
ADC SPI Bus
adc_sclk
adc_sdi
adc_sck
adc_sdo
E-Link
elink0_p
elink0_n
elink1_p
elink1_n
elink2_p
elink2_n
elink3_p
elink3_n
elink4_p
elink4_n
elink5_p
elink5_n
elink6_p
elink6_n
elink7_p
elink7_n
elink8_p
elink8_n
elink9_p
elink9_n
elink10_p
elink10_n
elink11_p
elink11_n
elink12_p
elink12_n
elink13_p
elink13_n
elink
BANK 0
U1A
XC6SLX100-3FGG676C
U1E
BANK 4
XC6SLX100-3FGG676C
U1D
BANK 3
XC6SLX100-3FGG676C
U1F
BANK 5
XC6SLX100-3FGG676C
U1B
BANK 1
XC6SLX100-3FGG676C
U1C
XC6SLX100-3FGG676C
BANK 2
Samtec IO
XP1A [40..1]
XP1B [40..1]
XP1C [40..1]
XP1D [40..1]
XP2A [40..1]
XP2B [40..1]
XP2C [40..1]
XP2D [40..1]
XP3A [40..1]
XP3B [40..1]
XP3C [40..1]
XP3D [40..1]
XP4A [40..1]
XP4B [40..1]
XP4C [40..1]
XP4D [40..1]
IO
gbt_reset_ex
en_2v5_sfp_xfpga
+3V3
R98
4.7K
0603
U39A
SN74LVC1G07-EP
0=GBTx FEC; 1=GBTx widebus
gbt_widebus_3v3
pulled up to 1.5v
gbt_widebus
U43A
SN74LVC1G34
R111
330R
0603
D9
LTST-C193KGKT-5A
GND
U43B
SN74LVC1G34
VCC
NC
GND
The address bus A[25:0] along with the BUSY, FOE_B, FCS_B, and FWE_B pins toggle during configuration. The system should be able to handle activity on these dual-purpose pins during the configuration process
Using these as LED outputs, for example, is a safe option
CSO_B
DOUT_BUSY
FCS
FWE
FOE
_A[25..0]_
these are marked on the schematic by ****
gbt_txrdy
gbt_tx_datavalid
gbt_widebus_3v3
OUTPUT ONLY on Address Pins
UG385_c3_56_110209
Note that fusing of the cards is opposite to what is indicated here (320 MHz and 40 MHz are swapped)
A1
XP3
FPGA IO
ALCT S-6 LX100 Optical Mezzanine
UCLA High Energy Physics
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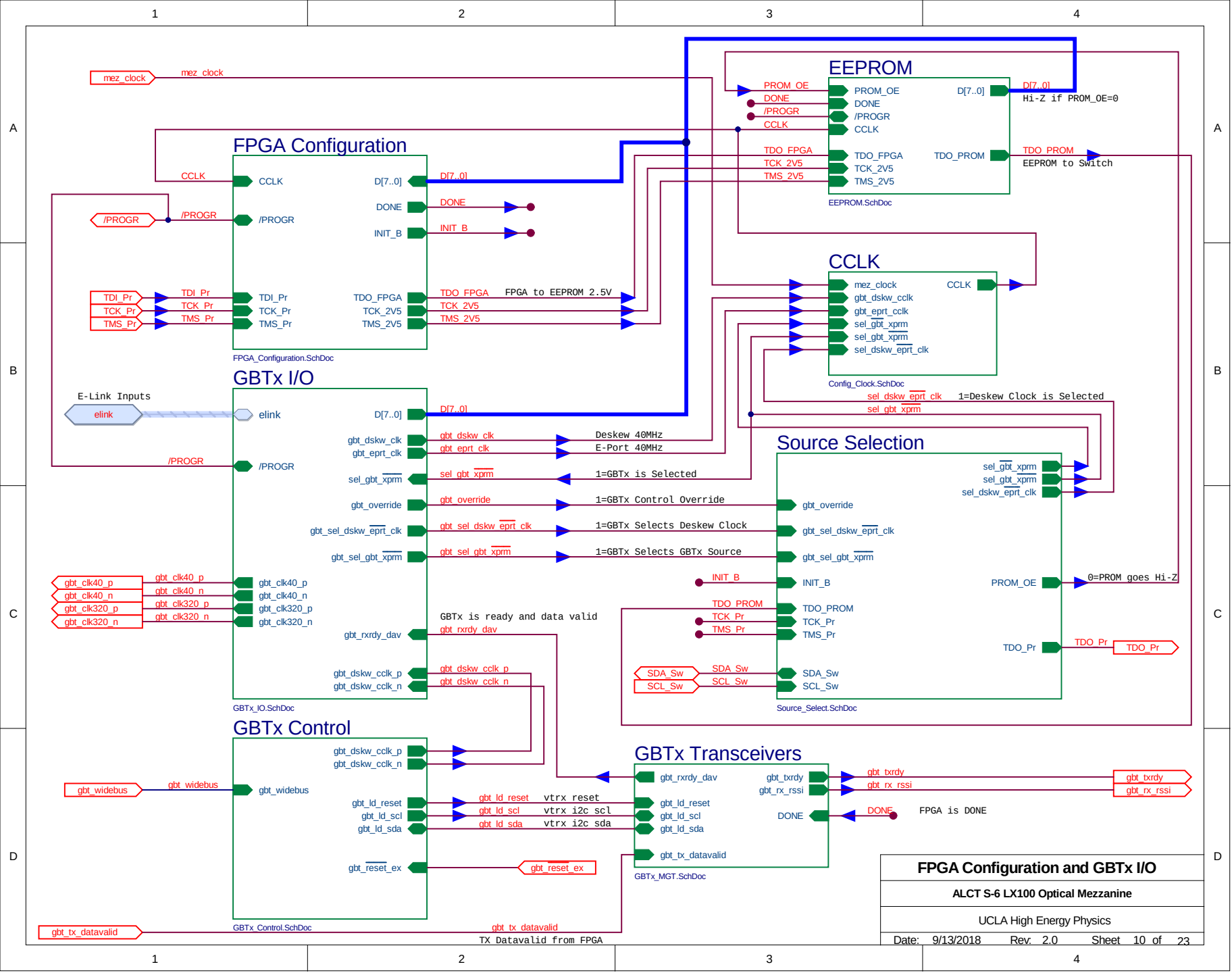
EEPROM
FPGA Configuration
CCLK
GBTx I/O
Source Selection
GBTx Control
GBTx Transceivers
mez_clock
/PROGR
TDI_Pr
TCK_Pr
TMS_Pr
PROM_OE
DONE
CCLK
TDO_FPGA
TCK_2V5
TMS_2V5
TDO_PROM
D[7..0]
INIT_B
Hi-Z if PROM_OE=0
EEPROM to Switch
FPGA to EEPROM 2.5V
EEPROM.SchDoc
FPGA_Configuration.SchDoc
Config_Clock.SchDoc
E-Link Inputs
elink
gbt_dskw_clk
gbt_eprt_clk
Deskew 40MHz
E-Port 40MHz
sel_gbt_xprm
1=GBTx is Selected
gbt_override
1=GBTx Control Override
gbt_sel_dskw_eprt_clk
1=GBTx Selects Deskew Clock
gbt_sel_gbt_xprm
1=GBTx Selects GBTx Source
1=Deskew Clock is Selected
gbt_clk40_p
gbt_clk40_n
gbt_clk320_p
gbt_clk320_n
GBTx is ready and data valid
gbt_rxrdy_dav
gbt_dskw_cclk_p
gbt_dskw_cclk_n
INIT_B
0=PROM goes Hi-Z
SDA_Sw
SCL_Sw
GBTx_IO.SchDoc
Source_Select.SchDoc
gbt_widebus
gbt_ld_reset
gbt_ld_scl
gbt_ld_sda
vtrx reset
vtrx i2c scl
vtrx i2c sda
gbt_reset_ex
GBTx_Control.SchDoc
gbt_txrdy
gbt_rx_rssi
gbt_tx_datavalid
FPGA is DONE
TX Datavalid from FPGA
GBTx_MGT.SchDoc
FPGA Configuration and GBTx I/O
ALCT S-6 LX100 Optical Mezzanine
UCLA High Energy Physics
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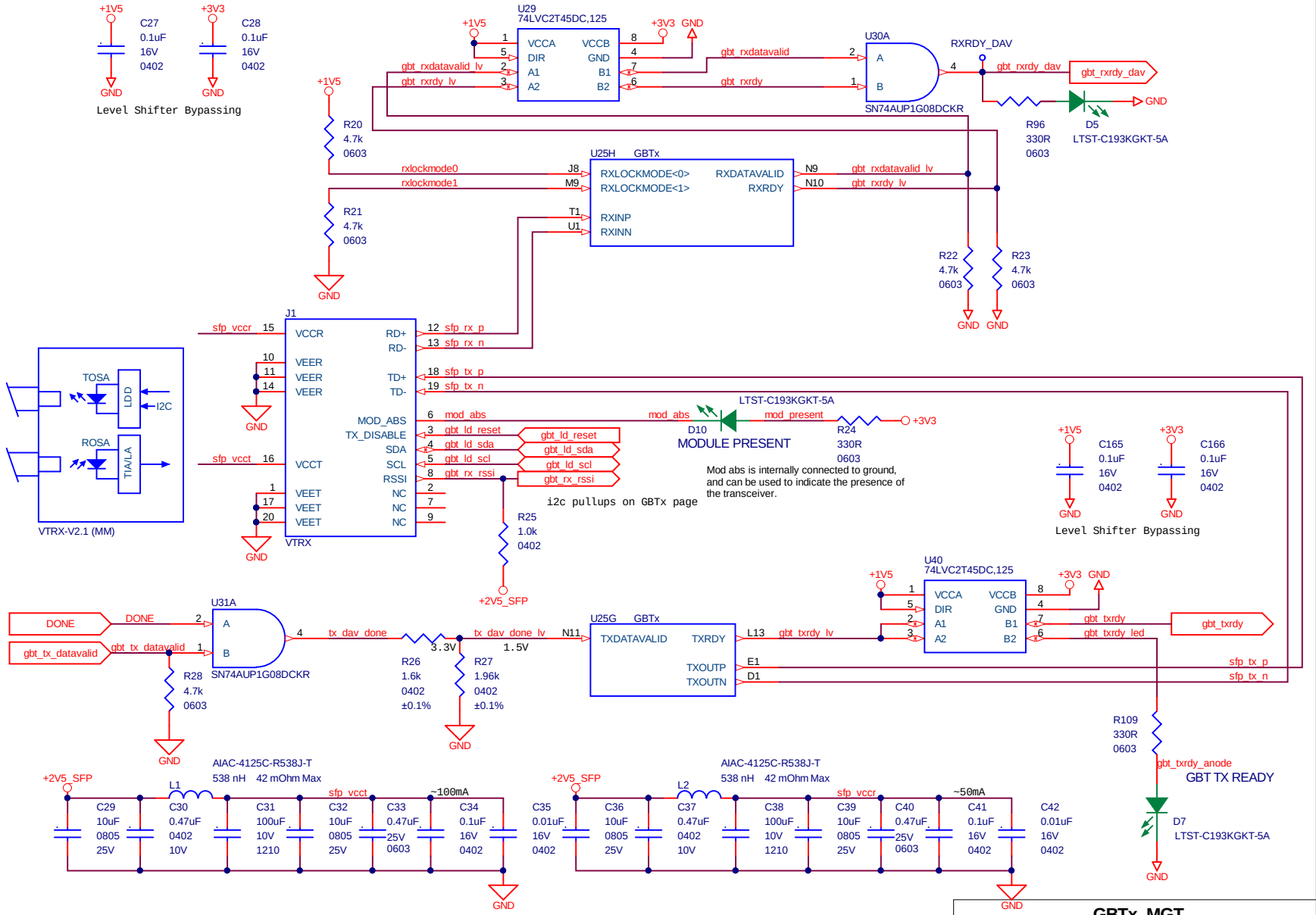
C27 0.1uF 16V 0402
C28 0.1uF 16V 0402
Level Shifter Bypassing
U29 74LVC2T45DC,125
VCCA VCCB DIR GND A1 B1 A2 B2
gbt_rxdatavalid_lv
gbt_rxrdy_lv
gbt_rxdatavalid
gbt_rxrdy
U30A
SN74AUP1G08DCKR
RXRDY_DAV
gbt_rxrdy_dav
R96 330R 0603
D5 LTST-C193KGKT-5A
R20 4.7k 0603
R21 4.7k 0603
U25H GBTx
RXLOCKMODE<0>
RXLOCKMODE<1>
RXDATAVALID
RXRDY
RXINP
RXINN
rxlockmode0
rxlockmode1
R22 4.7k 0603
R23 4.7k 0603
J1
VCCR VEER VEER VEER VCCT VEET VEET VEET
RD+ RD- TD+ TD-
MOD_ABS TX_DISABLE SDA SCL RSSI NC NC NC
sfp_vccr sfp_vcct
sfp_rx_p sfp_rx_n sfp_tx_p sfp_tx_n
mod_abs gbt_ld_reset gbt_ld_sda gbt_ld_scl gbt_rx_rssi
VTRX
VTRX-V2.1 (MM)
TOSA ROSA LDD TIA/LA I2C
LTST-C193KGKT-5A
D10 MODULE PRESENT
mod_present
R24 330R 0603
Mod abs is internally connected to ground, and can be used to indicate the presence of the transceiver.
i2c pullups on GBTx page
R25 1.0k 0402
+2V5_SFP
C165 0.1uF 16V 0402
C166 0.1uF 16V 0402
Level Shifter Bypassing
U40 74LVC2T45DC,125
gbt_txrdy
gbt_txrdy_led
U31A
SN74AUP1G08DCKR
DONE
gbt_tx_datavalid
tx_dav_done
tx_dav_done_lv
R26 1.6k 0402 ±0.1%
R27 1.96k 0402 ±0.1%
R28 4.7k 0603
U25G GBTx
TXDATAVALID TXRDY TXOUTP TXOUTN
L13 gbt_txrdy_lv
E1 D1
R109 330R 0603
gbt_txrdy_anode
GBT TX READY
D7 LTST-C193KGKT-5A
AIAC-4125C-R538J-T 538 nH 42 mOhm Max
L1
C29 10uF 0805 25V
C30 0.47uF 0402 10V
C31 100uF 10V 1210
C32 10uF 0805 25V
C33 0.47uF 25V 0603
C34 0.1uF 16V 0402
~100mA
L2
C35 0.01uF 16V 0402
C36 10uF 0805 25V
C37 0.47uF 0402 10V
C38 100uF 10V 1210
C39 10uF 0805 25V
C40 0.47uF 25V 0603
C41 0.1uF 16V 0402
C42 0.01uF 16V 0402
~50mA
GBTx_MGT
ALCT S-6 LX100 Optical Mezzanine
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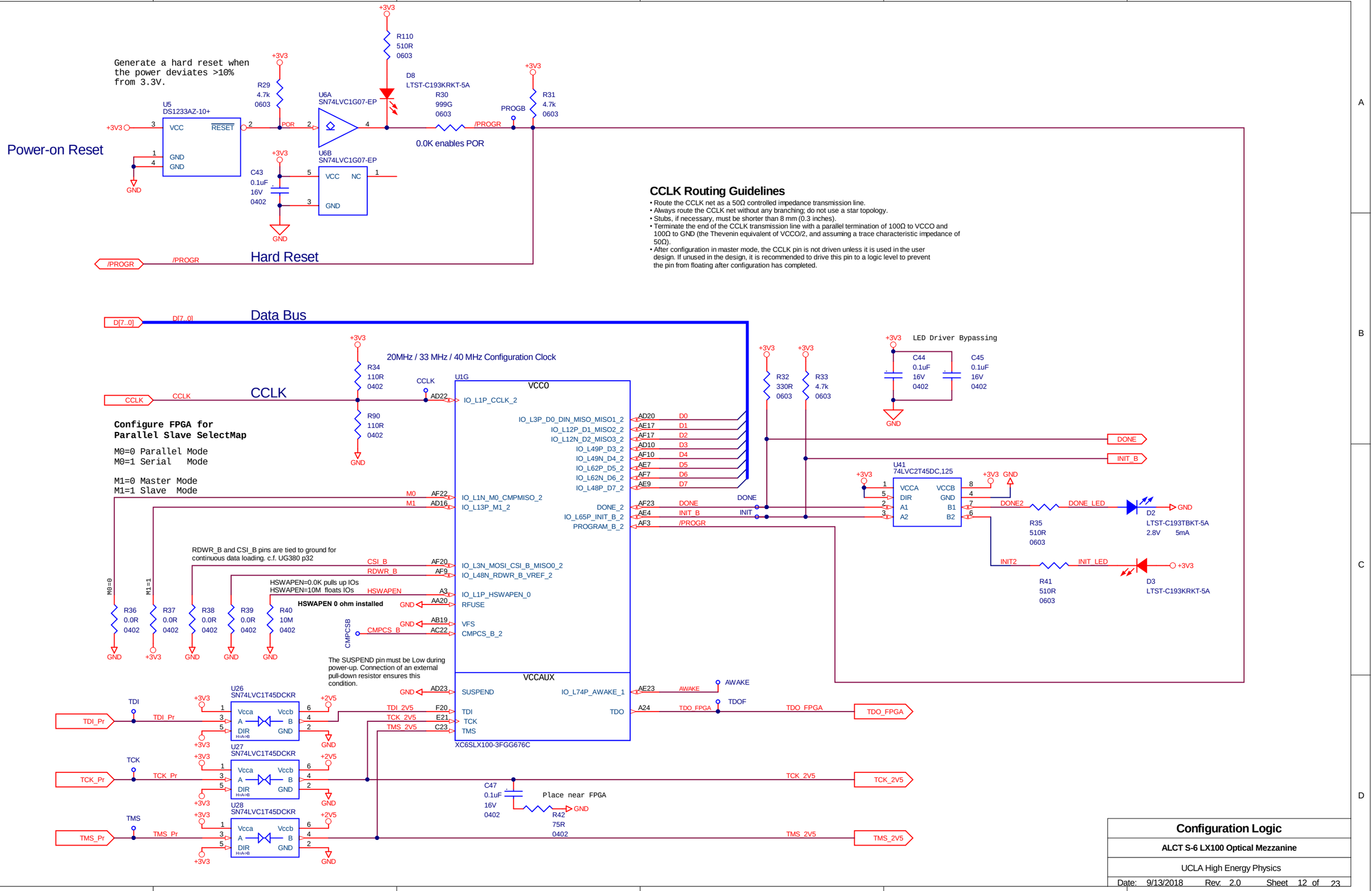

Configuration Logic		
ALCT S-6 LX100 Optical Mezzanine		
UCLA High Energy Physics		
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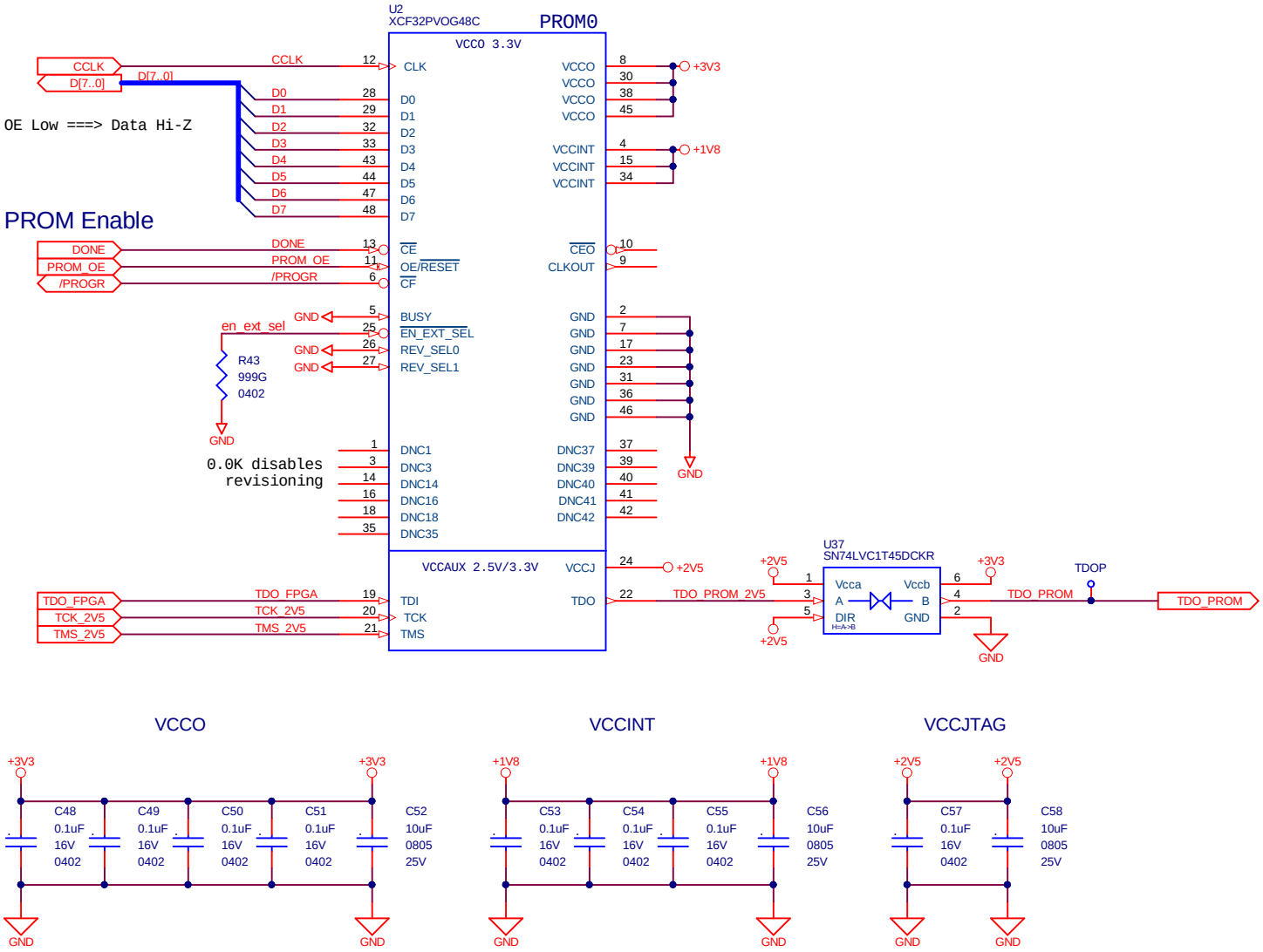

EEPROM	
ALCT S-6 LX100 Optical Mezzanine	
UCLA High Energy Physics	
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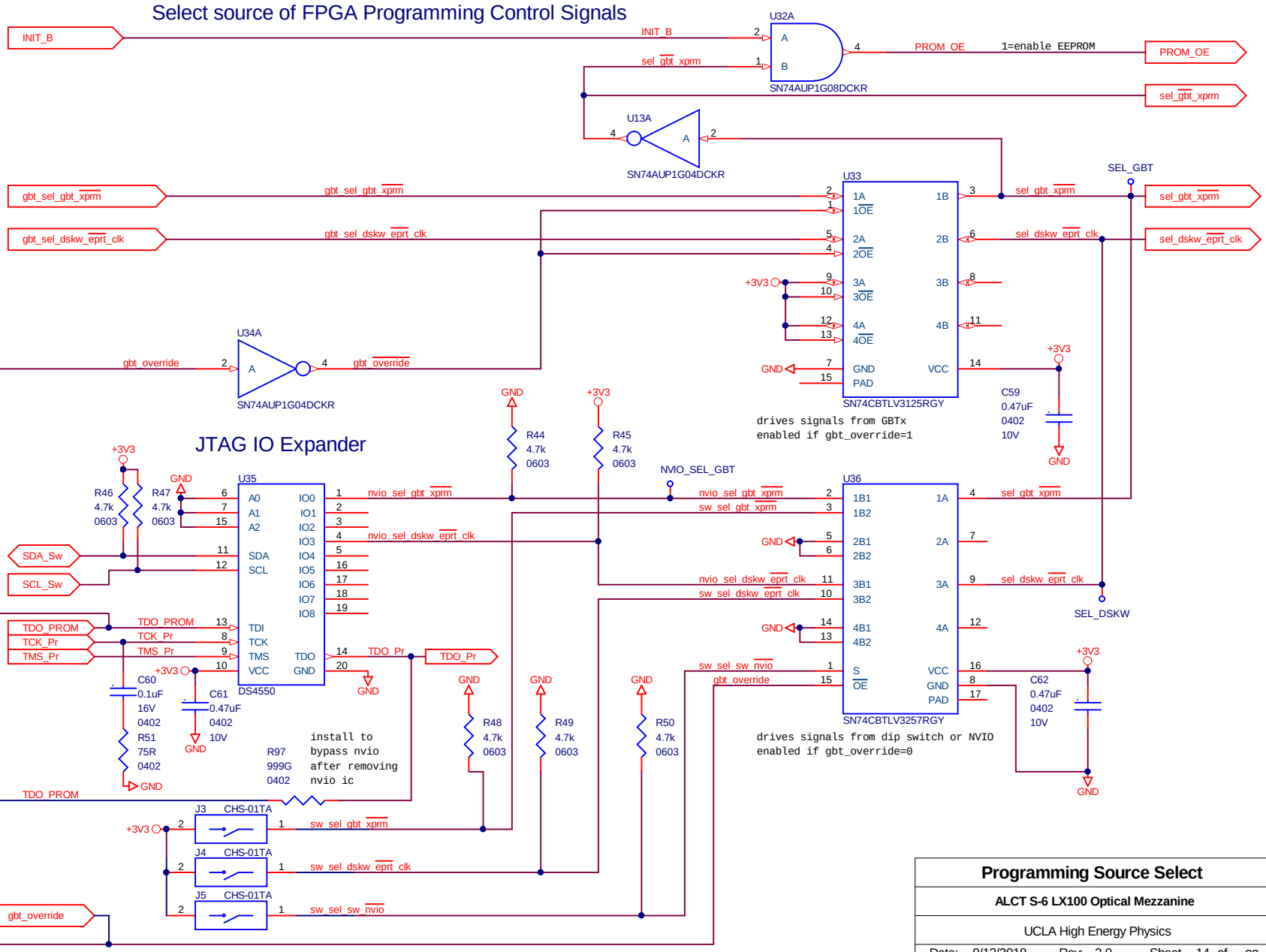
Select source of FPGA Programming Control Signals
INIT_B
U32A
SN74AUP1G08DCKR
PROM_OE
1=enable EEPROM
sel_gbt_xprm
U13A
SN74AUP1G04DCKR
SEL_GBT
gbt_sel_gbt_xprm
gbt_sel_dskw_eprt_clk
U33
SN74CBTLV3125RGY
drives signals from GBTx
enabled if gbt_override=1
U34A
gbt_override
SN74AUP1G04DCKR
C59
0.47uF
0402
10V
JTAG IO Expander
U35
DS4550
R44
4.7k
0603
R45
4.7k
0603
R46
4.7k
0603
R47
4.7k
0603
NVIO_SEL_GBT
nvio_sel_gbt_xprm
nvio_sel_dskw_eprt_clk
SDA_Sw
SCL_Sw
TDO_PROM
TCK_Pr
TMS_Pr
TDO_Pr
C60
0.1uF
16V
0402
C61
0.47uF
0402
10V
R51
75R
0402
R97
999G
0402
install to
bypass nvio
after removing
nvio ic
U36
SN74CBTLV3257RGY
sw_sel_gbt_xprm
sw_sel_dskw_eprt_clk
sw_sel_sw_nvio
drives signals from dip switch or NVIO
enabled if gbt_override=0
SEL_DSKW
C62
0.47uF
0402
10V
R48
4.7k
0603
R49
4.7k
0603
R50
4.7k
0603
J3 CHS-01TA
J4 CHS-01TA
J5 CHS-01TA
Programming Source Select
ALCT S-6 LX100 Optical Mezzanine
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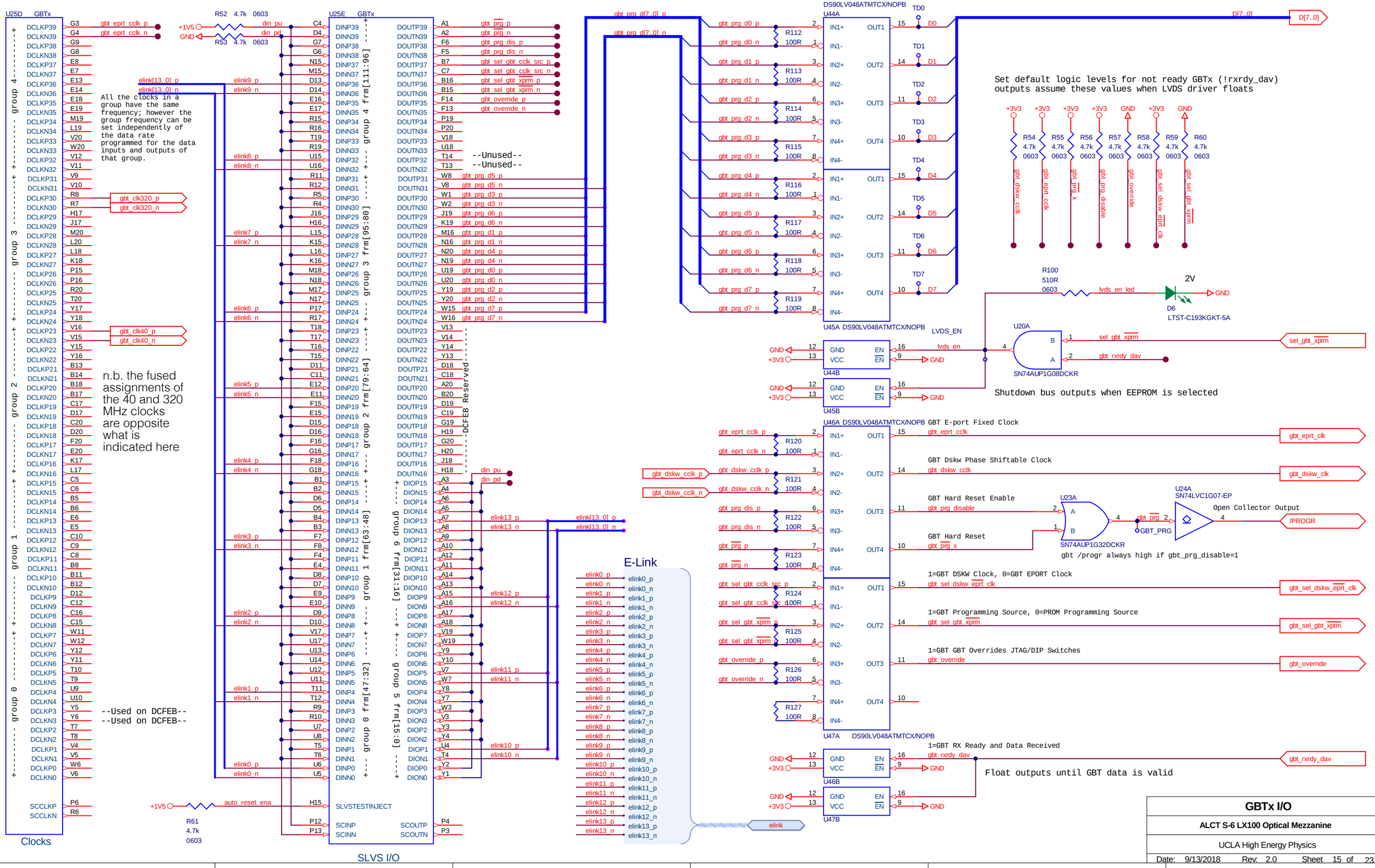
U25D GBTx
U25E GBTx
All the clocks in a group have the same frequency; however the group frequency can be set independently of the data rate programmed for the data inputs and outputs of that group.
n.b. the fused assignments of the 40 and 320 MHz clocks are opposite what is indicated here
--Used on DCFEB--
--Used on DCFEB--
--Unused--
--Unused--
DCFEB Reserved
Clocks
SLVS I/O
E-Link
DS90LV048ATMTCX/NOPB
U44A
U45A DS90LV048ATMTCX/NOPB
U45B
U46A DS90LV048ATMTCX/NOPB GBT E-port Fixed Clock
U47A DS90LV048ATMTCX/NOPB
U46B
U47B
LVDS_EN
Set default logic levels for not ready GBTx (!rxrdy_dav) outputs assume these values when LVDS driver floats
Shutdown bus outputs when EEPROM is selected
SN74AUP1G08DCKR
SN74AUP1G32DCKR
SN74LVC1G07-EP
Open Collector Output
gbt /progr always high if gbt_prg_disable=1
GBT Dskw Phase Shiftable Clock
GBT Hard Reset Enable
GBT Hard Reset
1=GBT DSKW Clock, 0=GBT EPORT Clock
1=GBT Programming Source, 0=PROM Programming Source
1=GBT GBT Overrides JTAG/DIP Switches
1=GBT RX Ready and Data Received
Float outputs until GBT data is valid
D6
LTST-C193KGKT-5A
GBTx I/O
ALCT S-6 LX100 Optical Mezzanine
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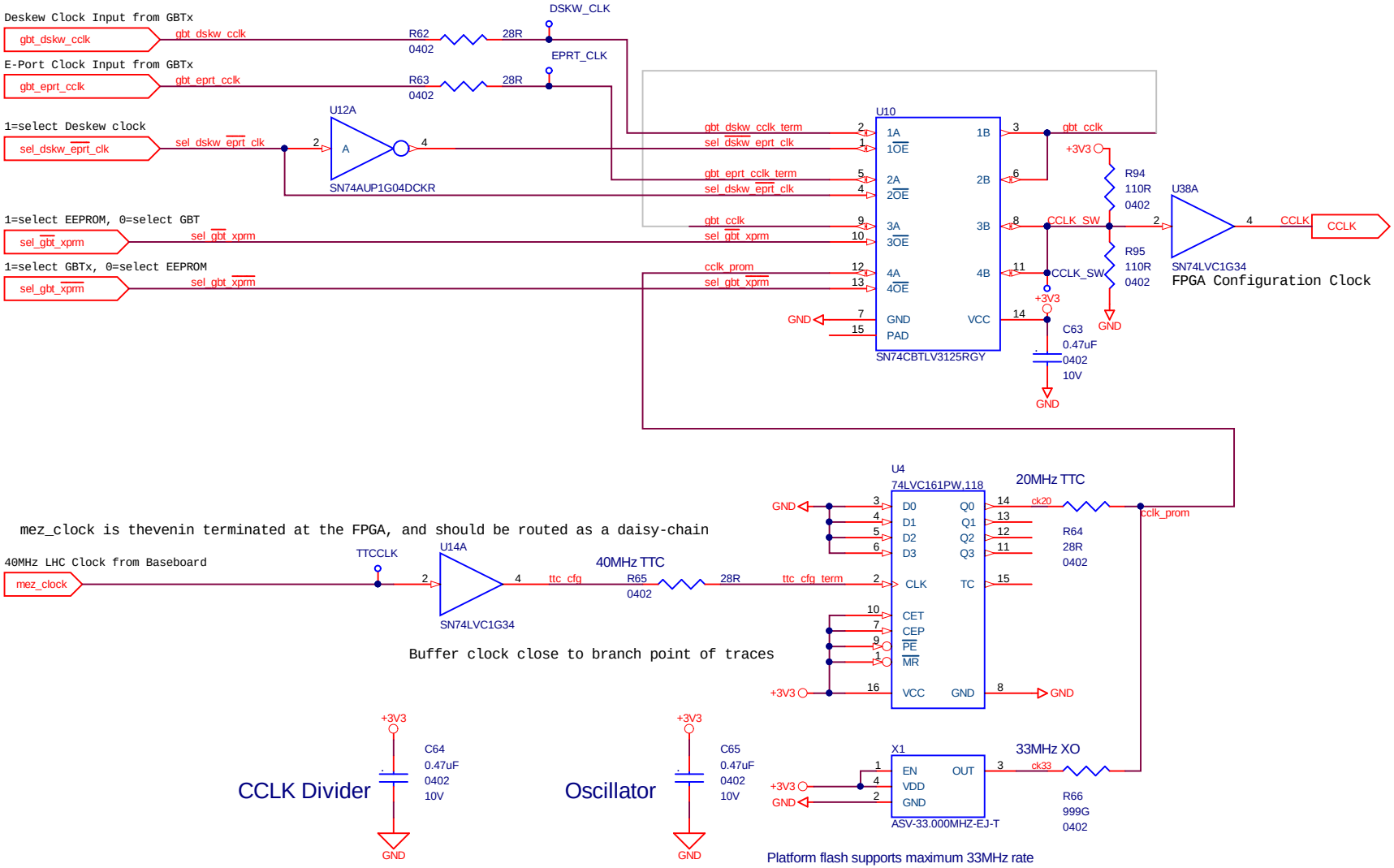

Configuration Clock	
ALCT S-6 LX100 Optical Mezzanine	
UCLA High Energy Physics	
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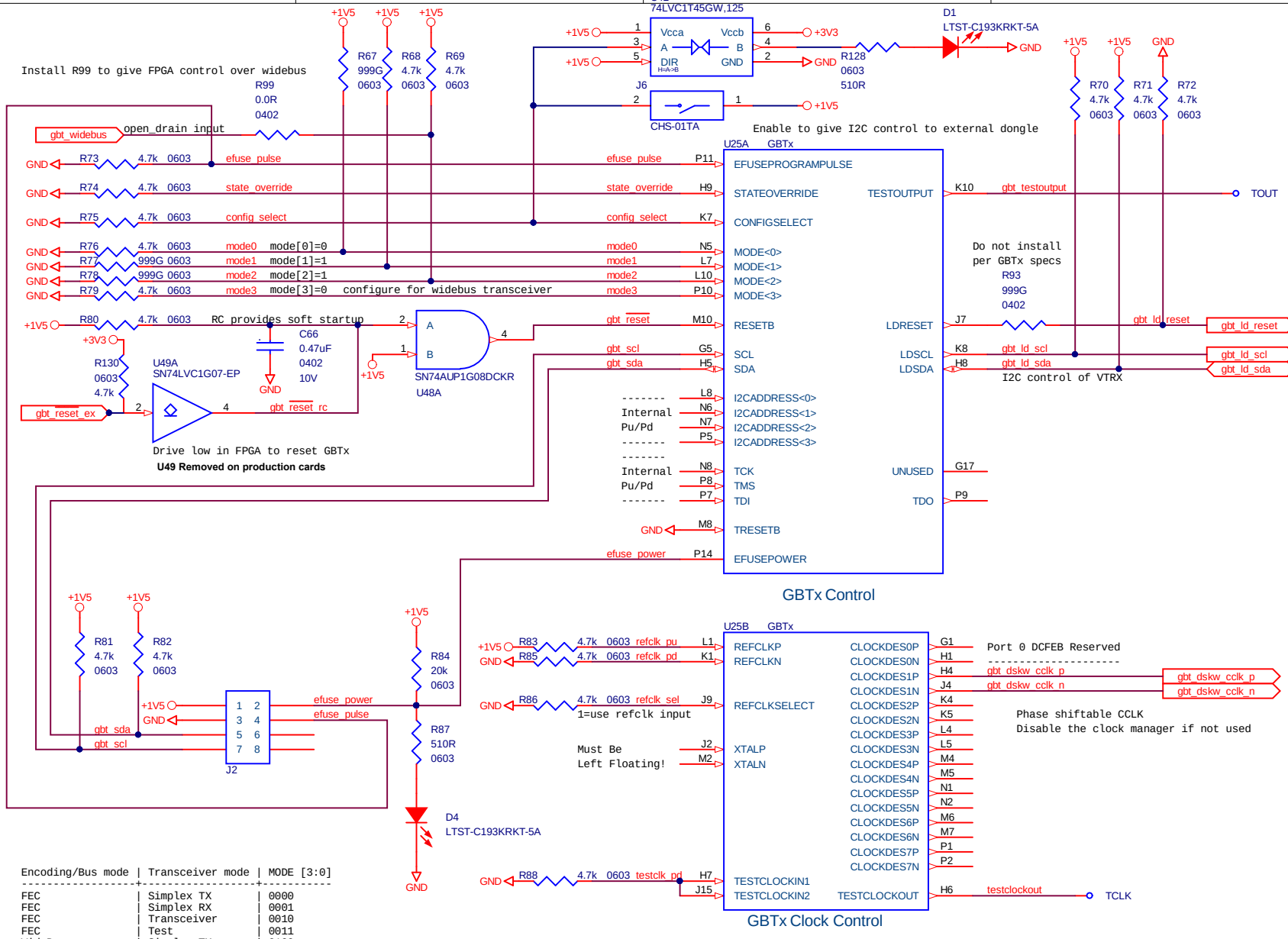
Install R99 to give FPGA control over widebus
R99 0.0R 0402
gbt_widebus
open_drain input
R67 999G 0603
R68 4.7k 0603
R69 4.7k 0603
U42 74LVC1T45GW,125
Vcca
Vccb
A
B
DIR
GND
R128 0603 510R
D1 LTST-C193KRKT-5A
J6
CHS-01TA
Enable to give I2C control to external dongle
R70 4.7k 0603
R71 4.7k 0603
R72 4.7k 0603
R73 4.7k 0603 efuse_pulse
R74 4.7k 0603 state_override
R75 4.7k 0603 config_select
R76 4.7k 0603 mode0 mode[0]=0
R77 999G 0603 mode1 mode[1]=1
R78 999G 0603 mode2 mode[2]=1
R79 4.7k 0603 mode3 mode[3]=0 configure for widebus transceiver
U25A GBTx
EFUSEPROGRAMPULSE
STATEOVERRIDE
CONFIGSELECT
MODE<0>
MODE<1>
MODE<2>
MODE<3>
RESETB
SCL
SDA
I2CADDRESS<0>
I2CADDRESS<1>
I2CADDRESS<2>
I2CADDRESS<3>
TCK
TMS
TDI
TRESETB
EFUSEPOWER
TESTOUTPUT
LDRESET
LDSCL
LDSDA
UNUSED
TDO
Do not install per GBTx specs
R93 999G 0402
I2C control of VTRX
R80 4.7k 0603 RC provides soft startup
C66 0.47uF 0402 10V
R130 0603 4.7k
U49A SN74LVC1G07-EP
gbt_reset_ex
gbt_reset_rc
U48A SN74AUP1G08DCKR
Drive low in FPGA to reset GBTx
U49 Removed on production cards
GBTx Control
R81 4.7k 0603
R82 4.7k 0603
R84 20k 0603
R87 510R 0603
J2
D4 LTST-C193KRKT-5A
U25B GBTx
R83 4.7k 0603 refclk_pu
R85 4.7k 0603 refclk_pd
R86 4.7k 0603 refclk_sel
1=use refclk input
Must Be Left Floating!
R88 4.7k 0603 testclk_pd
REFCLKP
REFCLKN
REFCLKSELECT
XTALP
XTALN
TESTCLOCKIN1
TESTCLOCKIN2
CLOCKDES0P
CLOCKDES0N
CLOCKDES1P
CLOCKDES1N
CLOCKDES2P
CLOCKDES2N
CLOCKDES3P
CLOCKDES3N
CLOCKDES4P
CLOCKDES4N
CLOCKDES5P
CLOCKDES5N
CLOCKDES6P
CLOCKDES6N
CLOCKDES7P
CLOCKDES7N
TESTCLOCKOUT
Port 0 DCFEB Reserved
Phase shiftable CCLK
Disable the clock manager if not used
GBTx Clock Control
Encoding/Bus mode | Transceiver mode | MODE [3:0]
FEC | Simplex TX | 0000
FEC | Simplex RX | 0001
FEC | Transceiver | 0010
FEC | Test | 0011
WideBus | Simplex TX | 0100
WideBus | Simplex RX | 0101
WideBus | Transceiver | 0110
GBTx Control
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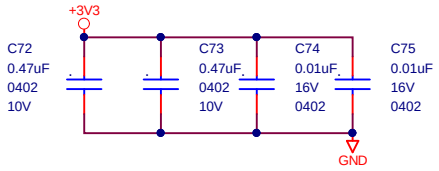
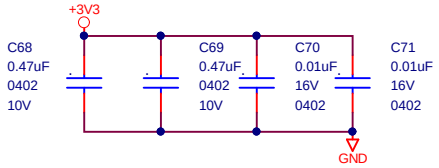
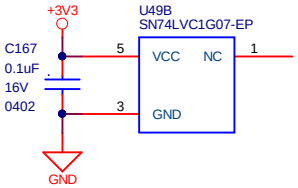
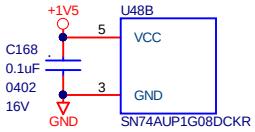


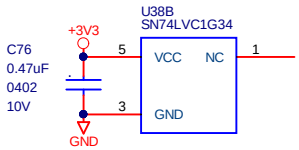
LVDS RECEIVER BYPASSING

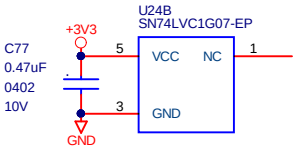


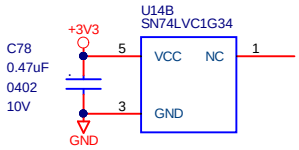
LVDS RECEIVER BYPASSING

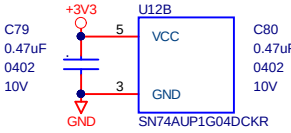


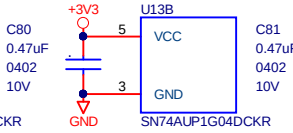


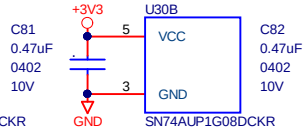


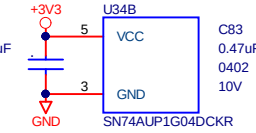


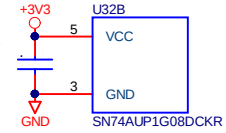


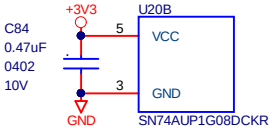


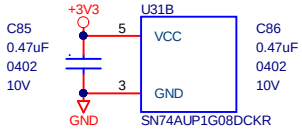


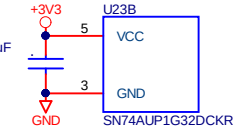


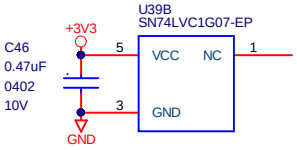












PROMless Power	
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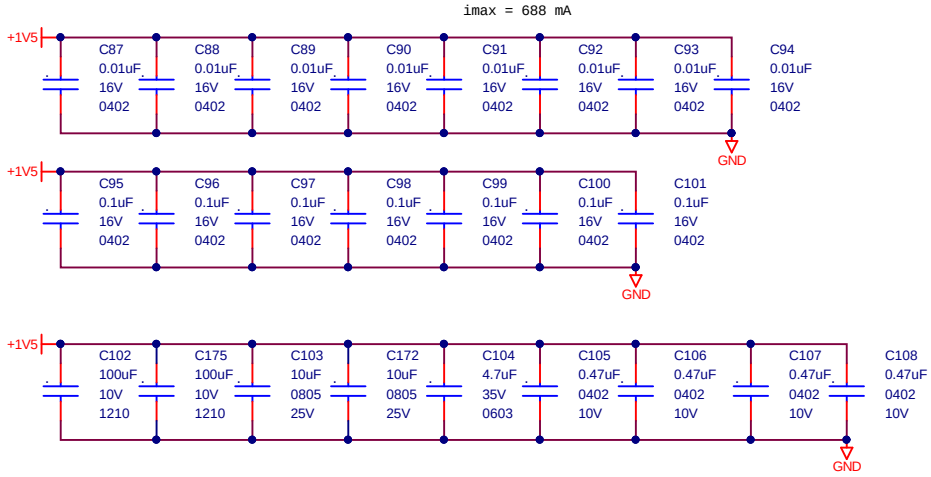
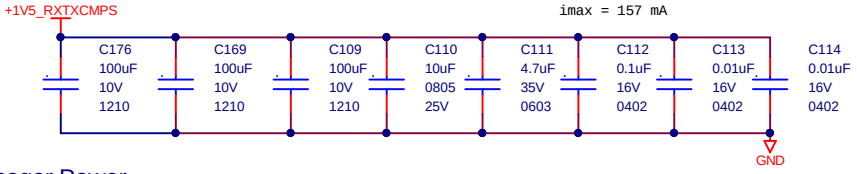
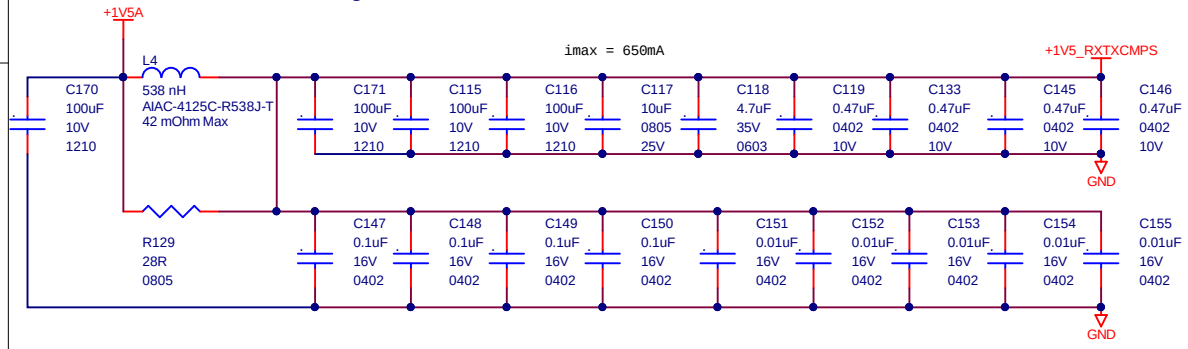
IO & Core Power

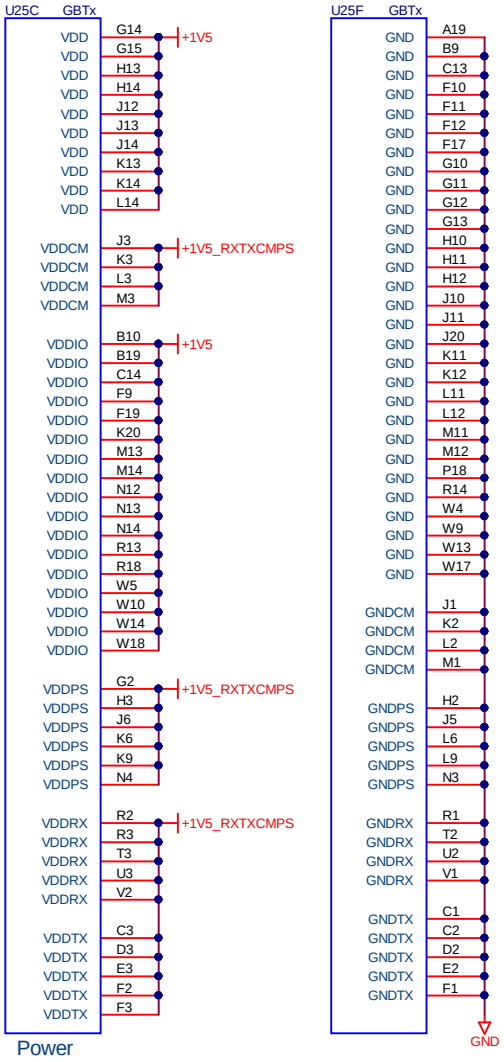


Phase Shifter Power



RX & TX & Clock Manager Power





Power

GBTx Power	
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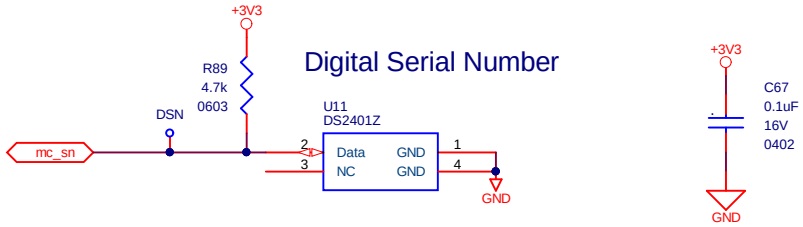

Digital Serial Number	
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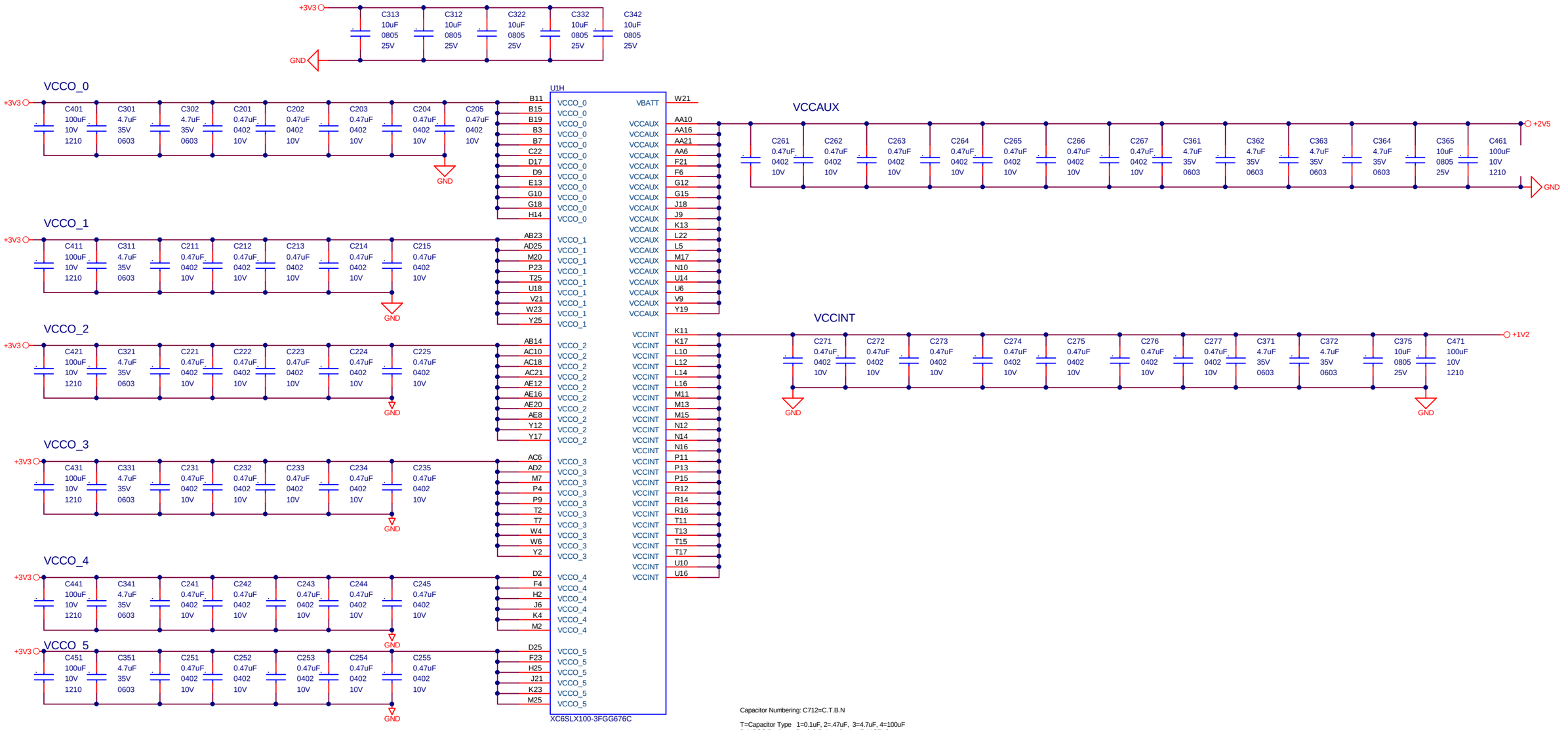

Capacitor Numbering: C712=C.T.B.N

T=Capacitor Type 1=0.1uF, 2=.47uF, 3=4.7uF, 4=100uF
B=VCCO Bank Bank 0-5, Aux=6, Int=7, MGT=8
N=Nth capacitor of type T in bank N

VCCINT		VCCAUX			VCCO 0			VCCO 1			VCCO 2			VCCO 3			VCCO 4			VCCO 4			TOTAL		
Package	Device	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47	100	4.7	0.47			
FG(G)676	LX100	1	2	4	2	3	6	1	1	3	1	1	3	1	1	3	1	1	3	1	1	2	1	1	2	46

Power distribution per Xilinx doc UG393(v1.2) July 15,2010
Table 2-1 for FF(G)900 Spartan-6 device

VBATT = Decryptor key memory backup supply. When key is not used, tie this pin to VCC or GND, or it can be left floating

Placement Rules:
100uF As close to FPGA as possible
4.7uF No more than 3" from periphery of FPGA
0.47uF No more than 1" from periphery of FPGA

FPGA Power

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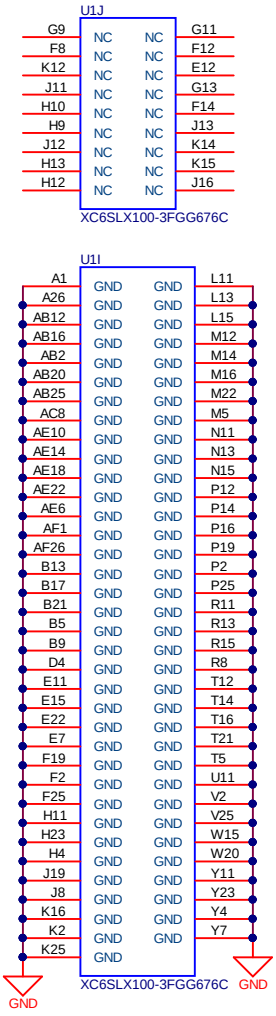

FPGA Ground			
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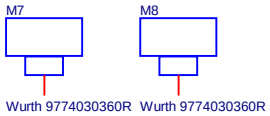
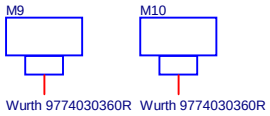
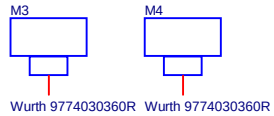
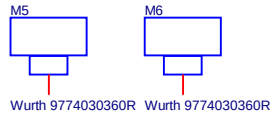
Additional mounts providing for affixing a cover plate to the mezzanine



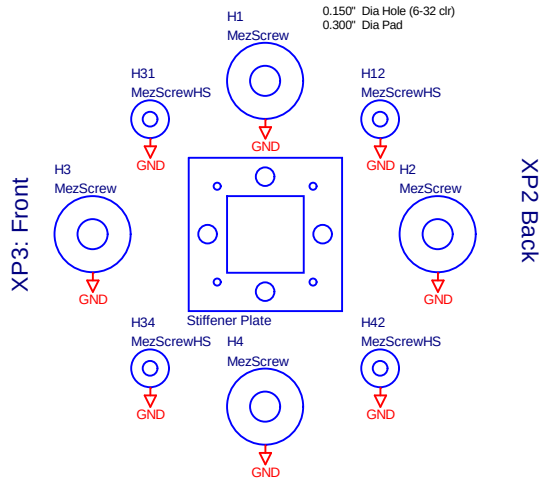


Mounts for HS2069DB heatsink

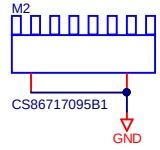




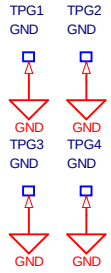
XP1: Top



XP4: Bottom



Test Point Pin GNDs



Assembly Fiducials

Mechanical			
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