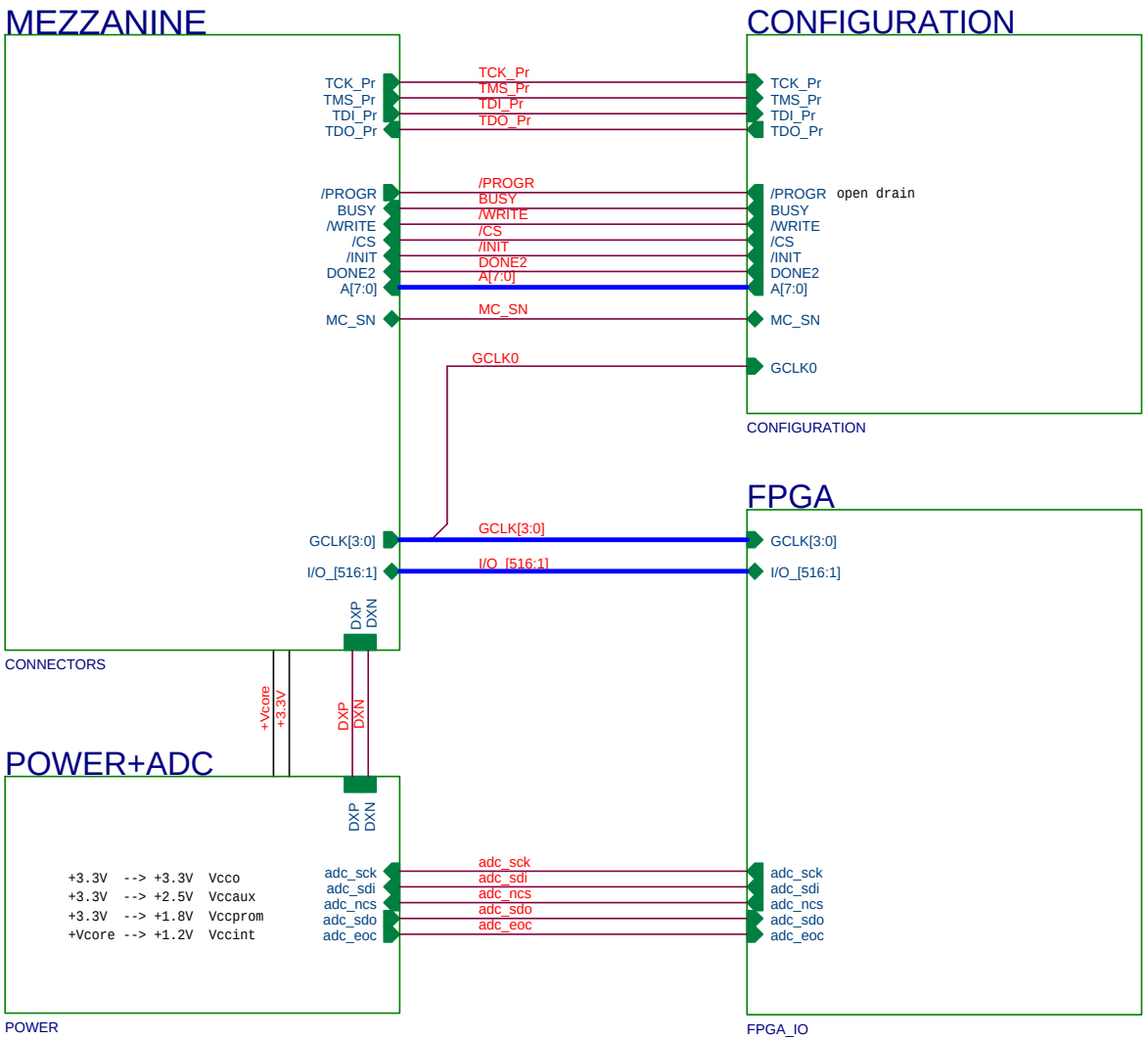
09/24/2012
Rev 1

UCLA Spartan-6 FPGA Mezzanine



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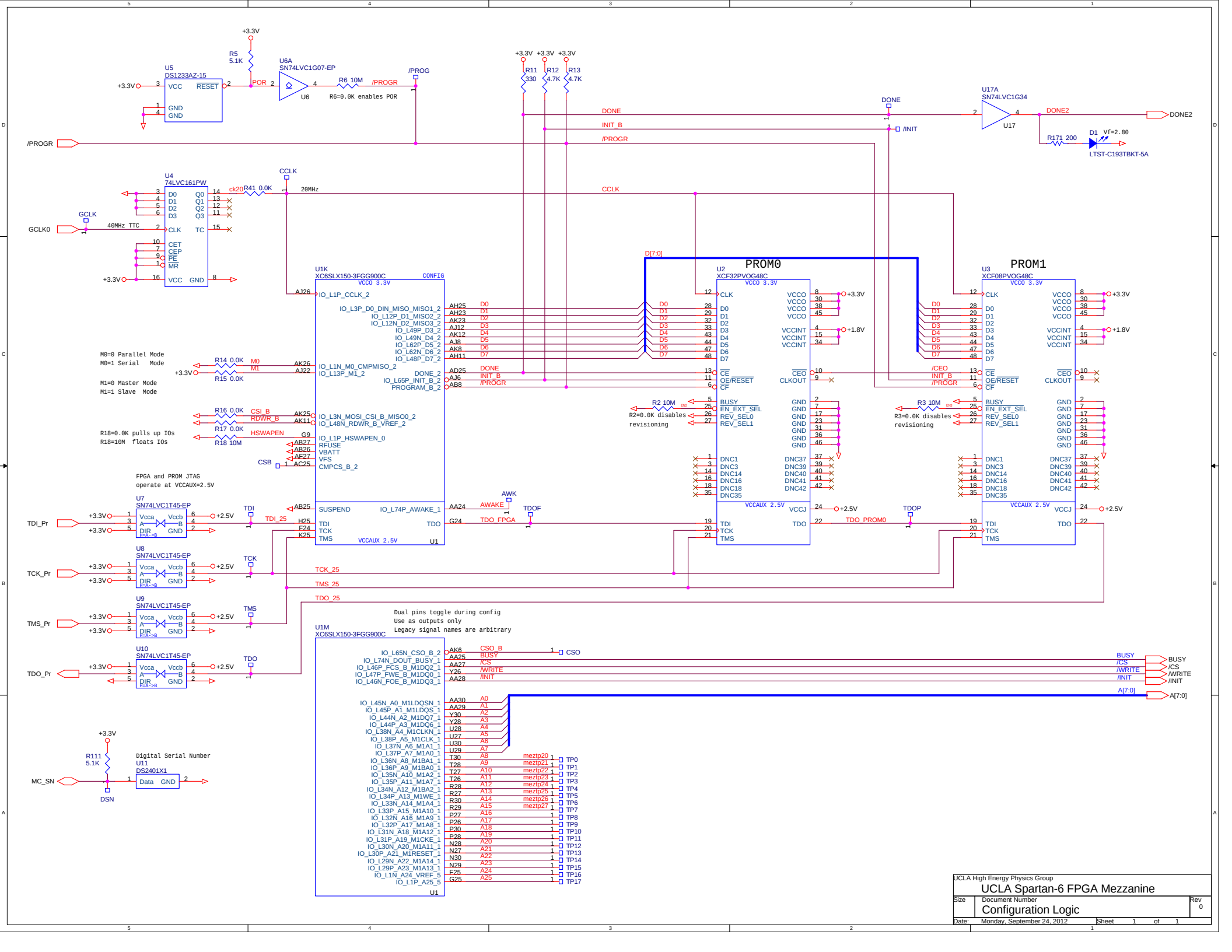
U5
DS1233AZ-15
U6A
SN74LVC1G07-EP
R6=0.0K enables POR
U4
74LVC161PW
U1K
XC6SLX150-3FGG900C
CONFIG
PROM0
XCF32PVOG48C
PROM1
XCF08PVOG48C
R2=0.0K disables revisioning
R3=0.0K disables revisioning
M0=0 Parallel Mode
M0=1 Serial Mode
M1=0 Master Mode
M1=1 Slave Mode
R18=0.0K pulls up IOs
R18=10M floats IOs
FPGA and PROM JTAG
operate at VCCAUX=2.5V
U7
SN74LVC1T45-EP
U8
SN74LVC1T45-EP
U9
SN74LVC1T45-EP
U10
SN74LVC1T45-EP
Dual pins toggle during config
Use as outputs only
Legacy signal names are arbitrary
U1M
XC6SLX150-3FGG900C
Digital Serial Number
U11
DS2401X1
U17A
SN74LVC1G34
U17
LTST-C193TBKT-5A
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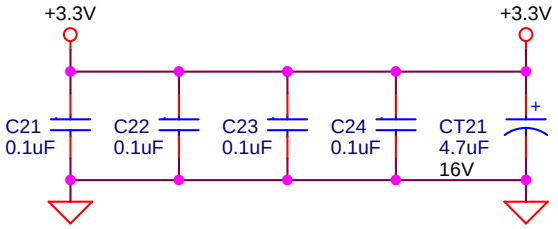
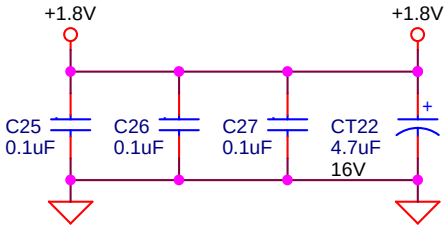
UCLA Spartan-6 FPGA Mezzanine
Configuration Logic
Monday, September 24, 2012

PROM0

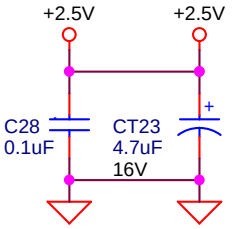
VCC0



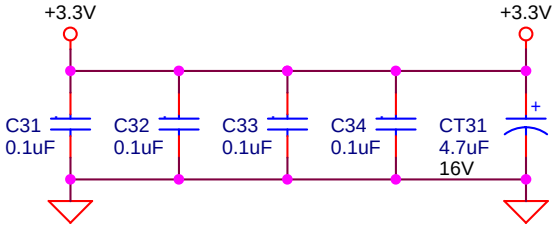
VCCINT

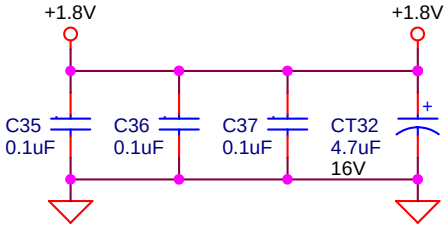


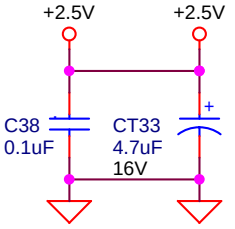
VCCJTAG



PROM1

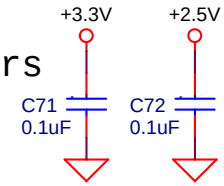


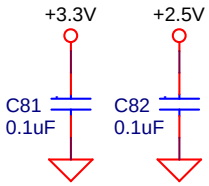


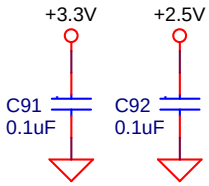


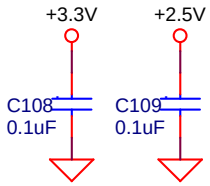
Level Translators

VCC0 VCCAUX

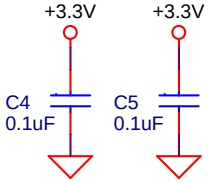


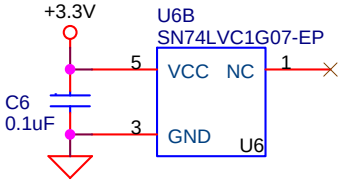


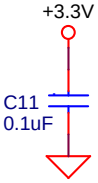


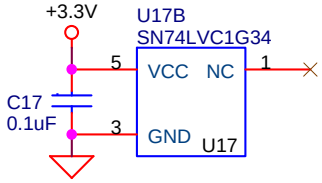


CCLK PROG DSN









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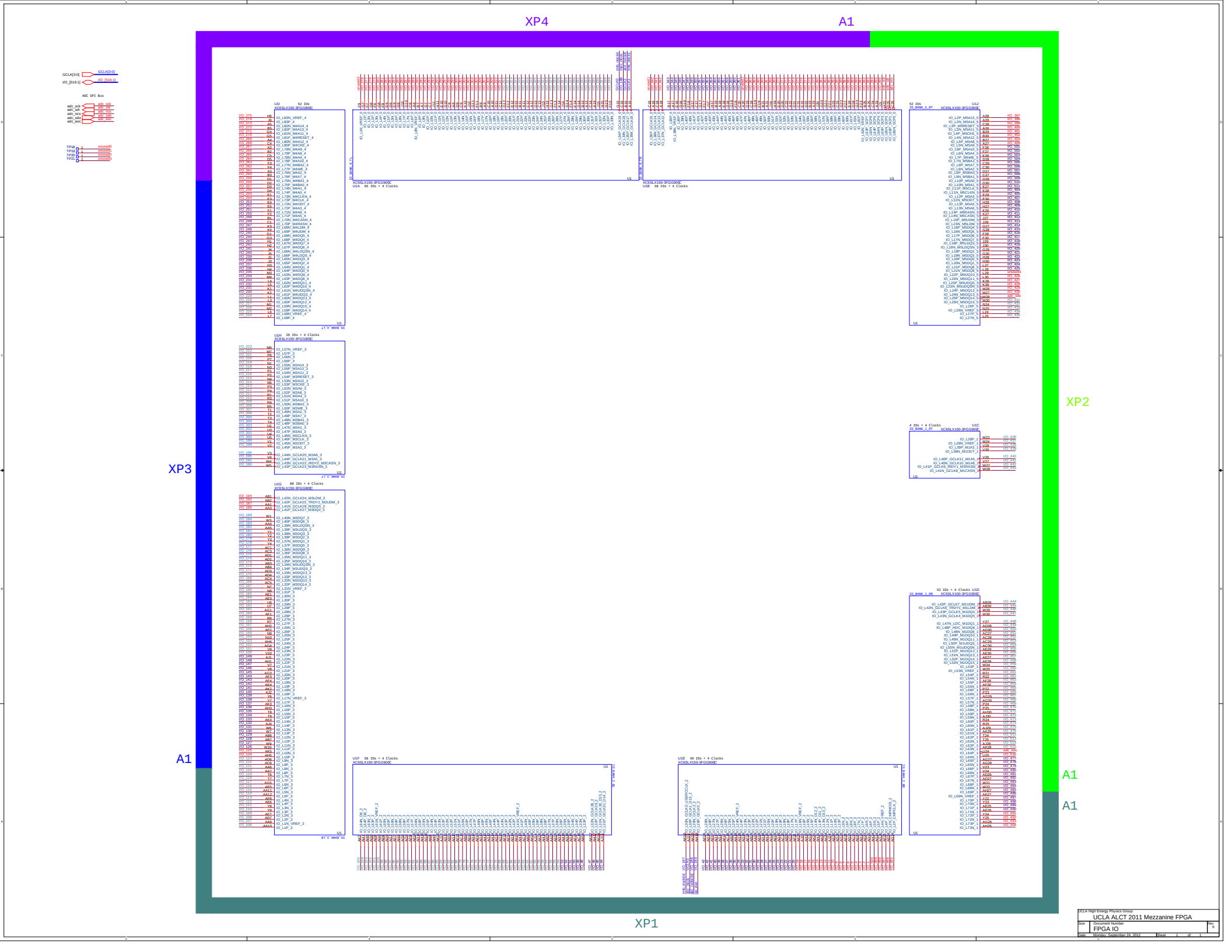
XP4
A1
XP2
XP3
A1
A1
XP1
GCLK[3:0]
I/O_IS16:1]
ADC SPI Bus
adc_sck
adc_sdi
adc_ncs
adc_sdo
adc_sncc
TP1
TP2
TP3
TP4
unused0
unused1
unused2
unused3
U1I
52 IOs
XC6SLX150-3FGG900C
U1H
26 IOs + 4 Clocks
XC6SLX150-3FGG900C
U1G
80 IOs + 4 Clocks
XC6SLX150-3FGG900C
U1F
58 IOs + 4 Clocks
XC6SLX150-3FGG900C
U1E
49 IOs + 4 Clocks
XC6SLX150-3FGG900C
U1A
65 IOs + 4 Clocks
XC6SLX150-3FGG900C
U1B
58 IOs + 4 Clocks
XC6SLX150-3FGG900C
U1J
52 IOs
IO_BANK_5_RT
XC6SLX150-3FGG900C
U1C
4 IOs + 4 Clocks
IO_BANK_1_RT
XC6SLX150-3FGG900C
U1D
53 IOs + 4 Clocks
IO_BANK_1_RB
XC6SLX150-3FGG900C
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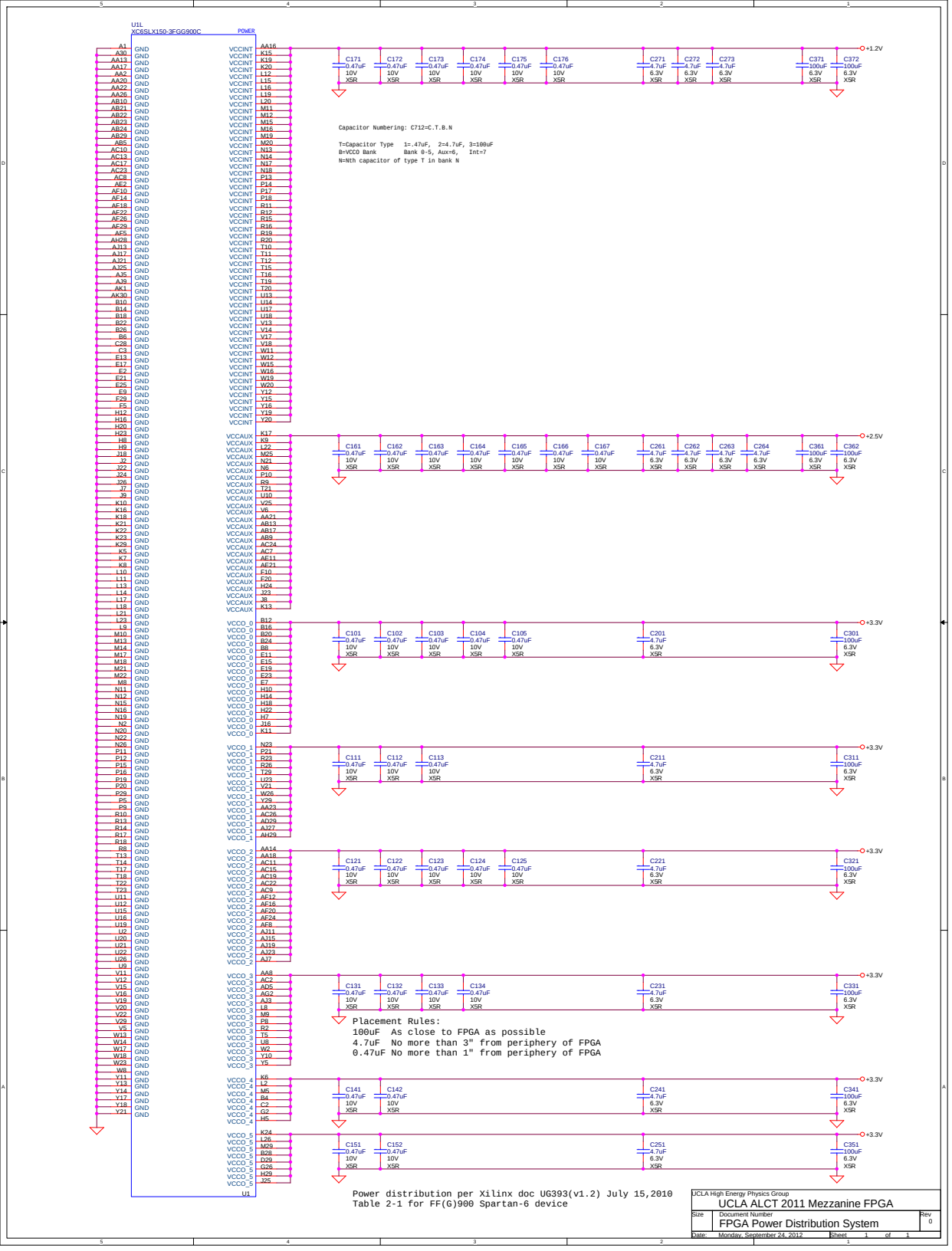
U1L
XC6SLX150-3FGG900C
POWER
GND
VCCINT
VCCAUX
VCCO_0
VCCO_1
VCCO_2
VCCO_3
VCCO_4
VCCO_5
U1
+1.2V
+2.5V
+3.3V
C171 C172 C173 C174 C175 C176 C271 C272 C273 C371 C372
C161 C162 C163 C164 C165 C166 C167 C261 C262 C263 C264 C361 C362
C101 C102 C103 C104 C105 C201 C301
C111 C112 C113 C211 C311
C121 C122 C123 C124 C125 C221 C321
C131 C132 C133 C134 C231 C331
C141 C142 C241 C341
C151 C152 C251 C351
0.47uF 10V X5R
4.7uF 6.3V X5R
100uF 6.3V X5R
Capacitor Numbering: C712=C.T.B.N
T=Capacitor Type 1=.47uF, 2=4.7uF, 3=100uF
B=VCCO Bank Bank 0-5, Aux=6, Int=7
N=Nth capacitor of type T in bank N
Placement Rules:
100uF As close to FPGA as possible
4.7uF No more than 3" from periphery of FPGA
0.47uF No more than 1" from periphery of FPGA
Power distribution per Xilinx doc UG393(v1.2) July 15,2010
Table 2-1 for FF(G)900 Spartan-6 device
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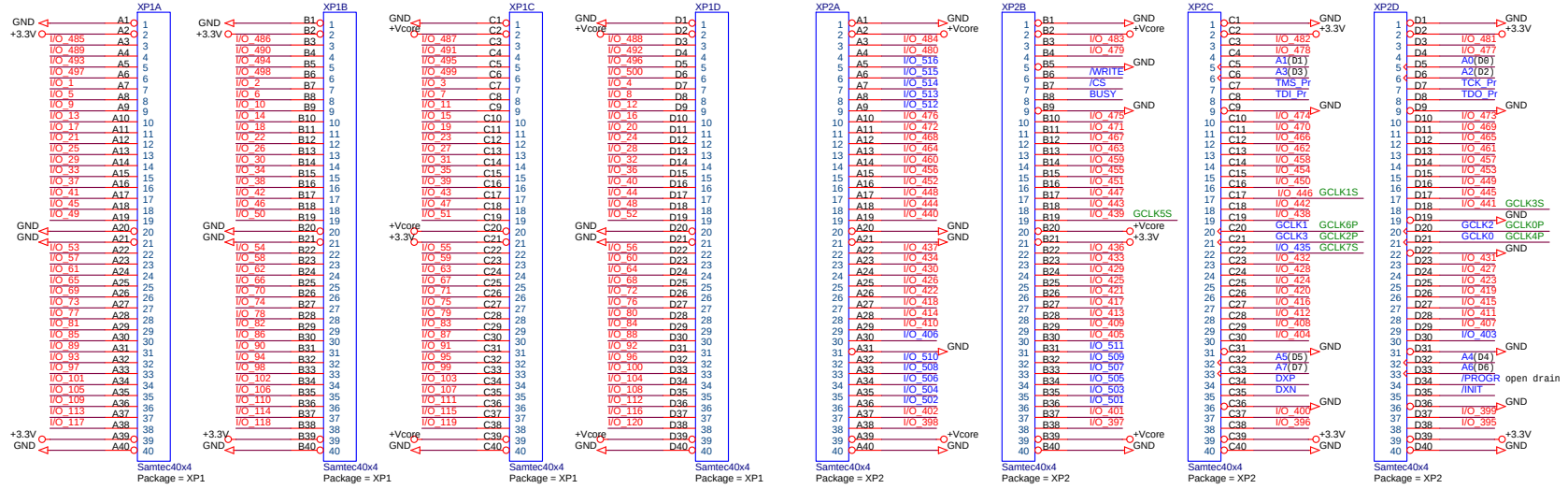

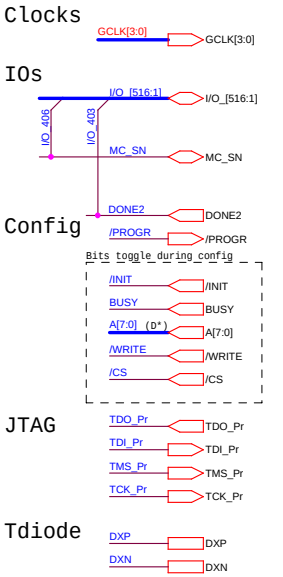

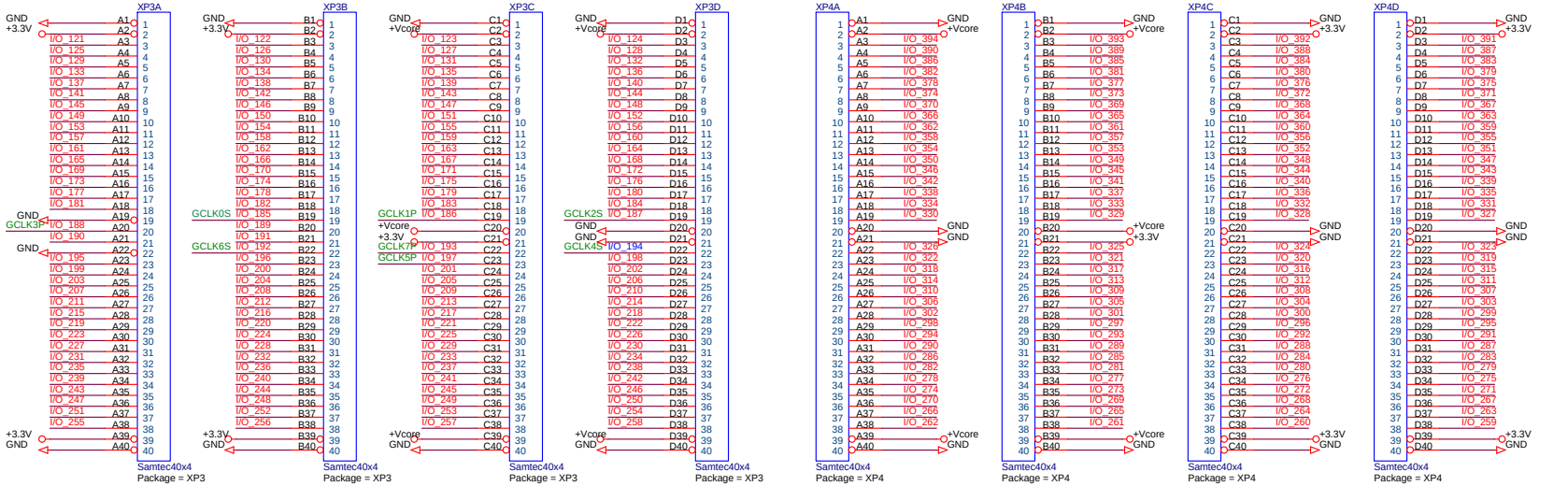

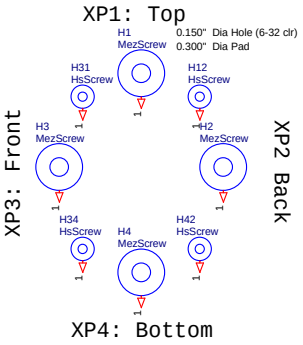

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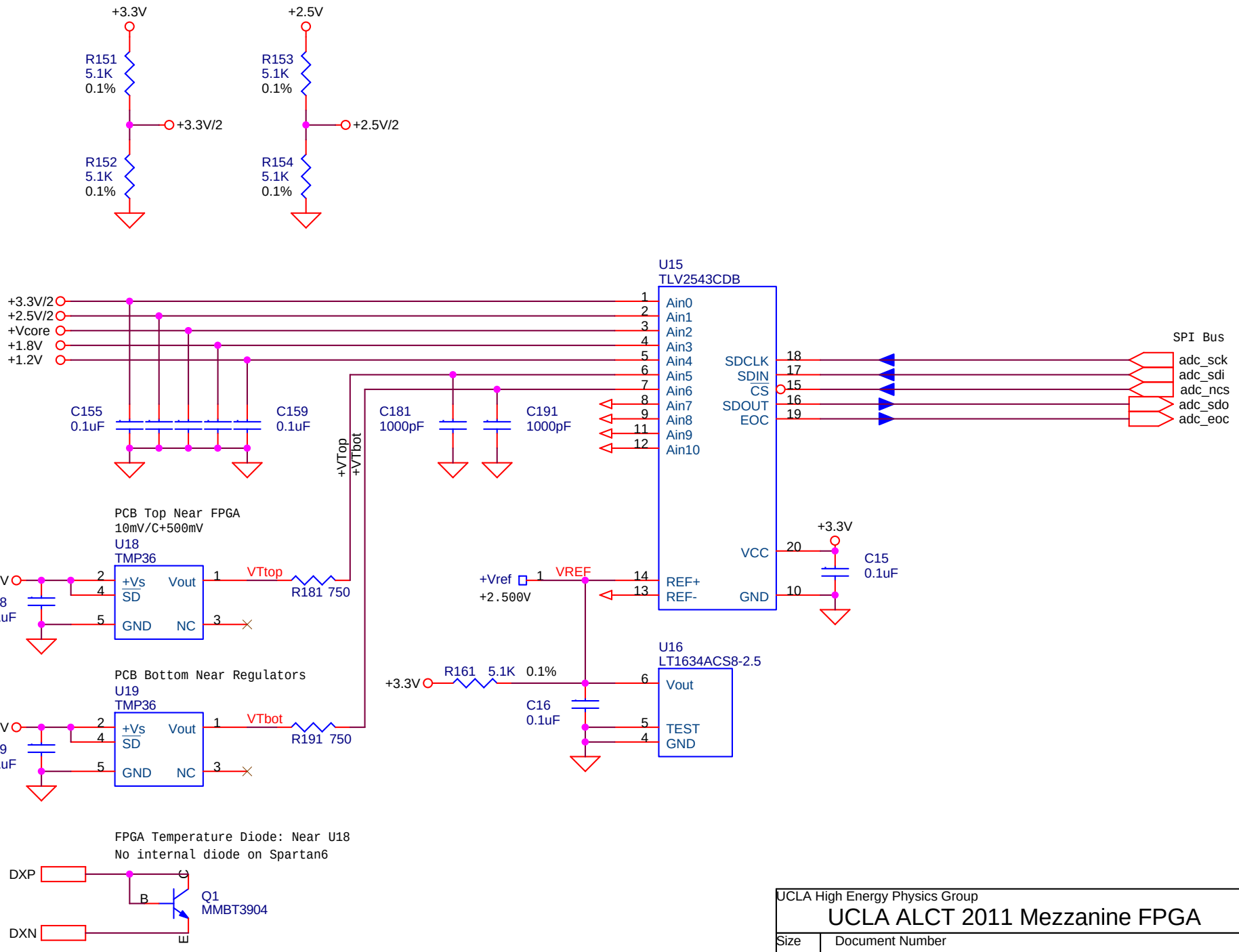

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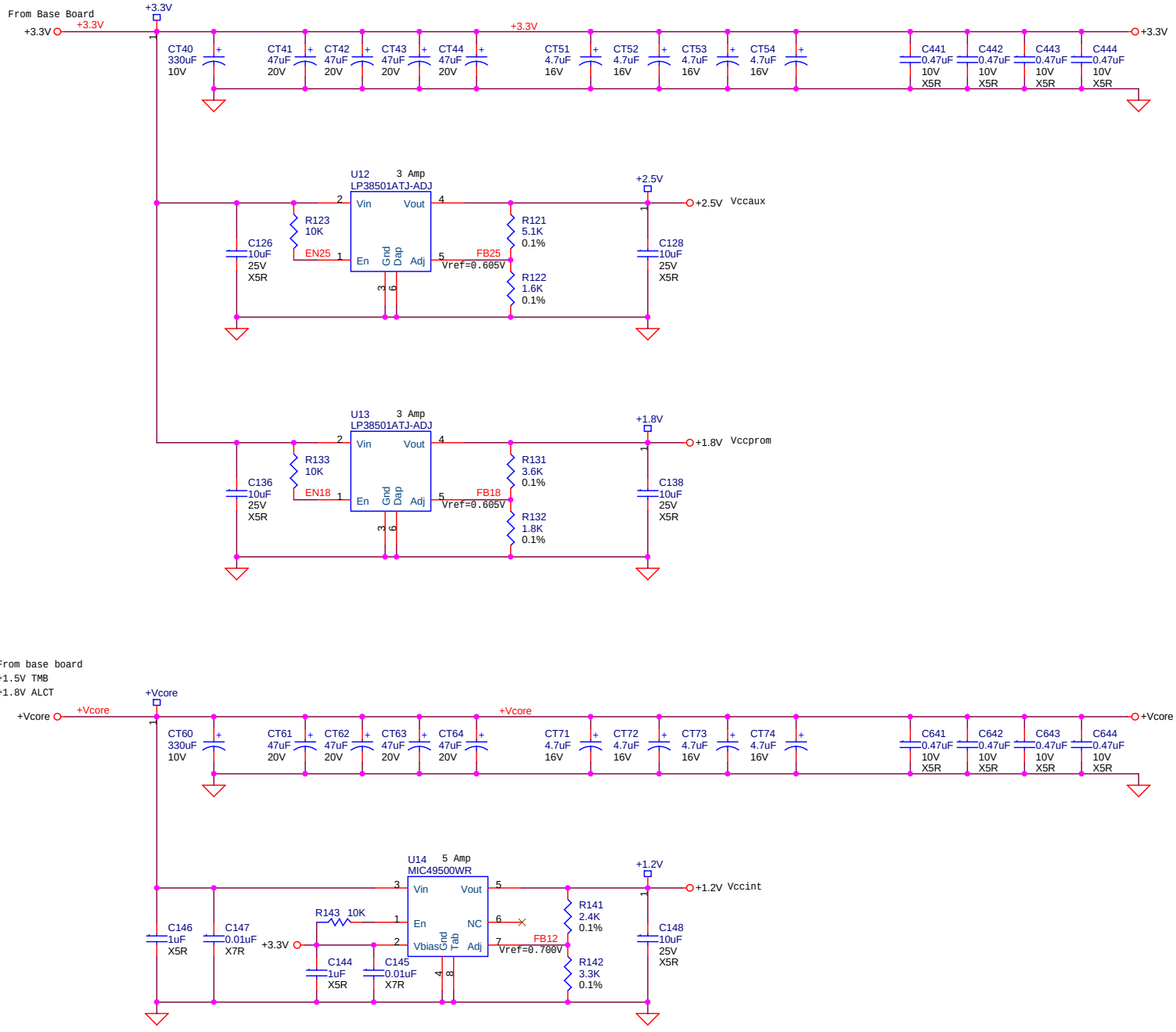

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