Clock Propagation Delays over EMU Peripheral Backplane

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The EMU peripheral backplane [1] is a 21-slot custom 6U backplane that provides communications between Clock and Control Board (CCB), Muon Port Card (MPC), nine Trigger Motherboards (TMB) and nine DAQ Motherboards (DMB) (Figure 1). The main 40.08Mhz system clock is distributed from the CCB to every module over differential point-to-point pairs of equal lengths. Each clock signal can be adjusted individually to each slot using PHOS4 [2] delay ASIC. Four such ASICs reside on a CCB board and can be programmed over VME.

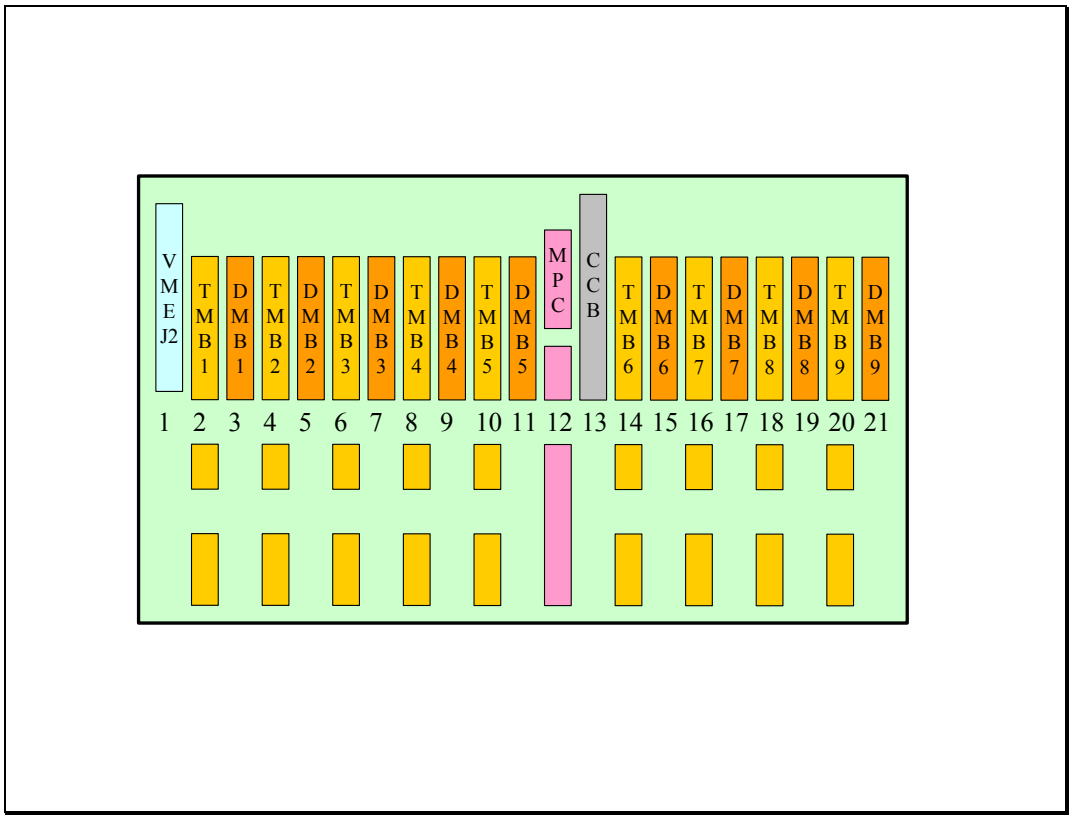

Figure 1: EMU Custom Peripheral Backplane

The goal of our test was to measure the propagation delays of the clock signals arriving from CCB to each slot with and without PHOS4 ASICs installed on a CCB board. When the PHOS4 were installed, all their delay channels were programmed with the same value of delay (0, 5, 10, 15 or 20 ns). A small board with a DS90LV032A LVDS receiver was used at the receiver end. In both cases the delay of the rising edge of clock at the DS90LV032A output in respect to the rising edge of 40.08 MHz clock at the input of the clock buffer (before PHOS4 chips) at the CCB was measured. The clock source was a

CCB on-board quartz oscillator (80.16 MHz divided by 2). The results are shown in Table 1.

Table 1

PHOS4 preprogrammed delay, ns	0	5	10	15	20	No PHOS4
TMB1 (slot 2)	-6.6	-1.7	3.7	8.7	13.6	11.8
DMB1 (slot 3)	-6.7	-1.8	3.8	8.6	13.7	11.9
TMB2 (slot 4)	-6.8	-2.0	3.1	8.3	13.2	11.8
DMB2 (slot 5)	-5.8	-1.2	4.2	9.2	14.2	11.9
TMB3 (slot 6)	-6.5	-1.5	4.0	9.1	14.0	11.9
DMB3 (slot 7)	-7.0	-2.1	3.5	9.0	13.5	11.8
TMB4 (slot 8)	-7.0	-2.0	3.3	8.2	13.2	11.8
DMB4 (slot 9)	-6.1	-1.2	4.0	9.1	14.0	12.0
TMB5 (slot 10)	-5.8	-1.1	4.2	9.3	14.3	11.8
DMB5 (slot 11)	-7.0	-2.0	3.1	8.0	13.2	11.8
MPC (slot 12)	-5.7	-1.3	4.2	9.2	14.0	11.8
TMB6 (slot 14)	-6.8	-1.5	3.5	8.1	13.7	11.9
DMB6 (slot 15)	-6.9	-2.0	3.4	8.3	14.0	12.0
TMB7 (slot 16)	-6.5	-1.7	3.8	8.2	14.0	11.9
DMB7 (slot 17)	-7.0	-2.1	3.2	8.0	13.2	11.9
TMB8 (slot 18)	-6.0	-1.3	4.0	8.9	14.0	12.0
DMB8 (slot 19)	-6.8	-1.9	3.7	8.3	14.0	12.0
TMB9 (slot 20)	-6.2	-1.7	4.0	8.8	13.9	11.8
DMB9 (slot 21)	-6.4	-1.8	3.8	8.1	13.3	11.8
Average delay, ns	-6.5 (+0.8/-0.5)	-1.7 (+0.5/-0.5)	3.7 (+0.5/-0.6)	8.6 (+0.6/-0.6)	13.7 (+0.5/-0.5)	11.9 (+0.1/-0.1)
Δdelay max, ns	1.3	1.0	1.1	1.2	1.0	0.2

As one can see from the last row of Table 1, in the presence of PHOS4 delay ASICs on a CCB board the dispersion of the clock propagation delay from slot to slot can be as high as 1.3 ns. When all PHOS4 were removed from their sockets, and clock inputs wired directly to respective outputs, the delay dispersion decreased to 0.2 ns.

Conclusion

As our measurements show, while PHOS4 ASICs provide an adjustable clock delays from the CCB to each slot in the EMU crate individually, the dispersion of clock delays from slot to slot depends on PHOS4 preprogrammed settings and can be as high as 1.3 ns. In order to get lower dispersion an individual clock adjustments (unique for each CCB) would be required. In case of absence of PHOS4 ASICs the dispersion decreases to 0.2 ns, but the clock delays cannot be adjusted from slot to slot.

References

[1]. http://www.phys.ufl.edu/~madorsky/backplane/
[2]. http://lhcb-elec.web.cern.ch/lhcb-elec/meetings/lhcbweek_february00/delaychip22022000.pdf