# Prototype Clock and Control Board for the CSC Sector Processor Crates

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This document specifies the prototype Clock and Control Board (CCB) for the CMS Endcap Muon electronics residing in the Sector Processor (SP) crates in the counting room. The standard set of modules in each crate consists of two SP and six Sector Receivers (SR). The general block diagram of the CCB is shown on Fig.1.

## 1. TTC Interface

The TTC interface is based on the TTCrx chip [1]. The prototype CCB includes connectors for the TTCrx mezzanine board.

The general sequence of L1ACC, Reset and BX0 commands is described in [2]. Particularly, for the Reset sequence, the TTC sends a broadcast command (either system, or user) to the TTCrx indicating that the next L1ACC has to be treated as a Reset. After this data is sent, a single L1ACC is generated. CCB decoding logic recognizes this command and treats the next incoming L1ACC as a RESET signal. After some predetermined interval the next broadcast command is transmitted over the TTC indicating that the next L1ACC should be treated as Bunch Crossing 0. In a similar fashion, CCB recognizes this command and treats the next L1ACC as a BX0. After that CCB internal logic enables generation of L1A to backplane upon every L1ACC from TTC system.

We use only one option when BrcstStr2 and Brcst<7:6> are synchronized to Clock40Des1. We do not use an option when BrcstStr2 and Brcst<7:6> are synchronized to Clock40Des2

The TTCrx chip can be programmed using an I2C interface and interface controller PCF8584 over VME (see Fig.2). This controller is located on CCB board as well.

## 2. External Inputs, Outputs and Front Panel LEDs

The following external inputs will be provided on the front panel:

- CLOCK (NIM and ECL)
- EXTERNAL TRIGGER (EXT) (NIM and ECL)
- RESET (NIM and ECL)
- BX0 (NIM and ECL)
- Two RESERVED (RSV1 and RSV2), (NIM and ECL)

Three non-TTC clock options are possible: external NIM clock, external ECL clock, and clock generated by on-board quartz oscillator. The CSR<0..2> bits are responsible for the clock selection. An EXT trigger pulse causes generation of the 25 ns long L1ACC signal which is synchronized with the selected by VME clock source. Input RESET, BX0, RSV1 and RSV2 signals will cause generation of the RES, BX0, RSV1 and RSV2 signals 25 ns long each on the custom backplane, also synchronized with the selected clock.

The following NIM outputs are provided on the front panel:

- CLOCK
- RESET
- BX0
- L1ACC
- RSV1
- RSV2

A 16-pin connector will provide all differential ECL connections on the front panel. All NIM connections are provided using LEMO connectors. 10-pin header is intended for JTAG connection to Altera Byte (or Bit-) Blaster.

The following LEDs (with one-shots) are provided on the front panel:
- DTACK (access to CCB over VME)
- JTAG (access to PLD over JTAG)
- CLOCK (output to backplane)
- BX0 (output to backplane)
- RESET (output to backplane)
- L1ACC (output to backplane)
- EXTERNAL TRIGGER (on any external trigger source)
- +3.3V, +5V, -5.2V (no one-shots)

## 3. Clock adjustments and settings

There are fine and coarse delays for clock and command signals incorporated on the TTCrx chip [1]. We use the TTCrx Clock40Des1 deskewed signal as the main clock signal from the TTCrx board. Three other possible clock sources are ECL and NIM clocks from external connectors on the front panel, and clock from quartz oscillator.

One of four clock sources listed above can be chosen using CSR<0..2> bits (see Table 4). The selected signal acts as a main master clock for the CCB internal logic. The phase of the clock signal provided to synchronization logic, can be adjusted with 2 ns step accuracy with respect to the main master clock. CSR4<0..3> bits are used for the fine tuning. That means that the phase of L1ACC, BX0, RESET, RSV1 and RSV2 signals distributed to all slots in crate can be adjusted with 2 ns accuracy in respect to the main CCB master clock (Fig.2).

The selected clock is distributed to the SP and SR modules in the crate via its custom backplane. The phase of each of eight clock signals distributed over this backplane can be adjusted with 2 ns step accuracy with respect to the main master clock individually to each slot in crate using CSR2…CSR3 (see Table 4 and Fig.2).

There is also the possibility to send just a single 25 ns clock pulse to all modules in crate upon special VME command (see Tables 3 and 4). Two other VME commands (Table 3) allow user to set all backplane clock drivers either in "1" or "0" state. This option can be useful for debugging purposes.

## 4. Backplane Interface

The prototype CCB is located in the middle of the crate on station 13 for the final system, and on slot 14 for the summer'2000 tests. Point-to-point connections for communication between the CCB and the SP and SR modules are based on the National DS90LV031/032 chipset. Two reserved signals RSV1 and RSV2 are intended for possible use in the future. Pin assignment for the 125-pin connector (AMP 100141-1 for the backplane, AMP 100624-1 for the plugged boards) is shown in Table 1.

Table 1

| CCB Pinout | | | | | | |
|---|---|---|---|---|---|---|
| | Row a | Row b | Row c | Row d | Row e | |
| 1 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Receiver SR4, very left |
| 2 | CLK- | CLK+ | GND | BX+ | BX- | |
| 3 | RST- | RST+ | GND | L1+ | L1- | |
| 4 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Receiver SR4, very right |
| 5 | CLK- | CLK+ | GND | BX+ | BX- | |
| 6 | RST- | RST+ | GND | L1+ | L1- | |
| 7 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Receiver SR1, left |
| 8 | CLK- | CLK+ | GND | BX+ | BX- | |
| 9 | RST- | RST+ | GND | L1+ | L1- | |
| 10 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Receiver SR1, right |
| 11 | CLK- | CLK+ | GND | BX+ | BX- | |
| 12 | RST- | RST+ | GND | L1+ | L1- | |
| 13 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Processor, left |
| 14 | CLK- | CLK+ | GND | BX+ | BX- | |
| 15 | RST- | RST+ | GND | L1+ | L1- | |
| 16 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Processor, right |
| 17 | CLK- | CLK+ | GND | BX+ | BX- | |
| 18 | RST- | RST+ | GND | L1+ | L1- | |
| 19 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Receiver SR2,3, left |
| 20 | CLK- | CLK+ | GND | BX+ | BX- | |
| 21 | RST- | RST+ | GND | L1+ | L1- | |
| 22 | RSV1- | RSV1+ | GND | RSV2+ | RSV2- | Sector Receiver SR2,3, right |

| | | | | | | |
|---|---|---|---|---|---|---|
| 23 | CLK- | CLK+ | GND | BX+ | BX- | |
| 24 | RST- | RST+ | GND | L1+ | L1- | |
| 25 | N/C | N/C | GND | N/C | N/C | |

## 5. VME Interface

CCB can be addressed in the VME crate using either geographical or logical A24D16 addressing. An on-board DIP switch is used for mode selection. Geographical mode utilizes the geographical address lines GA<4-0> available on VME64x backplane. In this mode CCB recognizes its address space when the code on address lines A<23-19> is equal to the 5-bit geographical address of the slot in crate where it is located.

The CCB performs A24D16 VME Slave Function. Base Address is selectable using DIP Switches S3 (bits A8…A15) and S7 (bits A16..A23). If switch is in "On" state, the bit is "0". If switch is in "Off" state, the bit is "1" (see Table 2). During CCB initial testing and debugging base address C00000(hex) and logical address mode are used. Decoded addresses and VME commands are listed in Table 3.

Table 2

| Switch S6 | | Switch S3 | | Switch S7 | |
|---|---|---|---|---|---|
| 1-4 on, 2-3 off | Geogr. Addr. | 1-16 on | A8=0 | 1-16 on | A16=0 |
| 1-4 off, 2-3 on | Logical Addr. | 2-15 on | A9=0 | 2-15 on | A17=0 |
| 1-4 on, 2-3 on | Prohibited | 3-14 on | A10=0 | 3-14 on | A18=0 |
| 1-4 off, 2-3 off | Prohibited | 4-13 on | A11=0 | 4-13 on | A19=0 |
| | | 5-12 on | A12=0 | 5-12 on | A20=0 |
| | | 6-11 on | A13=0 | 6-11 on | A21=0 |
| | | 7-10 on | A14=0 | 7-10 on | A22=0 |
| | | 8-9 on | A15=0 | 8-9 on | A23=0 |

Table 3

| Address (hex) | Access | Register |
|---|---|---|
| Base + 0 | Write | Generate L1ACC (1) |
| Base + 2 | Write | Generate RESET (1) |
| Base + 4 | Write | Generate BX0 (1) |
| Base + 6 | Write | Generate RSV1 (1) |
| Base + 8 | Write | Generate RSV2 (1) |
| Base + a | Write | Generate reset to CCB internal logic |
| Base + c | Write/Read | Access to PCF8584 I2C controller |
| Base + e | Write/Read | Access to PCF8584 I2C controller |
| Base + 10 | Write | Reset PCF8584 I2C controller |
| Base + 12 | Write | Reset TTCrx chip |
| Base + 14 | | Reserved |
| Base + 16 | | Reserved |
| Base +18 | | Reserved |
| Base + 1a | | Reserved |
| Base + 1c | | Reserved |

| | | |
|---|---|---|
| Base + 1e | | Reserved |
| Base + 20 | Write | Send 25 ns pulse to backplane drivers (2) |
| Base + 22 | Write | Set Clock line to backplane drivers in “1” state (2) |
| Base + 24 | Write | Set Clock line to backplane drivers in “0” state (2) |
| Base + 26 | Write/Read | CSR1 |
| Base + 28 | Write/Read | CSR2 |
| Base + 2a | Write/Read | CSR3 |
| Base + 2c | Write/Read | CSR4 |
| Base + 2e | Write/Read | CSR5 |
| Base + 30 | | Reserved |

(1) 25 ns long pulse to backplane drivers will be generated upon these commands. Each of these signals is synchronized with the selected clock.

(2) See CSR1<0-2> bit assignment in Table 3.

## 6. Control and Status Registers (CSR)

Bit assignment of the CSR<1-4> is shown in Tables 4-7.

Table 4

CSR1

| Bit | Function |
|---|---|
| 0-2 | **Source of 40MHz clock to backplane drivers**<br>Bit 2 Bit 1 Bit 0<br>0 0 0 Continuous clock from on-board quartz oscillator<br>0 0 1 Continuous Clock40Des1 from TTCrx mezzanine board<br>0 1 0 Continuous clock from the front panel NIM input<br>0 1 1 Continuous clock from the front panel ECL input<br>1 0 0 25 ns clock pulse generated upon VME command<br>1 0 1 Set Clock line to backplane drivers in “1” or “0” state<br>1 1 0 Not used<br>1 1 1 Not used |
| 3-4 | **Source of BC0, RESET, L1ACC, RSV1 and RSV2 signals to backplane**<br>**Bit 4 Bit 3**<br>**0 0 from NIM inputs**<br>**0 1 from ECL inputs**<br>**1 0 from TTCrx**<br>**1 1 from VME** |
| 5 | Reserved |
| 6 | Reserved |
| 7 | Reserved |
| 8-15 | Reserved |

Table 5

CSR2

| Bit | Function |
|---|---|
| 0-3 | Fine delay of the clock signals to SR4 (left), step 2 ns (bit 0 is LSB) |

| | |
|---|---|
| 4-7 | Fine delay of the clock signals to SR4 (right) , step 2 ns (bit 4 is LSB) |
| 8-11 | Fine delay of the clock signals to SR1 (left) , step 2 ns (bit 8 is LSB) |
| 12-15 | Fine delay of the clock signals to SR1 (right) , step 2 ns (bit 12 is LSB) |

Table 6

CSR3

| Bit | Function |
|---|---|
| 0-3 | Fine delay of the clock signals to SP (left) , step 2 ns (bit 0 is LSB) |
| 4-7 | Fine delay of the clock signals to SP (right) , step 2 ns (bit 4 is LSB) |
| 8-11 | Fine delay of the clock signals to SR2,3 (left) , step 2 ns (bit 8 is LSB) |
| 12-15 | Fine delay of the clock signals to SR2,3 (right) , step 2 ns (bit 12 is LSB) |

Table 7

CSR4

| Bit | Function |
|---|---|
| 0-3 | Fine delay of the source clock signal to CCB synchronization logic, step 2 ns (bit 0 is LSB) |
| 4-15 | Reserved |

## 6. JTAG Access

Either PLD (EPF10K50VRC240) or PROM (EPC2) can be accessed from Altera Byte/Bit Blaster cable for downloading (PLD) or programming (PROM). Switches S1 and S2 select one of these chips in a JTAG chain (see Table 8).

Table 8

| Switch S1 | Switch S2 | Device in JTAG chain |
|---|---|---|
| 1-4 off, 2-3 on | 1-4 off 2-3 on | PLD (EPF10K50VRC240) |
| 1-4 on, 2-3 off | 1-4 on, 2-3 off | PROM (EPC2) |
| Other combinations | Other combinations | Prohibited |

## References

[1]. TTCrx Reference Manual October 1999. Version 3.0. Available at: http://www.cern.ch/TTC/intro.html
[2]. W.H.Smith. CMS Synchronization Workshop Conclusions. Version 0.3. http://cmsdoc.cern.ch/~wsmith/synch_concl.pdf

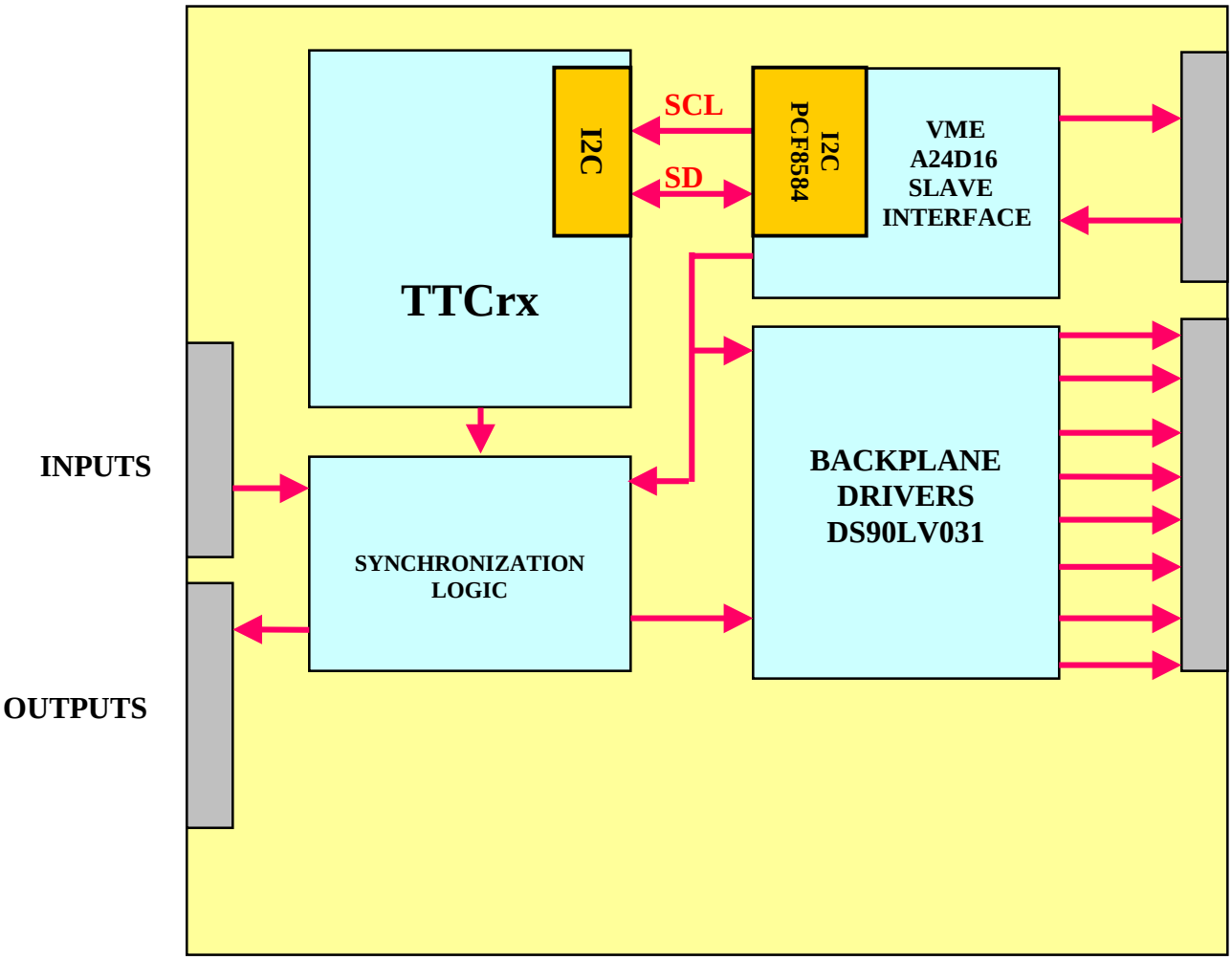


**Fig.1. CCB Block Diagram**

**Fig. 2. Signal Distribution to Backplane**