VME 9U MUON CLOCK AND CONTROL BOARD

'99 Prototype User's Manual

Version 2.1

08/15/2000

Abstract

This document describes the functionality of the 9U Muon Clock and Control Board (CCB) Prototype for the CMS Cathode Strip Chamber (CSC) peripheral electronics and its communication with other modules of the Trigger/DAQ system. The board comprises a TTCrx [1] mezzanine card that acts as an interface to Timing, Trigger and Control (TTC) system of the whole experiment.

1. TTC Signals for Trigger Electronics

Four signals are needed for trigger electronics in order to perform all the main synchronization and reset procedures. These signals are listed in Table 1. They can be either extracted from the TTCrx board or generated inside CCB when the TTC system is not available (in particular, during '99 beam test or for testing purposes). The sources of these signals in "TTC Simulator" mode are also listed in Table 1.

Table 1

Signal	TTC System	TTC Simulator
40 MHz clock	Clock40Des1	40MHz Quartz Oscillator
L1ACC	L1ACC	Trigger (*)
BX0	BX0	VME Command
RESET	RESET	VME Command

* - The source of Trigger signal distributed to all modules is a PRT input connector on the front panel. The CCB synchronizes a Trigger input with its own 40MHz clock. Before distribution to other module this 25 ns signal can be delayed for up to 255 clock periods (6.4 us total). Since the internal logic delay is ~4 clock periods, the total delay will be 100 + n*25 ns, where (n) is a programmable value defined by CSR2.

The "PRT" output on the front panel is a 100 ns pulse originating from one of four sources: TR1 (front panel), TR2 (front panel), delayed PRT input (front panel) or VME command. CSR1[2..1] bits are responsible for source selection.

2. Electrical Interface

The CCB distributes four signals to each trigger/DAQ module over individual cables. Pin assignment of the 20-pin header (3M 80610565154, Digikey part number MHB20K-ND) is given in Table 2. National DS90LV031/32 chipset is used.

Table 2

Contact	Signal	Contact	Signal
1	GND	2	GND
3	CLOCK+	4	CLOCK-
5	GND	6	GND
7	BX0+	8	BX0-
9	GND	10	GND
11	RESET+	12	RESET-
13	GND	14	GND
15	L1ACC+	16	L1ACC-
17	GND	18	GND
19	GND	20	GND

3. Control and Status Registers (CSR)

Data formats of the CSR1 and CSR2 are given in Tables 3 and 4 respectively.

Table 3

CSR1 bit	Function
0	TTC Simulator (if "0") or TTCrx (if "1") source of CLOCK, L1A, BX0, RES signals distributed to all modules in crate
1	Source of PRT output when TTC Simulator (*)
2	Source of PRT output when TTC Simulator (*)
3-15	Not used

(*) Bit 2 Bit 1

0	0	TR1 is a source
0	1	TR2 is a source
1	0	PRT is a source
1	1	VME write command is a source

Table 4

CSR2 bit	Function
7-0	Delay of the PRT input pulse; 0-255 clock cycles
15-8	Not used

4. VME Interface

The CCB performs A24D16 VME Slave functions. Base address is selectable using on-board DIP switches (Table 5). Decoded VME addresses are listed in Table 6. The Base address during testing is C00000(hex).

Table 5

Switch S4		Switch S5	
1-16 on	A8=0	1-16 on	A16=0
2-15 on	A9=0	2-15 on	A17=0

3-14 on	A10=0	3-14 on	A18=0
4-13 on	A11=0	4-13 on	A19=0
5-12 on	A12=0	5-12 on	A20=0
6-11 on	A13=0	6-11 on	A21=0
7-10 on	A14=0	7-10 on	A22=0
8-9 on	A15=0	8-9 on	A23=0

Table 6

Address (hex)	Access	Register
Base + 0	Write	Generate Trigger
Base + 2	Write	Generate Reset
Base + 4	Write	Generate BX0
Base + 6	Read/Write	CSR1
Base + 8	Read/Write	CSR2
Base + a	Write	Reset internal logic
Base + c	Read/Write	I2C controller PCF8584 (for TTCrx access)
Base + e	Read/Write	I2C controller PCF8584 (for TTCrx access)
Base + 10	Write	Reset I2C controller PCF8584

5. JTAG Chain

The content of the PLD (Altera EPF10K50) or EPROM (EPC2) can be downloaded over Altera Bit- or ByteBlaster cable (Table 7).

Table 7

Switch S1	Switch S2	Switch S3	Device in JTAG chain
1-4 off 2-3 on	1-4 on 2-3 off	1-4 on 2-3 off	EPC2
1-4 on 2-3 off	1-4 off 2-3 off	1-4 off 2-3 on	PLD
Other combinations			Prohibited

6. Front Panel

There are on the front panel:

LEMO connectors:

- TR1 (Input, NIM)
- TR2 (Input, NIM)
- PRT (Input, NIM)
- CLK (Output, NIM)
- BX0 (Output, NIM)
- RES (Output, NIM)
- L1A (Output, NIM)
- PRT (Output, NIM)
- RESERVED (NIM); 3 inputs and 3 outputs

- 10-pin JTAG header for Altera Bit- or ByteBlaster cable

LEDs:

- +3.3V, +5V, -5.2V Power (green)
- CLK, BX0, RES, L1A (red)
- TR1, TR2, PRT (green)
- VME Access, JTAG Access (yellow)

References

[1] B.G.Taylor. Timing, Trigger and Control (TTC) Systems for LHC Detectors. CERN/ECP http://www.cern.ch/TC/intro.html