DCFEB Optical Link Test Setup

13 August 2018

Introduction

The proposed test stand allows to test the following optical links:

- Finisar FTRJ-8519 transmitters installed on DCFEB boards in the CSC system at CMS;
- VTTX transmitters installed on xDCFEB boards in the upgraded CSC system
- Adapter boards (Finisar – to – VTTX) for DCFEBs

1. Parts

The stand consists of the following parts (Fig.1):

- Optical DAQ Motherboard version 2 (ODMBv2, [1])
- Patch Panel Interconnect Board (PPIB, preproduction version [2])
- DCFEB or xDCFEB [3] board under test
- Commercial counter, for example HP
- Windows based laptop with Xilinx ISE ver.14.7 installed; equipped with Platform Cable USB II [4]
- Three copper cables with 50-pin connectors
- Optical fanout 12 LC – to – MTP
- Power supply (PS) (should provide 3.3V @ 3A and 5V @ 1A to ODMB (separate wires) and 3V @ 3A; 4V @ 2A, 5V @ 2A (one connector) to DCFEB or xDCFEB
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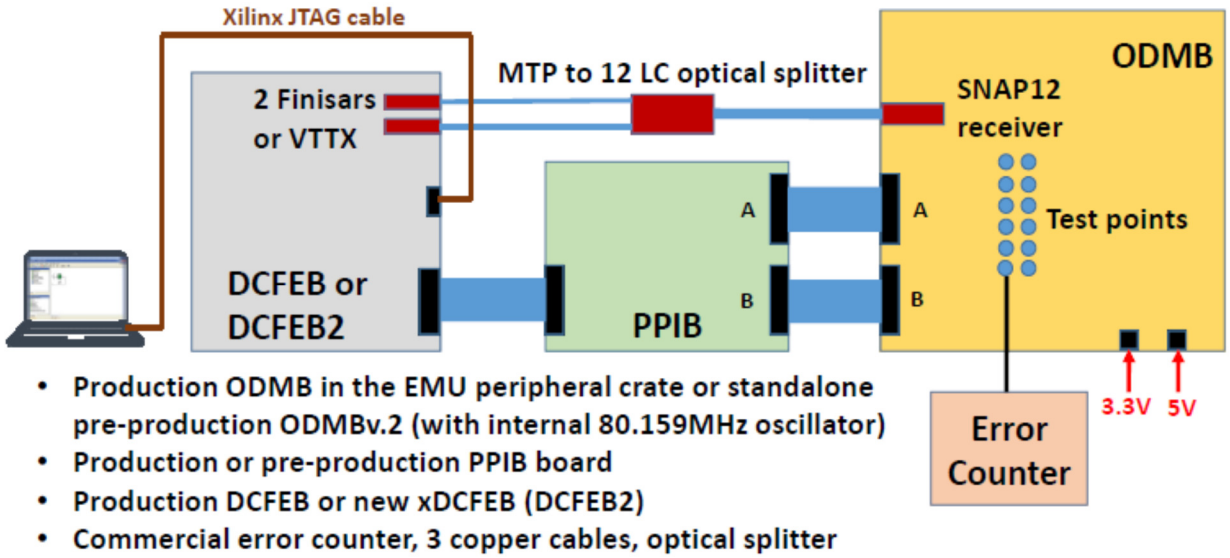

Fig.1: Block diagram of the test stand

2. Connections

- Connect +3.3V and +5V wires from PS to ODMB (Fig.2). While the ODMB is a 9U VME board, it can be used standalone, without any control software and VME crate;

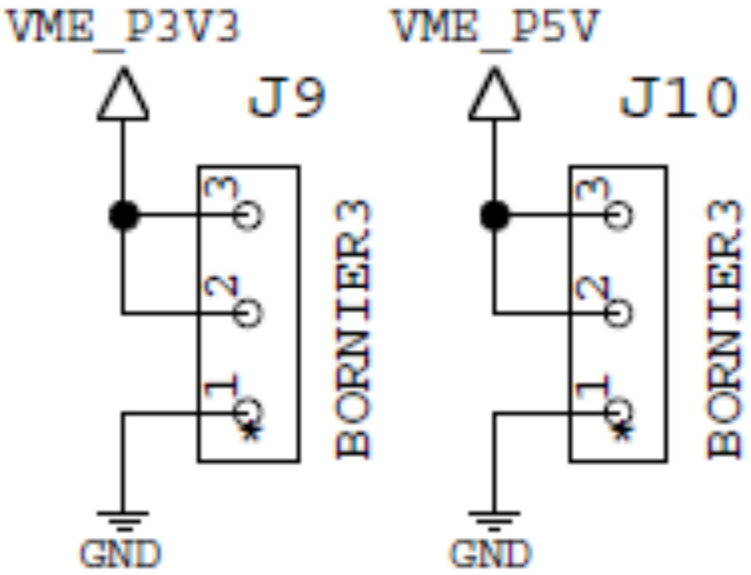

Fig.2: Power connectors of ODMB

- Connect power supply cable to DCFEB;
- Connect ODMB and PPIB with two cables; make sure “A” output of ODMB is connected to “A” input of PPIB; same for the “B” cable. +3.3V power to PPIB is provided in both these cables;
- Connect one of 7 outputs of PPIB (any of them) to DCFEB. The only signal that needs to be delivered from ODMB to DCFEB through the PPIB for this test is the 40.079MHz LHC-like clock. It is provided in LVDS levels to the inputs of QPLL and can be checked with a scope on both ends of resistor R13 (Fig.3, top side of the DCFEB board, close to 14-pin Xilinx JTAG connector).
- Connect fibers 1 and 2 of the fanout to Finisar or VTTX optical receivers. The other side of the fanout (MTP) should be connected to the 12-channel receiver on the front panel of ODMB;
- Connect an input of the Counter to either TP14 or TP15 test points on the ODMB board;
- Connect Xilinx Platform cable to ODMB (14-pin black connector on the front panel).

The test stand, as assembled at Rice University, is shown in Fig.4.

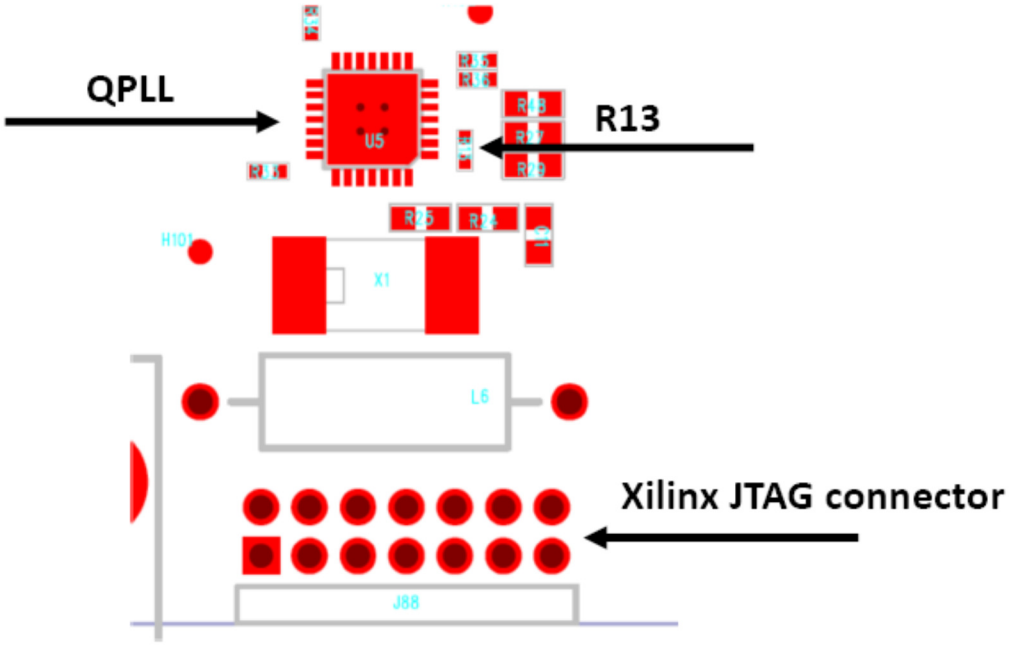

Fig.3: Position of resistor R13

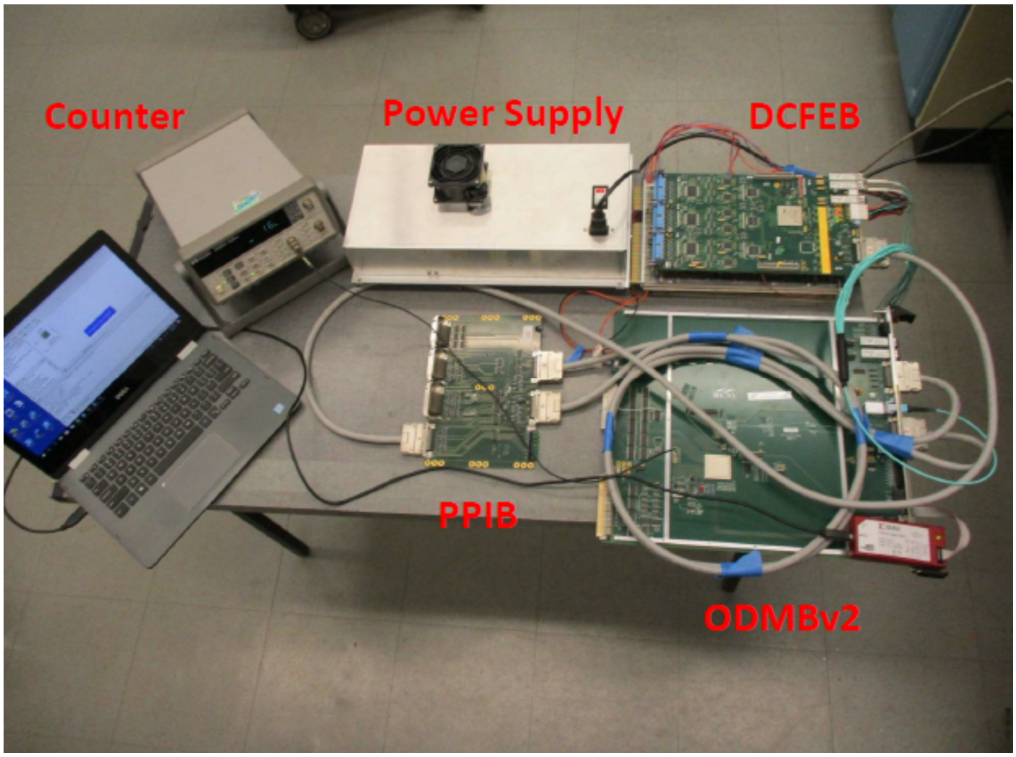

Fig.4: Picture of the test stand assembled at Rice University

3. Software and Firmware

Turn PS on. Make sure all powers are delivered to all boards correctly. Run Xilinx ISE 14.7 on your laptop. Start Impact configuration. Make sure that Impact correctly identifies Xilinx XC6VLX130T-1FGG1156C FPGA in the JTAG chain on ODMB board. You can either program the XCF128X EPROM (with the .mcs file) or load the FPGA (with the .bit file). Files for ODMBv2 #9 and #10 can be found here:

http://padley.rice.edu/cms/odmb_prbs7_071918.bit
http://padley.rice.edu/cms/odmb_prbs7_071918.mcs

The firmware for the ODMB configures 12 GTX receivers from the Reflex Photonics SNAP12 part into continuous PRBS7 receiving mode at 3.2Gbps (synchronized with the clock originating from the crystal oscillator on ODMB board). Each receiver has its own PRBSERROUT output which is routed to TP6…TP17. Errors (if any) can be counted by an external counter. There are also two internal error counters for receivers corresponding to fibers 1 and 2. Five lower bits of these counters are provided to LEDs on the front panel of ODMB (left and right colomns, see Fig.4). Push-button PB1 is needed to reload the FPGA from its XCF128X EPROM. The lower PB2 is needed to reset the internal error counters. The lower PB3 is not used.

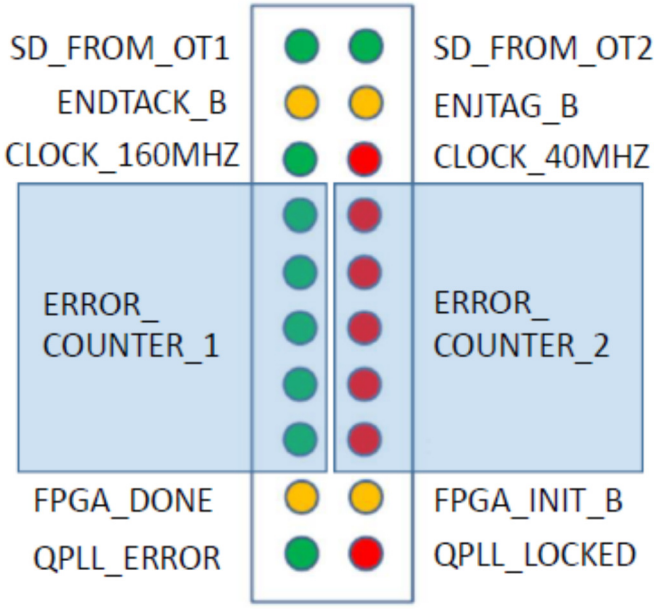

Fig.4: LEDs on the front panel of ODMB, as used in the test firmware

Remove Xilinx cable from the ODMB and plug it into the DCFEB under test (Fig.5). Initialize the chain, it should be the same as one on ODMB (XC6VLX130T-1FGG1156C FPGA with XCF128X EPROM). Load the following file into the FPGA:

http://padley.rice.edu/cms/dcfeb_prbs7_072018.bit

The firmware for the DCFEB links (or identical links on the xDCFEB) configures 2 GTX transmitters used on DCFEB into continuous PRBS7 transmitter mode at 3.2Gbps (synchronized with the clock originating from the ODMB). When the firmware is loaded, the three LED[0..2] should be blinking (~5Hz) and LED15 should be permanently "on" (QPLL on DCFEB is locked to the incoming clock). The QPLL must be locked for correct operation of optical links.

4. Measurements

When the firmware is loaded to both boards, reset the internal error counters on the ODMB and continue monitoring of TP14 and TP15 (or TP23 which is an OR of TP14 and TP15) with the counter for ~5 minutes. That's enough to transmit ~10^{12} bits. If the link operates properly, there should be no errors and there levels on TP14, TP15 and TP23 should be "0". Alternatively, the 10 LEDs on the front panel can be monitored. Then an external counter is not needed.

The easiest way to introduce errors is to unlock the QPLL on DCFEB. To do this, remove the jumper ST12 on ODMB board (eliminate the clock source to QPLL on the ODMB board). The errors should appear immediately in both links.

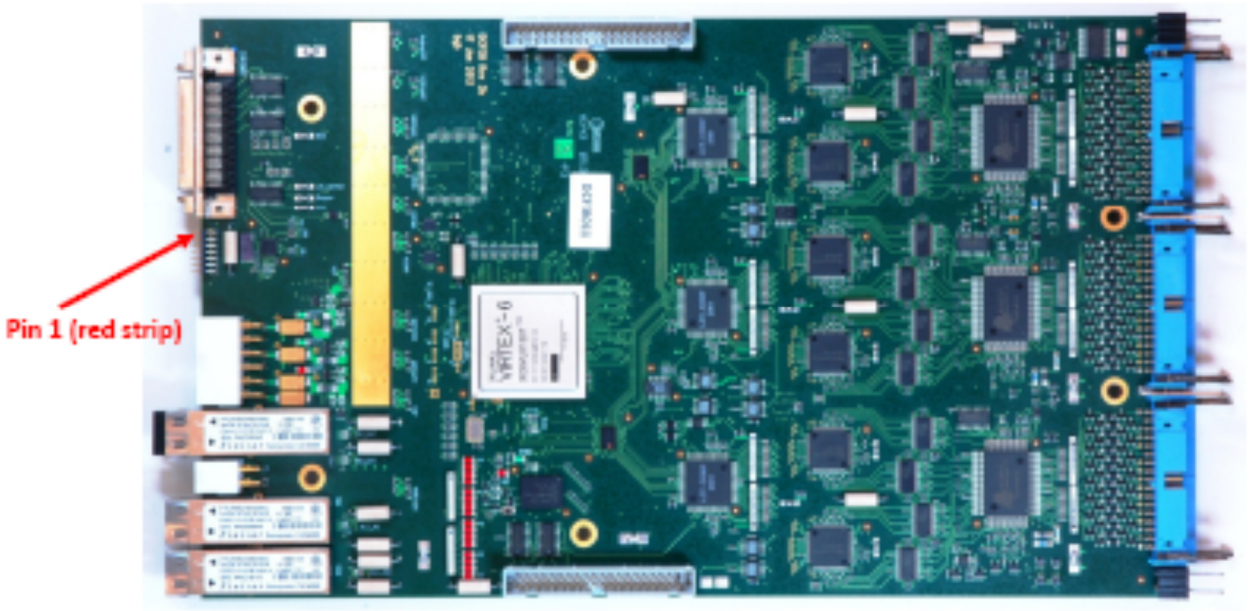

Fig.5: JTAG connection to DCFEB/xDCFEB

References

[1] http://hep.ucsb.edu/cms/odmb/hardware/odmb_v2_schematics.pdf

[2] http://padley.rice.edu/cms/Patch_Panel/EDA-02717-V1-0_sch.pdf

[3] https://twiki.cern.ch/twiki/pub/CMS/CSCdescriptionDCFEB/dcfeb_v3b.pdf

[4] https://www.xilinx.com/support/documentation/data_sheets/ds593.pdf