JTAG Controller Board Specification

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Introduction

The board is intended for evaluation of the National Semiconductor JTAG 1149.1. SCANSTA101 System Test Access Master [1]. Its block diagram is shown on Fig.1. The board is build as a VME A24D16 Slave; the dimensions are 6U x 160 mm. The VME interface circuitry is implemented in the Xilinx XCR3128 CPLD. The SCANSTA101 Master provides JTAG access to external devices via two front panel connectors. One 14-pin connector is compatible with the Xilinx JTAG cable (LVTTL levels), and another 16-pin connector is compatible with the JTAG cable for the CSC EMU Trigger Motherboard [2] (LVDS levels).

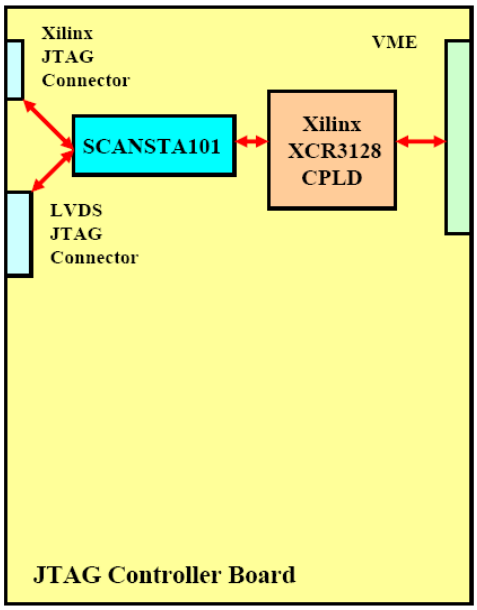

Fig.1: Block Diagram of the JTAG Controller Board

1. SCANSTA101 JTAG Master

The SCANSTA101 is designed to function as a test master for the IEEE 1149.1 boundary scan test system. It is an enhanced version, and a replacement for, the SCANPSC100 device. The interface from the SCANSTA101 to the system processor (VME bus master, in our case) is implemented by reading and writing registers, some of which map to locations in the SCANSTA101 memory. Hardware handshaking and interrupt lines are provided as part of the processor interface. The block diagram of the device is shown in Fig.2.

The external JTAG slave devices are connected via the front panel connectors. These may be any JTAG-compatible FPGA, programmable memories and others. The internal Test and Debug Interface Port (Fig.2) is not used, although its inputs and outputs are available on the board as a test points. TRIST_SM and /TRST0_SM outputs are not used. The SCK clock input is provided by the CPLD and is programmable (currently 20MHz). Addresses A[4:1] are mapped to VME address lines VME_A[4:1], and Data lines D[15:0] are mapped to VME_D[15:0].

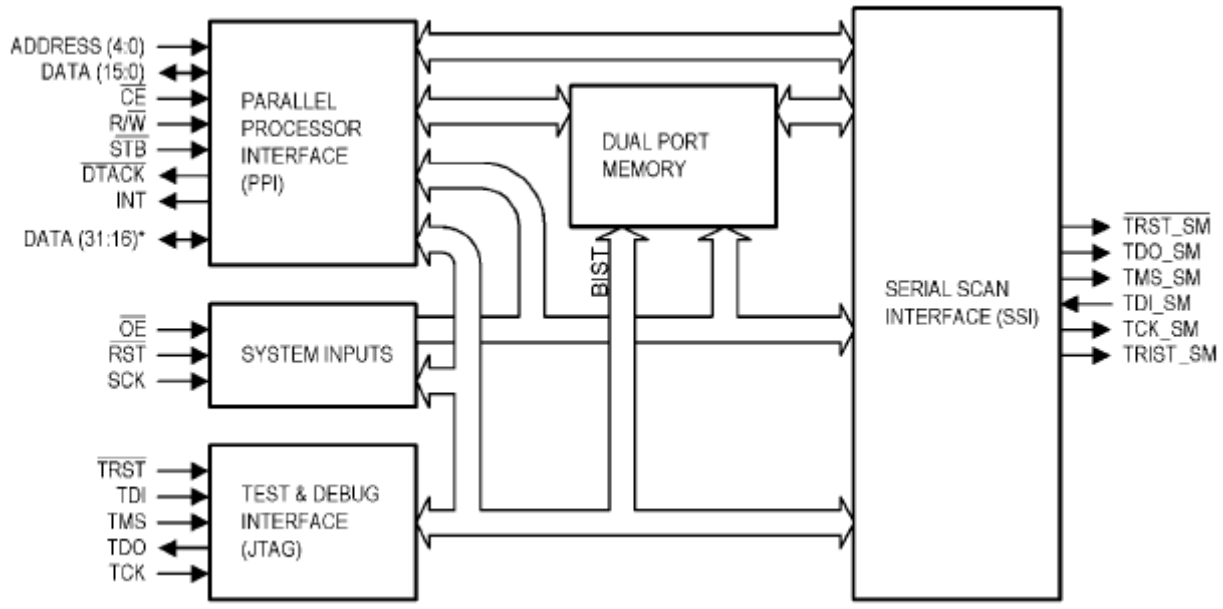

Fig.2: Block Diagram of the SCANSTA101 JTAG Master

2. VME Access

16-bit VME bus is used to access the SCANSTA101 Parallel Processor Interface. All the VME Slave A24D16 interface functions are implemented in the Xilinx XCR3128 CPLD. The upper 5 bits address bits can be decoded either from GA[4:0] geographical lines of the VME64x backplane or from the on-board switch S3. Decoded addresses are listed in Table 1. For more details see the datasheet [1]. The CPLD itself can be programmed via the standard Xilinx JTAG cable (14-pin connector P2, above the CPLD).

Table 1

Address (hex)	Register/Port	Access Type
Base + 0	SCANSTA101 Start Register	W/R
Base + 2	SCANSTA101 Status Register	W/R
Base + 4	SCANSTA101 Interrupt Control Register	W/R
Base + 6	SCANSTA101 Interrupt Status Register	W/R
Base + 8	SCANSTA101 Setup Register	W/R
Base + A	SCANSTA101 Clock Divider Register	W/R
Base + C	N/A	-
Base + E	SCANSTA101 TDI_SM LFSR Exponent Register	W/R

Base + 10	SCANSTA101 TDI_SM LFSR LSB Seed Register	W/R
Base + 12	SCANSTA101 TDI_SM LFSR MSB Seed Register	W/R
Base + 14	SCANSTA101 TDI_SM LFSR LSB Result Register	W/R
Base + 16	SCANSTA101 TDI_SM LFSR MSB Result Register	W/R
Base + 18	SCANSTA101 Index Register	W/R
Base + 1A	TDO_SM	W/R
Base + 1C	TDI_SM	W/R
Base + 1E	Expected	W/R
Base + 20	Mask	W/R
Base + 22	SCANSTA101Vector Index Register	W/R
Base + 24	Vector 1/2/3/4	W/R
Base + 26	SCANSTA101 Header/Trailer Index Register	W/R
Base + 28	Data Header/Trailer, Instruction Header/Trailer	W/R
Base + 2A	SCANSTA101 Macro Index Register	W/R
Base + 2C	Macro 1/2/3/…/16	W/R
Base + 2E	SCANSTA101 Sequencer Index Register	W/R
Base + 30	Sequencer	W/R
Base + 32	SCANSTA101 Scan Bridge Support Index Register	W/R
Base + 34	Scan Bridge Support Register	W/R
Base + 36… Base + 3E	N/A	-
Base + 40	Reset SCANSTA101 Device	Write only
Base + 60	Firmware Date (bits 4:0 = day, bits 8:5 = month, bits 12:9 = year (complement to 2000, bits 15:13 = “0”)	Read Only
Base + 62	General purpose 16-bit register	W/R
Base + 64	Reset internal VME interface circuitry	Write only

There are two clock signals provided to the CPLD from on-board oscillators: 80.157MHz and 32MHz.

3. Interrupts

Under certain conditions the SCANSTA101 Master can generate a signal to interrupt output. This output is used to generate a VME Interrupt of ROAK type (release-on-acknowledge, when the interrupter releases its interrupt request on VME bus in response to the interrupt acknowledge cycle). The actual interrupt request may be send to any of the IRQ[7:1] VME lines; the selection is defined by an on-board switch S1 (S1-1 for IRQ1, S1-2 for IRQ2 and so on; only one should be "on"). The VME interface circuitry returns the 16-bit STATUS/ID during interrupt acknowledge cycle.

4. External Connectors

There are two external connectors on the front panel of the board. Pin assignment is shown in Table 2. When S2-1 is "on", the TDO output of the P2 connector (LVTTL) is connected to TDI_SM input of the SCANSTA101 Master. When S2-1 is "off", the TDO output of the P4 connector (LVDS) is connected to TDI_SM input of the SCANSTA101 Master. The DS90LV032 receiver (with 100 Ohm termination) and DS90LV031 transmitter (without termination) are used for LVDS signals.

Table 2

14-pin connector P3 (top)		**16-pin connector P4 (bottom)**	
Pin	Signal	Pin	Signal
1	GND	1	TCK+ (LVDS, TCK_SM output of the SCANSTA101)
2	+3.3V	2	TCK- (LVDS, TCK_SM output of the SCANSTA101)
3	GND	3	TDI+ (LVDS, TDI_SM input of the SCANSTA101)
4	TMS (TMS_SM output of the SCANSTA101)	4	TDI- (LVDS, TDI_SM input of the SCANSTA101)
5	GND	5	TMS+ (LVDS, TMS_SM output of the SCANSTA101)
6	TCK (TCK_SM output of the SCANSTA101)	6	TMS- (LVDS, TMS_SM output of the SCANSTA101)
7	GND	7	+3.3V if S2-2 is "on"; not connected if S2-2 is "off"
8	TDI (TDI_SM input of the SCANSTA101)	8	GND
9	GND	9	TDO+ (LVDS, TDO_SM output of the SCANSTA101)
10	TDO (TDO_SM output of the SCANSTA101)	10	TDO1 (LVDS, TDO_SM output of the SCANSTA101)
11	GND	11	Connected to pin 12
12	Not connected	12	Connected to pin 11
13	GND	13	Connected to pin 14
14	Not connected	14	Connected to pin 13
		15	Connected to pin 16
		16	Connected to pin 15

5. Front Panel LEDs and Fuses

There are 7 LEDs on the front panel, listed below from top to bottom:

D4 (yellow) – TCK_SM output of the SCANSTA101 (with one-shot)

D6 (yellow) – VME DTACK (with one-shot; from any source: access to VME registers/ports; access to SCANSTA101 Master; interrupt acknowledge cycle)

D1 (red) – permanently blinking ~4Hz; derivative from the 80MHz oscillator frequency

D2 (red) - /DTACK output of the SCANSTA101 Master (with one-shot)

D3 (red) – not used

D7 (green) - +3.3V on-board power is “on”

D5 (green) - +5.0V on-board power is “on”

There are three fuses on the board. If the board is plugged into the VME64x compatible VME backplane, +3.3V can be provided either from the backplane (fuse F1 installed) or from the on-board voltage regulator (fuse F3 is installed). If the board is plugged into the old style VME backplane, then the +3.3V power should be provided from the regulator and fuse F3 be installed. Fuse F2 (+5V) should always be installed.

References

[1] http://www.national.com/ds/SC/SCANSTA101.pdf

[2] http://cmsdoc.cern.ch/cms/MUON/cscTrigger/html/CERN/striplct.html