Muon Port Card

Reference Manual

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Introduction

2000 Muon Port Card (MPC) Prototype board receives data from up to three Trigger Motherboards (TMB, '99 Prototypes), performs sorting "3 best muons out of 18" and transmits data representing those three best muons to Sector Receiver (SR) board over six optical links (Fig.1). MPC is interfacing with three TMB over National DS90CR285/286 Channel Link chipsets. Three DS90CR286 Channel Link receivers are needed for communication with one TMB. MPC includes six HDMP-1022 G-link serializers and six Methode MDX-19 optical modules for communication with one SR.

In addition to the main sorter logic, two groups of FIFO buffers are implemented in order to test the MPC internal logic and its communication with Trigger Motherboards (TMB) over channel links and with Sector Receiver (SR) board over optical links (Fig.2). MPC testing circuitry consists of two independent groups of FIFO buffers: FIFO_A and FIFO_B. FIFO_A is intended for testing of communication with SR and consists of 15 buffers available from VME for write and read operation (Tables 1 and 2). FIFO_A is 240-bit wide and 8-bit deep. Test patterns representing six muons can be transmitted simultaneously from all FIFOs to G-link transmitters and further to SR at 40MHz on VME command (see Table 1). FIFO_B is intended for testing of the communication with TMB. It consists of 9 buffers available from VME for read and write operations (Tables 1 and 3). FIFO_B is 120-bit wide and 8-bit deep. Patterns rearranged after the sorting logic (from either TMBs, or FIFO_A) can be received and stored in FIFO_B.

1. VME Interface

MPC can be addressed using either geographical or logical A24D16 addressing. An on-board DIP switch S2-8 is used for mode selection. When S2 8-9 switch is "off", the geographical mode is selected. When S2 8-9 switch is "on", the logical address mode is selected. Geographical mode utilizes the geographical address lines GA<4-0> available on VME64x backplane. In this mode the MPC recognizes its address space when the code on address lines A<23-19> is equal to the 5-bit geographical address of the slot in crate where it is located.

During the initial MPC testing and debugging base address E00000(hex) and logical address mode are used. Decoded addresses and VME commands are listed in Table 1.

Table 1

Address (hex)	Access	Function
E04040	Read/Write	CSR1
E04042	-	Reserved
E04044	Write	Generate FRAMES signal to all G-link transmitters
E04046	Write	Generate RESET signal to all G-link transmitters
E04048	Write	Generate RESET signal to all FIFO_A and FIFO_B
E0404A	Write	Generate RESET MPC internal logic
E04000	Read/Write	FIFO_B1
E04002	Read/Write	FIFO_B2
E04004	Read/Write	FIFO_B3
E04006	Read/Write	FIFO_B4
E04008	Read/Write	FIFO_B5
E0400A	Read/Write	FIFO_B6
E0400C	Read/Write	FIFO_B7
E0400E	Read/Write	FIFO_B8
E04010	Read/Write	FIFO_B9
E04014	Read/Write	CSR7
E04016	Read/Write	CSR6
E04018	Read	CSR3 (FIFO_B FULL status)
E0401A	Read	CSR4 (FIFO_B EMPTY status)
E0401C	Read/Write	CSR2
E0401E	Read/Write	CSR5
E04020	Read/Write	FIFO_A1
E04022	Read/Write	FIFO_A2
E04024	Read/Write	FIFO_A3
E04026	Read/Write	FIFO_A4
E04028	Read/Write	FIFO_A5
E0402A	Read/Write	FIFO_A6
E0402C	Read/Write	FIFO_A7
E0402E	Read/Write	FIFO_A8
E04030	Read/Write	FIFO_A9
E04032	Read/Write	FIFO_A10
E04034	Read/Write	FIFO_A11
E04036	Read/Write	FIFO_A12
E04038	Read/Write	FIFO_A13
E0403A	Read/Write	FIFO_A14
E0403C	Read/Write	FIFO_A15
E0403E	Write	Send 8 words from all FIFO_A in Test mode
E00000-E007FE	Read/Write	LUT RAM1 (Muon 1)
E00800-E00FFE	Read/Write	LUT RAM2 (Muon 2)
E01000-E017FE	Read/Write	LUT RAM3 (Muon 3)
E01800-E01FFE	Read/Write	LUT RAM4 (Muon 4)
E02000-E027FE	Read/Write	LUT RAM5 (Muon 5)
E02800-E02FFE	Read/Write	LUT RAM6 (Muon 6)

2. FIFO Buffers

FIFO_A bit assignment is given in Table 2.

Table 2

FIFO_A Buffers

Buffer	Muon	Function	Buffer	Muon	Function	Buffer	Muon	Function
FIFO1_0	1	FLAG	FIFO6_0	3	FLAG	FIFO11_0	5	FLAG
FIFO1_1	1	S_PAT1	FIFO6_1	3	S_PAT1	FIFO11_1	5	S_PAT1
FIFO1_2	1	S_PAT2	FIFO6_2	3	S_PAT2	FIFO11_2	5	S_PAT2
FIFO1_3	1	S_PAT3	FIFO6_3	3	S_PAT3	FIFO11_3	5	S_PAT3
FIFO1_4	1	S_PAT4	FIFO6_4	3	S_PAT4	FIFO11_4	5	S_PAT4
FIFO1_5	1	S_PAT5	FIFO6_5	3	S_PAT5	FIFO11_5	5	S_PAT5
FIFO1_6	1	S_PAT6	FIFO6_6	3	S_PAT6	FIFO11_6	5	S_PAT6
FIFO1_7	1	S_PAT7	FIFO6_7	3	S_PAT7	FIFO11_7	5	S_PAT7
FIFO1_8	1	S_PAT8	FIFO6_8	3	S_PAT8	FIFO11_8	5	S_PAT8
FIFO1_9	1	S_L/R	FIFO6_9	3	S_L/R	FIFO11_9	5	S_L/R
FIFO1_10	1	S_HS1	FIFO6_10	3	S_HS1	FIFO11_10	5	S_HS1
FIFO1_11	1	S_HS2	FIFO6_11	3	S_HS2	FIFO11_11	5	S_HS2
FIFO1_12	1	S_HS3	FIFO6_12	3	S_HS3	FIFO11_12	5	S_HS3
FIFO1_13	1	S_HS4	FIFO6_13	3	S_HS4	FIFO11_13	5	S_HS4
FIFO1_14	1	S_HS5	FIFO6_14	3	S_HS5	FIFO11_14	5	S_HS5
FIFO1_15	1	S_HS6	FIFO6_15	3	S_HS6	FIFO11_15	5	S_HS6
FIFO2_0	1	S_HS7	FIFO7_0	3	S_HS7	FIFO12_0	5	S_HS7
FIFO2_1	1	S_HS8	FIFO7_1	3	S_HS8	FIFO12_1	5	S_HS8
FIFO2_2	1	W_PQ1	FIFO7_2	3	W_PQ1	FIFO12_2	5	W_PQ1
FIFO2_3	1	W_PQ2	FIFO7_3	3	W_PQ2	FIFO12_3	5	W_PQ2
FIFO2_4	1	W_AMU	FIFO7_4	3	W_AMU	FIFO12_4	5	W_AMU
FIFO2_5	1	W_GID1	FIFO7_5	3	W_GID1	FIFO12_5	5	W_GID1
FIFO2_6	1	W_GID2	FIFO7_6	3	W_GID2	FIFO12_6	5	W_GID2
FIFO2_7	1	W_GID3	FIFO7_7	3	W_GID3	FIFO12_7	5	W_GID3
FIFO2_8	1	W_GID4	FIFO7_8	3	W_GID4	FIFO12_8	5	W_GID4
FIFO2_9	1	W_GID5	FIFO7_9	3	W_GID5	FIFO12_9	5	W_GID5
FIFO2_10	1	W_GID6	FIFO7_10	3	W_GID6	FIFO12_10	5	W_GID6
FIFO2_11	1	W_GID7	FIFO7_11	3	W_GID7	FIFO12_11	5	W_GID7
FIFO2_12	1	W_BX1	FIFO7_12	3	W_BX1	FIFO12_12	5	W_BX1
FIFO2_13	1	W_BX2	FIFO7_13	3	W_BX2	FIFO12_13	5	W_BX2
FIFO2_14	1	W_BX3	FIFO7_14	3	W_BX3	FIFO12_14	5	W_BX3
FIFO2_15	1	W_BX4	FIFO7_15	3	W_BX4	FIFO12_15	5	W_BX4
FIFO3_0	1	W_BX5	FIFO8_0	3	W_BX5	FIFO13_0	5	W_BX5
FIFO3_1	1	BXMA1	FIFO8_1	3	BXMA1	FIFO13_1	5	BXMA1
FIFO3_2	1	BXMA2	FIFO8_2	3	BXMA2	FIFO13_2	5	BXMA2
FIFO3_3	1	STA1	FIFO8_3	3	STA1	FIFO13_3	5	STA1
FIFO3_4	1	STA2	FIFO8_4	3	STA2	FIFO13_4	5	STA2
FIFO3_5	1	STB1	FIFO8_5	3	STB1	FIFO13_5	5	STB1
FIFO3_6	1	STB2	FIFO8_6	3	STB2	FIFO13_6	5	STB2
FIFO3_7	1	SY_ER	FIFO8_7	3	SY_ER	FIFO13_7	5	SY_ER
FIFO3_8	2	FLAG	FIFO8_8	4	FLAG	FIFO13_8	6	FLAG
FIFO3_9	2	S_PAT1	FIFO8_9	4	S_PAT1	FIFO13_9	6	S_PAT1
FIFO3_10	2	S_PAT2	FIFO8_10	4	S_PAT2	FIFO13_10	6	S_PAT2
FIFO3_11	2	S_PAT3	FIFO8_11	4	S_PAT3	FIFO13_11	6	S_PAT3
FIFO3_12	2	S_PAT4	FIFO8_12	4	S_PAT4	FIFO13_12	6	S_PAT4
FIFO3_13	2	S_PAT5	FIFO8_13	4	S_PAT5	FIFO13_13	6	S_PAT5

FIFO3_14	2	S_PAT6	FIFO8_14	4	S_PAT6	FIFO13_14	6	S_PAT6
FIFO3_15	2	S_PAT7	FIFO8_15	4	S_PAT7	FIFO13_15	6	S_PAT7
FIFO4_0	2	S_PAT8	FIFO9_0	4	S_PAT8	FIFO14_0	6	S_PAT8
FIFO4_1	2	S_L/R	FIFO9_1	4	S_L/R	FIFO14_1	6	S_L/R
FIFO4_2	2	S_HS1	FIFO9_2	4	S_HS1	FIFO14_2	6	S_HS1
FIFO4_3	2	S_HS2	FIFO9_3	4	S_HS2	FIFO14_3	6	S_HS2
FIFO4_4	2	S_HS3	FIFO9_4	4	S_HS3	FIFO14_4	6	S_HS3
FIFO4_5	2	S_HS4	FIFO9_5	4	S_HS4	FIFO14_5	6	S_HS4
FIFO4_6	2	S_HS5	FIFO9_6	4	S_HS5	FIFO14_6	6	S_HS5
FIFO4_7	2	S_HS6	FIFO9_7	4	S_HS6	FIFO14_7	6	S_HS6
FIFO4_8	2	S_HS7	FIFO9_8	4	S_HS7	FIFO14_8	6	S_HS7
FIFO4_9	2	S_HS8	FIFO9_9	4	S_HS8	FIFO14_9	6	S_HS8
FIFO4_10	2	W_PQ1	FIFO9_10	4	W_PQ1	FIFO14_10	6	W_PQ1
FIFO4_11	2	W_PQ2	FIFO9_11	4	W_PQ2	FIFO14_11	6	W_PQ2
FIFO4_12	2	W_AMU	FIFO9_12	4	W_AMU	FIFO14_12	6	W_AMU
FIFO4_13	2	W_GID1	FIFO9_13	4	W_GID1	FIFO14_13	6	W_GID1
FIFO4_14	2	W_GID2	FIFO9_14	4	W_GID2	FIFO14_14	6	W_GID2
FIFO4_15	2	W_GID3	FIFO9_15	4	W_GID3	FIFO14_15	6	W_GID3
FIFO5_0	2	W_GID4	FIFO10_0	4	W_GID4	FIFO15_0	6	W_GID4
FIFO5_1	2	W_GID5	FIFO10_1	4	W_GID5	FIFO15_1	6	W_GID5
FIFO5_2	2	W_GID6	FIFO10_2	4	W_GID6	FIFO15_2	6	W_GID6
FIFO5_3	2	W_GID7	FIFO10_3	4	W_GID7	FIFO15_3	6	W_GID7
FIFO5_4	2	W_BX1	FIFO10_4	4	W_BX1	FIFO15_4	6	W_BX1
FIFO5_5	2	W_BX2	FIFO10_5	4	W_BX2	FIFO15_5	6	W_BX2
FIFO5_6	2	W_BX3	FIFO10_6	4	W_BX3	FIFO15_6	6	W_BX3
FIFO5_7	2	W_BX4	FIFO10_7	4	W_BX4	FIFO15_7	6	W_BX4
FIFO5_8	2	W_BX5	FIFO10_8	4	W_BX5	FIFO15_8	6	W_BX5
FIFO5_9	2	BXMA1	FIFO10_9	4	BXMA1	FIFO15_9	6	BXMA1
FIFO5_10	2	BXMA2	FIFO10_10	4	BXMA2	FIFO15_10	6	BXMA2
FIFO5_11	2	STA1	FIFO10_11	4	STA1	FIFO15_11	6	STA1
FIFO5_12	2	STA2	FIFO10_12	4	STA2	FIFO15_12	6	STA2
FIFO5_13	2	STB1	FIFO10_13	4	STB1	FIFO15_13	6	STB1
FIFO5_14	2	STB2	FIFO10_14	4	STB2	FIFO15_14	6	STB2
FIFO5_15	2	SY_ER	FIFO10_15	4	SY_ER	FIFO15_15	6	SY_ER

Bit assignment of all FIFO_B buffers is given in Table 3. More detailed bit definition can be found in TMB Manual. One important feature of FIFO_B buffers is that data from FIFO_A or from TMB can be saved in FIFO_B only if there is at least one valid muon. This allows to acquire into FIFO_B the data, representing valid muons only. FLAG Bit from Muon 1 acts as a "Write Enable" signal for all FIFO_B buffers. This means that if there is just one valid muon coming from FIFO_A or TMB, it will be stored in FIFO_B<1..3> and "0" will be written into FIFO_B<4..9>. This feature assures that all FIFO_B buffers will contain the equal number of words inside. As for VME access, any data can be loaded and read out of any FIFO_B buffer independently.

Table 3

FIFO_B Buffers

Buffer	Muon	Function	Buffer	Muon	Function	Buffer	Muon	Function
FIFO1_0	1	FLAG	FIFO4_0	2	FLAG	FIFO7_0	3	FLAG
FIFO1_1	1	S_PAT1	FIFO4_1	2	S_PAT1	FIFO7_1	3	S_PAT1
FIFO1_2	1	S_PAT2	FIFO4_2	2	S_PAT2	FIFO7_2	3	S_PAT2

FIFO1_3	1	S_PAT3	FIFO4_3	2	S_PAT3	FIFO7_3	3	S_PAT3
FIFO1_4	1	S_PAT4	FIFO4_4	2	S_PAT4	FIFO7_4	3	S_PAT4
FIFO1_5	1	S_PAT5	FIFO4_5	2	S_PAT5	FIFO7_5	3	S_PAT5
FIFO1_6	1	S_PAT6	FIFO4_6	2	S_PAT6	FIFO7_6	3	S_PAT6
FIFO1_7	1	S_PAT7	FIFO4_7	2	S_PAT7	FIFO7_7	3	S_PAT7
FIFO1_8	1	S_PAT8	FIFO4_8	2	S_PAT8	FIFO7_8	3	S_PAT8
FIFO1_9	1	S_L/R	FIFO4_9	2	S_L/R	FIFO7_9	3	S_L/R
FIFO1_10	1	S_HS1	FIFO4_10	2	S_HS1	FIFO7_10	3	S_HS1
FIFO1_11	1	S_HS2	FIFO4_11	2	S_HS2	FIFO7_11	3	S_HS2
FIFO1_12	1	S_HS3	FIFO4_12	2	S_HS3	FIFO7_12	3	S_HS3
FIFO1_13	1	S_HS4	FIFO4_13	2	S_HS4	FIFO7_13	3	S_HS4
FIFO1_14	1	S_HS5	FIFO4_14	2	S_HS5	FIFO7_14	3	S_HS5
FIFO1_15	1	S_HS6	FIFO4_15	2	S_HS6	FIFO7_15	3	S_HS6
FIFO2_0	1	S_HS7	FIFO5_0	2	S_HS7	FIFO8_0	3	S_HS7
FIFO2_1	1	S_HS8	FIFO5_1	2	S_HS8	FIFO8_1	3	S_HS8
FIFO2_2	1	W_PQ1	FIFO5_2	2	W_PQ1	FIFO8_2	3	W_PQ1
FIFO2_3	1	W_PQ2	FIFO5_3	2	W_PQ2	FIFO8_3	3	W_PQ2
FIFO2_4	1	W_AMU	FIFO5_4	2	W_AMU	FIFO8_4	3	W_AMU
FIFO2_5	1	W_GID1	FIFO5_5	2	W_GID1	FIFO8_5	3	W_GID1
FIFO2_6	1	W_GID2	FIFO5_6	2	W_GID2	FIFO8_6	3	W_GID2
FIFO2_7	1	W_GID3	FIFO5_7	2	W_GID3	FIFO8_7	3	W_GID3
FIFO2_8	1	W_GID4	FIFO5_8	2	W_GID4	FIFO8_8	3	W_GID4
FIFO2_9	1	W_GID5	FIFO5_9	2	W_GID5	FIFO8_9	3	W_GID5
FIFO2_10	1	W_GID6	FIFO5_10	2	W_GID6	FIFO8_10	3	W_GID6
FIFO2_11	1	W_GID7	FIFO5_11	2	W_GID7	FIFO8_11	3	W_GID7
FIFO2_12	1	W_BX1	FIFO5_12	2	W_BX1	FIFO8_12	3	W_BX1
FIFO2_13	1	W_BX2	FIFO5_13	2	W_BX2	FIFO8_13	3	W_BX2
FIFO2_14	1	W_BX3	FIFO5_14	2	W_BX3	FIFO8_14	3	W_BX3
FIFO2_15	1	W_BX4	FIFO5_15	2	W_BX4	FIFO8_15	3	W_BX4
FIFO2_0	1	W_BX5	FIFO6_0	2	W_BX5	FIFO9_0	3	W_BX5
FIFO3_1	1	BXMA1	FIFO6_1	2	BXMA1	FIFO9_1	3	BXMA1
FIFO3_2	1	BXMA2	FIFO6_2	2	BXMA2	FIFO9_2	3	BXMA2
FIFO3_3	1	STA1	FIFO6_3	2	STA1	FIFO9_3	3	STA1
FIFO3_4	1	STA2	FIFO6_4	2	STA2	FIFO9_4	3	STA2
FIFO3_5	1	STB1	FIFO6_5	2	STB1	FIFO9_5	3	STB1
FIFO3_6	1	STB1	FIFO6_6	2	STB1	FIFO9_6	3	STB1
FIFO3_7	1	SYER	FIFO6_7	2	SYER	FIFO9_7	3	SYER

FIFO_B3<8..15>, FIFO_B6<8..15> and FIFO_B9<8..15> are always “0”.

3. Interface to Sector Receiver

MPC transmits data to SR over six optical links (120 bits total, representing three best muons based on result of sorting). Data format is given in Table 4. CSCID bits represent the geographical number of each TMB connected to MPC. Muon 1 and muon 2 arrive from TMB1, muons 3 and 4 arrive from TMB2 etc. Bunch crossing number transmitted to SR belongs to the first best muon. SY_ER can be translated from muon 1 (when CSR5<8>=1) or arrive from MPC synchronization logic. Upon Reset signal from CCB this logic sets up the 5-bit bunch crossing number counter into predefined state (CSR5<7..3>). Upon BX0 signal from CCB the synchronization logic is enabled and BXN counter starts counting on the next (BX1) clock pulse. The result of comparison of

the counter output against BXN permanently arriving along with the first, second, or third best output muons (selection is done using CSR5<2..1>) acts as a SY_ER bit from MPC. This internal logic of synchronization checking can be disabled if CSR5<0>=0.

CSCID<4..1> bits, corresponding to the source chambers, where the muons 1..6 came from, can be programmed in CSR6 and CSR7 (see Section 4) individually for each muon.

Table 4

Output data format to Sector Receiver

G-link	Muon	Function	G-link	Muon	Function	G-link	Muon	Function
Glink1_0	1	FLAG	Glink3_0	2	FLAG	Glink5_0	3	FLAG
G-link1_1	1	S_PAT1	G-link3_1	2	S_PAT1	G-link5_1	3	S_PAT1
G-link1_2	1	S_PAT2	G-link3_2	2	S_PAT2	G-link5_2	3	S_PAT2
G-link1_3	1	S_PAT3	G-link3_3	2	S_PAT3	G-link5_3	3	S_PAT3
G-link1_4	1	S_PAT4	G-link3_4	2	S_PAT4	G-link5_4	3	S_PAT4
G-link1_5	1	S_PAT5	G-link3_5	2	S_PAT5	G-link5_5	3	S_PAT5
G-link1_6	1	S_PAT6	G-link3_6	2	S_PAT6	G-link5_6	3	S_PAT6
G-link1_7	1	S_PAT7	G-link3_7	2	S_PAT7	G-link5_7	3	S_PAT7
G-link1_8	1	S_PAT8	G-link3_8	2	S_PAT8	G-link5_8	3	S_PAT8
G-link1_9	1	S_L/R	G-link3_9	2	S_L/R	G-link5_9	3	S_L/R
G-link1_10	1	S_HS1	G-link3_10	2	S_HS1	G-link5_10	3	S_HS1
G-link1_11	1	S_HS2	G-link3_11	2	S_HS2	G-link5_11	3	S_HS2
G-link1_12	1	S_HS3	G-link3_12	2	S_HS3	G-link5_12	3	S_HS3
G-link1_13	1	S_HS4	G-link3_13	2	S_HS4	G-link5_13	3	S_HS4
G-link1_14	1	S_HS5	G-link3_14	2	S_HS5	G-link5_14	3	S_HS5
G-link1_15	1	S_HS6	G-link3_15	2	S_HS6	G-link5_15	3	S_HS6
G-link1_15	1	S_HS7	G-link3_15	2	S_HS7	G-link5_15	3	S_HS7
G-link1_17	1	S_HS8	G-link3_17	2	S_HS8	G-link5_17	3	S_HS8
G-link1_18	1	W_PQ1	G-link3_18	2	W_PQ1	G-link5_18	3	W_PQ1
G-link1_19	1	W_PQ2	G-link3_19	2	W_PQ2	G-link5_19	3	W_PQ2
G-link2_0	1	W_AMU	G-link4_0	2	W_AMU	G-link6_0	3	W_AMU
G-link2_1	1	W_GID1	G-link4_1	2	W_GID1	G-link6_1	3	W_GID1
G-link2_2	1	W_GID2	G-link4_2	2	W_GID2	G-link6_2	3	W_GID2
G-link2_3	1	W_GID3	G-link4_3	2	W_GID3	G-link6_3	3	W_GID3
G-link2_4	1	W_GID4	G-link4_4	2	W_GID4	G-link6_4	3	W_GID4
G-link2_5	1	W_GID5	G-link4_5	2	W_GID5	G-link6_5	3	W_GID5
Glink2_6	1	W_GID6	Glink4_6	2	W_GID6	Glink6_6	3	W_GID6
G-link2_7	1	W_GID7	G-link4_7	2	W_GID7	G-link6_7	3	W_GID7
G-link2_8	1	CSCID1	G-link4_8	2	CSCID1	G-link6_8	3	CSCID1
G-link2_9	1	CSCID2	G-link4_9	2	CSCID2	G-link6_9	3	CSCID2
G-link2_10	1	CSCID3	G-link4_10	2	CSCID3	G-link6_10	3	CSCID3
G-link2_11	1	CSCID4	G-link4_11	2	CSCID4	G-link6_11	3	CSCID4
G-link2_12	1	BXMA1	G-link4_12	2	BXMA1	G-link6_12	3	BXMA1
Glink2_13	1	BXMA2	Glink4_13	2	BXMA2	Glink6_13	3	BXMA2
Glink2_14	1	STA1	Glink4_14	2	STA1	Glink6_14	3	STA1
Glink2_15	1	STA2	Glink4_15	2	STA2	Glink6_15	3	STA2
Glink2_16	1	STB1	Glink4_16	2	STB1	Glink6_16	3	STB1
Glink2_17	1	STB2	Glink4_17	2	STB2	Glink6_17	3	STB2
Glink2_18	1	W_BX1	Glink4_18	2	W_BX3	Glink6_18	3	W_BX5
Glink2_19	1	W_BX2	Glink4_19	2	W_BX4	Glink6_19	3	SY_ER

4. Control and Status Registers

CSR1 is implemented inside VME interface EPM9320GC280 PLD. CSR2…CSR7 (Table 5) are implemented inside sorter EPF10K200EGC599 PLD.

CSR1<0> - Test/Trigger Mode. When "1", FIFO_A is a data source for sorting logic and G-links. When "0", Trigger Motherboards are the sources of data.
CSR1<1> - INHIBIT. When "0", all Channel Link receiver outputs are in 3-state Condition, ensuring low current at power down. When "1", each power-down pin of 9 channel link receivers is enabled by CSR2<0..8>.
CSR1<15..2> - reserved
CSR2<0..8> When "1", set the power-down pin of channel link receivers 0..8 to high (active) state, i.e. enables channel links.
CSR2<9> When "1", enables sending 8 words from FIFO_A on BX0 command coming from CCB module (for testing purposes only)
CSR2<15..10> - reserved
CSR5<0> When "0" disabled the synchronization checking logic
CSR5<2..1> Selects first, second, or third best output muons against which BXN the synchronization checking is performed

CSR5<2>	CSR5<1>	
0	0	Muon 1
0	1	Muon 2
1	0	Muon 3
1	1	Not used

CSR5<7..3> Defines the BXN offset for MPC
CSR5<8> When "1", enables translation of SY_ER to SR from the first best muon only When "0", the SY_ER from the first best muon and MPC synchronization logic are OR'ed before transmission to SR.

Table 5

Bit	CSR3	CSR4
0	FIFO_B1_FULL (Low Byte)	FIFO_B1_EMPTY (Low Byte)
1	FIFO_B1_FULL (High Byte)	FIFO_B1_EMPTY (High Byte)
2	FIFO_B2_FULL (Low Byte)	FIFO_B2_EMPTY (Low Byte)
3	FIFO_B2_FULL (High Byte)	FIFO_B2_EMPTY (High Byte)
4	FIFO_B3_FULL (Low Byte)	FIFO_B3_EMPTY (Low Byte)
5	FIFO_B4_FULL (Low Byte)	FIFO_B4_EMPTY (Low Byte)
6	FIFO_B4_FULL (High Byte)	FIFO_B4_EMPTY (High Byte)
7	FIFO_B5_FULL (Low Byte)	FIFO_B5_EMPTY (Low Byte)
8	FIFO_B5_FULL (High Byte)	FIFO_B5_EMPTY (High Byte)
9	FIFO_B6_FULL (Low Byte)	FIFO_B6_EMPTY (Low Byte)
10	FIFO_B7_FULL (Low Byte)	FIFO_B7_EMPTY (Low Byte)
11	FIFO_B7_FULL (High Byte)	FIFO_B7_EMPTY (High Byte)
12	FIFO_B8_FULL (Low Byte)	FIFO_B8_EMPTY (Low Byte)
13	FIFO_B8_FULL (High Byte)	FIFO_B8_EMPTY (High Byte)
14	FIFO_B9_FULL (Low Byte)	FIFO_B9_EMPTY (Low Byte)
15	0	0

CSR6<3..0> defines the CSCID<4..1> corresponding to muon 1
CSR6<7..4> defines the CSCID<4..1> corresponding to muon 2
CSR6<11..8> defines the CSCID<4..1> corresponding to muon 3
CSR6<15..12> defines the CSCID<4..1> corresponding to muon 4
CSR7<3..0> defines the CSCID<4..1> corresponding to muon 5
CSR7<7..4> defines the CSCID<4..1> corresponding to muon 6

5. Look-Up Table RAM

Look-UP Table (LUT) RAM buffers are intended for translation of the 10-bit wire (anode) and strip (cathode) code for each incoming muon into 8-bit "quality" patterns using for sorting. Six LUT RAM buffers 1024*8 bits each are implemented into embedded RAM sells of the sorter PLD (EPF10K200EGC599). The larger the 8-bit RAM output code, the better for testing purposes the particular muon is. 8-bit strip SPAT<1..8> and 2-bit wire WPQ<1..2> bits arrange an address of each LUT RAM (see Table 6).

Table 6

LUT RAM Address Bit	Code
A10	W_PQ2
A9	W_PQ1
A8	S_PAT8
A7	S_PAT7
A6	S_PAT6
A5	S_PAT5
A4	S_PAT4
A3	S_PAT3
A2	S_PAT2
A1	S_PAT1

6. Sorting Logic

Sorting logic accepts 18 8-bit patterns from LUT RAM buffers representing the "quality" of each incoming muon and outputs the numbers of the first, second and third largest patterns (3*18=54 bits total). These 54 bits are used for the muon multiplexing onto sorter outputs. Because only six out of 18 muons are actually coming into MPC, the rest 12 patterns are set to "0", but sorting logic performs true sorting "3 objects out of 18". Sorting takes two clock cycles of the main 40MHz frequency. Three best muons in ranked order (120 bits total) are sent to six HDMP-1022 G-link serializers for further transmission to SR over optical cables.

7. On-board connectors and jumpers

Three 68-pin connectors J8, J14 and J15 located on the main 9U*400 mm MPC board are intended for communication with TMB over National DS90CR285/286 channel links. Pin assignment is given in Table 7.

Table 7

Pin	Channel Link	TMB Signal	MPC Signal	Pin	Channel Link	TMB Signal	MPC Signal
1	-	GND	GND	2	-	GND	GND
3	1	TxOUT0+	RxIN0+	4	1	TxOUT0-	RxIN0-
5	-	GND	GND	6	-	GND	GND
7	1	TxOUT1+	RxIN1+	8	1	TxOUT1-	RxIN1-
9	-	GND	GND	10	-	GND	GND
11	1	TxOUT2+	RxIN2+	12	1	TxOUT2-	RxIN2-
13	-	GND	GND	14	-	GND	GND
15	1	TxCLK+	RxCLK+	16	1	TxCLK-	RxCLK-
17	-	GND	GND	18	-	GND	GND
19	1	TxOUT3+	TxIN3+	20	1	TxOUT3-	RxIN3-
21	-	GND	GND	22	-	GND	GND
23	2	TxOUT0+	RxIN0+	24	2	TxOUT0-	RxIN0-
25	-	GND	GND	26	-	GND	GND
27	2	TxOUT1+	RxIN1+	28	2	TxOUT1-	RxIN1-
29	-	GND	GND	30	-	GND	GND
31	2	TxOUT2+	RxIN2+	32	2	TxOUT2-	RxIN2-
33	-	GND	GND	34	-	GND	GND
35	2	TxCLK+	RxCLK+	36	2	TxCLK-	RxCLK1-
37	-	GND	GND	38	-	GND	GND
39	2	TxOUT3+	RxIN3+	40	2	TxOUT3-	RxIn3-
41	-	GND	GND	42	-	GND	GND
43	3	TxOUT0+	RxIN0+	44	3	TxOUT0-	RxIN0-
45	-	GND	GND	46	-	GND	GND
47	3	TxOUT1+	RxIN2+	48	3	TxOUT1-	RxIN1-
49	-	GND	GND	50	-	GND	GND
51	3	TxOUT2+	RxIN2+	52	3	TxOUT2-	RxIN2-
53	-	GND	GND	54	-	GND	GND
55	3	TxCLK+	RxCLK+	56	3	TxCLK-	RxCLK-
57	-	GND	GND	58	-	GND	GND
59	3	TxOUT3+	RxIN3+	60	3	TxOUT3-	RxIN3-
61	-	GND	GND	62	-	GND	GND
63	-	GND	GND	64	-	GND	GND
65	-	Not used	Not used	66	-	Not used	Not used
67	-	Not used	Not used	68	-	Not used	Not used

20-pin J11 connector is intended for connection to Clock and Control Board (version CCB’99). Its pin assignment is given in Table 8. L1ACC is not used.

Table 8

Contact	Signal	Contact	Signal
1	GND	2	GND
3	CLOCK+	4	CLOCK-
5	GND	6	GND
7	BX0+	8	BX0-
9	GND	10	GND
11	RESET+	12	RESET-
13	GND	14	GND

15	L1ACC+	16	L1ACC-
17	GND	18	GND
19	GND	20	GND

10-pin J12 on the main MPC board is intended for the Altera Bit- or ByteBlaster connection for programming of the EPM9320 EPROM. Identical J7 connector on the mezzanine card is intended for the programming of two serial PROMs EPC2 and /or downloading of the EPF10K200EGC599 PLD over JTAG cable. Pin assignment of these connectors is given in Table 9. 10-pin connector J7 on the main board is not used at the current version of MPC.

Table 9

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TDO (Data from on-board device)	4	VCC
5	TMS	6	Not connected
7	Not connected	8	Not connected
9	TDI (Data from on-board device)	10	GND

J2 jumpers on the mezzanine card are intended for the JTAG chain configuration. When J2 1 and 2 are connected, there are three devices in JTAG chain (connector J7). The order of files in a chain (in Altera Max+ Programmer option) should be:

Device 1: EPC2 File name: mpcsel2.pof
Device 2: EPC2 File name: mpcsel2_1.pof
Device 3: EPF10K200EGC599 File name: mpcsel2.sof

If one or two devices are to be bypassed, the <none> should be marked instead of File name. When 2 and 3 at J2 are connected, only EPF10K200 PLD is in a JTAG loop.

J6 jumper on the main board selects VCC power (+5V when 2-3 is selected, or +3.3V when 1-2 is selected) to Altera Bit- or ByteBlaster.

J9 jumper on the main board selects VCC power (+5V when 1-2 is selected, or +3.3V when 2-3 is selected) for the device connected to J7 (not used at the moment).

J13 jumper is not used at the present configuration.

J3 jumper selects the clock source for main MPC and mezzanine boards. When 1-2, clock comes from the CCB. When 2-3, clock comes from on-board 40MHz oscillator.

8. Front panel

There are on the front panel:
- Six optical connectors to SR board
- Six red LEDs "1A, 1B, 2A, 2B, 3A, 3B" (with one-shots) indicate Flag bits of six incoming from TMB or FIFO_A muons

- Three red LEDs “SORT1-3” (with one-shots) indicate Flag bits of three output muons passing to SR and FIFO_B
- Yellow LED “TEST” indicates “Test Mode” (CSR1<0>=1) active
- Yellow LED “DTACK” (with one-shot) indicates access to MPC
- Yellow LED “JTAG” indicates an access to sorter PLD and/or two of its PROMs over JTAG cable
- Yellow LED “GEO” indicates access to MPC in geographical address mode
- Two green LEDs “+5V” and “+3.3V” indicate active on-board power.

9. How to program MPC in “Test” Mode

1. Reset MPC internal logic (write any data to E0404A address)
2. Reset FIFO buffers (write any data to E04048 address)
3. Reset G-links (write any data to E04046 address)
4. Write 0001(hex) into CSR1
5. Write 0200(hex) into CSR2
6. Write data into FIFOA_1…FIFOA_15 buffers (up to 8 words)
7. Send data from FIFOA (generate BX0 from CCB)
8. Read data representing three selected muons from FIFOB1…FIFOB9