CMS EMU Muon Port Card (MPC2004), Production Version

Specification

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Introduction

In each of stations 2-4 of the Cathode Strip Chambers (CSC) at the CMS Experiment, the Muon Port Card (MPC2004) receives up to two trigger primitives (called Local Charged Tracks, or LCT) from nine chambers corresponding to 60 degree sectors, or 18 in total. The MPC2004 reduces the number of LCTs to three and sends them over optical links to Sector Processors (SP) [1] residing in the Track Finder (TF) crate. In station 1, it receives LCT's from eight chambers corresponding to 20 degree sectors. For this region the total number of selected LCT's is two. The MPC2004 resides in the middle of the 21-slot 9U crate that is located on the periphery of the return yoke of the CMS detector. Other slots in a crate will be occupied by the Trigger Motherboards (TMB) [2], DAQ Motherboards [3], Clock and Control Board (CCB) [4] and VME controller. All modules in the crate communicate with each other over custom backplane. A simplified block diagram of the MPC2004 board is shown on Figure 1.

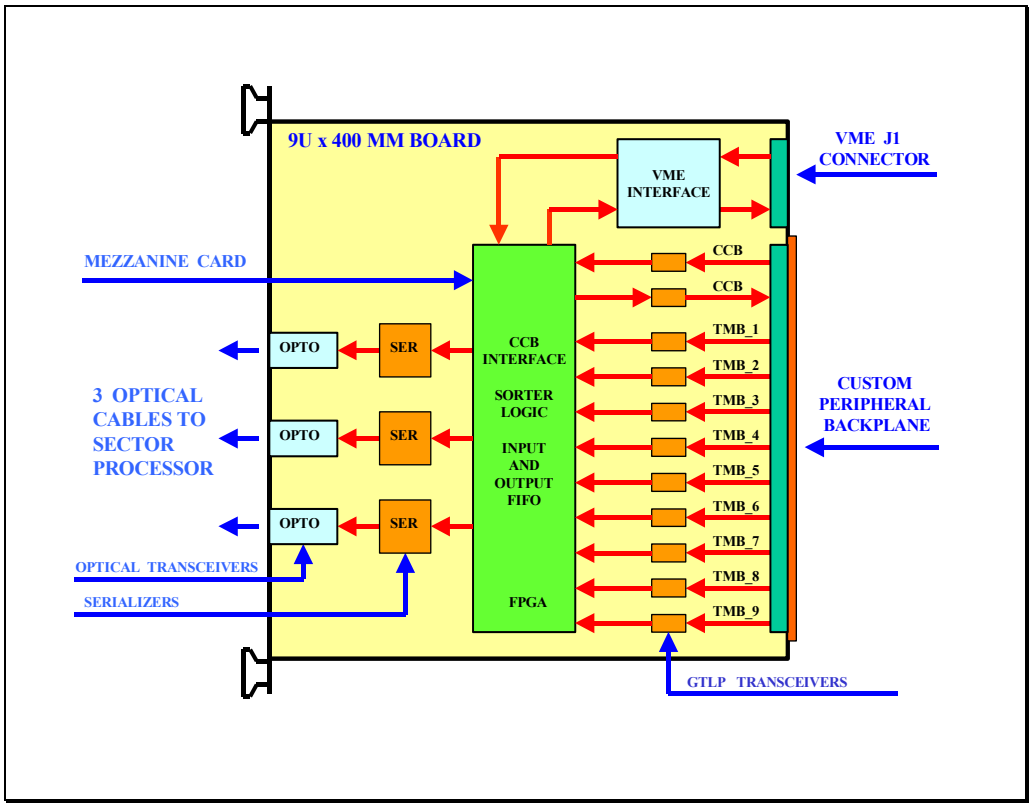

Figure1: Block Diagram of the Muon Port Card

1. Interface to Clock and Control Board

The CCB distributes several common (bussed) and individual (point-to-point) signals to each module in the peripheral crate. A full list of these signals is given in the CCB manual [4]. Its subset relevant to MPC2004 is shown in Table 1. Two clock signals, 40.08 and 80.16Mhz, are distributed from the CCB over LVDS lines. All the rest signals are transmitted using GTLP logic standard, with active level "0". The list of commands decoded by the MPC2004 is shown in Table 2.

Table 1

CCB-to-MPC Signals

Signal	Bits	Type	Logic	Duration
Ccb_clk40	1	Point-to-point	LVDS	40.08Mhz
Clk80_MPC	1	Point-to-point	LVDS	80.16Mhz
Fast Control Bus				
Ccb_clock40_enable	1	Bussed	GTLP	40.08Mhz
Ccb_cmd[5..0]	6	Bussed	GTLP	Level
Ccb_evcntres	1	Bussed	GTLP	25 ns
Ccb_bcntres	1	Bussed	GTLP	25 ns
Ccb_cmd_strobe	1	Bussed	GTLP	25 ns
Ccb_bc0	1	Bussed	GTLP	25 ns
Ccb_l1accept	1	Bussed	GTLP	25 ns
Ccb_data[7..0]	8	Bussed	GTLP	Level
Ccb_data_strobe	1	Bussed	GTLP	25 ns
Ccb_ttcrx_ready (former ccb_reserved[0])	1	Bussed	GTLP	Level
QPLL_locked (former ccb_reserved[1])	1	Bussed	GTLP	Level
Ccb_L1Reset (former ccb_reserved[4])	1	Bussed	GTLP	25 ns
Ccb_reserved[3..2]	2	Bussed	GTLP	Level
Total	26			
MPC Reload Bus				
Mpc_hard_reset	1	Point-to-point	GTLP	300 ns
Mpc_cfg_done	1	Point-to-point	GTLP	Level
Mpc_soft_reset (former Mpc_reserved[2])	1	Point-to-point	GTLP	25 ns
Mpc_reserved[1..0]	2	Point-to-point	GTLP	25 ns
Total	5			

Table 2

Commands decoded from the ccb_cmd[5..0] lines

Command	Ccb_cmd[5..0] code (hex)	Comment
BC0	1	Bunch crossing counter starts counting on the next clock tick
Start Trigger	6	
Stop Trigger	7	
L1Reset	3	Load initial value into BX counter, generate 3.2 us negative pulse on TX_EN pin of TLK2501 transmitters (IDLE mode)
Inject patterns from MPC	30	Send test patterns from the MPC FIFO_A to SP
Bunch Counter Reset	32	Load initial value into BX counter

2. Sorter Unit and Interface to Trigger Motherboard

The TMB may send to MPC2004 up to two LCTs every 25 ns. Each LCT is represented by 32 bits that are sent in two frames at 80 Mhz. The frame format is shown in Table 3. The "old" signal names in the second column are referred to initial document [5]. These names are used in Tables 4-7.

The MPC2004 sorting unit accepts 18 4-bit patterns "Quality[3..0]" that represent the "quality" of each incoming LCT and sends out three best (having the largest value of the "quality") patterns in ranked order. The LCTs with "Quality"=0 are cancelled by the sorter unit. If several patterns happen to have the same non-zero "Quality" value, then the pattern arriving from the TMB with the largest slot number in the crate will have the precedence. If two LCT from the same TMB are selected and both have the same "quality" value, then the LCT1 will have the precedence over LCT0. Selected 32-bit patterns are multiplexed into two 16-bit frames on the FPGA outputs and sent directly to TLK2501 serializers [6] in ranked order (see Section 3). Two signals (BX[0] and Sync_Er) may be added to these paths, see Section 4.1.

Table 3

TMB-to-MPC data Format (i=1..9)

		First frame transmitted at 80Mhz		Second frame transmitted at 80Mhz	
Line	**Old Name**	**Signal**	**LCT**	**Signal**	**LCT**
TMBi[0]	Lcti_vpf	Wire Group_0	0	½-strip_0	0
TMBi[1]	Lcti_qual0	Wire Group_1	0	½-strip_1	0
TMBi[2]	Lcti_qual1	Wire Group_2	0	½-strip_2	0
TMBi[3]	Lcti_qual2	Wire Group_3	0	½-strip_3	0
TMBi[4]	Lcti_qual3	Wire Group_4	0	½-strip_4	0
TMBi[5]	Lcti_qual4	Wire Group_5	0	½-strip_5	0
TMBi[6]	Lcti_qual5	Wire Group_6	0	½-strip_6	0
TMBi[7]	Lcti_qual6	CLCT Pattern_ID0	0	½-strip_7	0
TMBi[8]	Lcti_qual7	CLCT Pattern_ID1	0	L/R Bend Angle	0
TMBi[9]	Lcti_qual8	CLCT Pattern_ID2	0	SYNC_ER	0
TMBi[10]	Lcti_hs0	CLCT Pattern_ID3	0	BXN[0]	0
TMBi[11]	Lcti_hs1	Quality_0	0	BC0	0
TMBi[12]	Lcti_hs2	Quality_1	0	CSC_ID0	0
TMBi[13]	Lcti_hs3	Quality_2	0	CSC_ID1	0
TMBi[14]	Lcti_hs4	Quality_3	0	CSC_ID2	0
TMBi[15]	Lcti_hs5	Valid Pattern Flag	0	CSC_ID3	0
TMBi[16]	Lcti_hs6	Wire Group_0	1	½-strip_0	1
TMBi[17]	Lcti_hs7	Wire Group_1	1	½-strip_1	1
TMBi[18]	Lcti_wg0	Wire Group_2	1	½-strip_2	1
TMBi[19]	Lcti_wg1	Wire Group_3	1	½-strip_3	1
TMBi[20]	Lcti_wg2	Wire Group_4	1	½-strip_4	1
TMBi[21]	Lcti_wg3	Wire Group_5	1	½-strip_5	1
TMBi[22]	Lcti_wg4	Wire Group_6	1	½-strip_6	1
TMBi[23]	Lcti_wg5	CLCT Pattern_ID0	1	½-strip_7	1
TMBi[24]	Lcti_wg6	CLCT Pattern_ID1	1	L/R Bend Angle	1
TMBi[25]	Lcti_accmu	CLCT Pattern_ID2	1	SYNC_ER	1
TMBi[26]	Lcti_bx0	CLCT Pattern_ID3	1	BXN[0]	1
TMBi[27]	Lcti_bx1	Quality_0	1	BC0	1
TMBi[28]	Lcti_rsv0	Quality_1	1	CSC_ID0	1
TMBi[29]	Lcti_rsv1	Quality_2	1	CSC_ID1	1
TMBi[30]	Lcti_rsv2	Quality_3	1	CSC_ID2	1
TMBi[31]	Lcti_rsv3	Valid Pattern Flag	1	CSC_ID3	1

The MPC2004 chooses the best three out of 18 patterns it receives every 25 ns. If a particular pattern is accepted by MPC2004, then a "winner" bit is sent from MPC2004 back to corresponding TMB. The total number of "winner" bits is 18, and they are sent

back to TMB's in two 80Mhz frames. Each TMB may insert two corresponding bits into one of its streams to DMB for further monitoring. The "1" in the first frame indicates that an LCT0 from the particular TMB was accepted by the MPC2004. The "1" in the second frame indicates that the LCT1 from the particular TMB was accepted.

The input clock on MPC2004 board must be adjusted in respect to master CCB clock for reliable latching of 80Mhz data streams from all nine TMB boards into the FPGA. It can be done with CSR2[15..8] bits when CSR0[13]=0. During initial tests of the EMU peripheral crate in October 2005 it was found that for nine TMB2005 boards the "safe window" of data latching is when the CSR2[15..8]=(25…3B)h, or 5.5 ns. If CSR0[13]=1, then the clock will be set to a predefined value precisely in the middle of the "safe window" (which corresponds to CSR2[15..8]=30h). In this case there is no need to program the CSR2.

All signals from nine TMB's (32*9=288 lines) to MPC2004 as well as "winner" bits are transmitted over point-to-point lines using "negative" (active "0") GTLP logic. They are terminated (56 Ohm to +1.5V) on the MPC2004 board. Pin assignment for all four backplane connectors at the MPC slot 12 is given in Tables 4..7 (signal names and connector numbers are referred to [5]). Two sources of +1.5V power (Tables 6-7) from the custom backplane are used for GTLP termination only.

Table 4

Pin assignment of the X36 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Ccb_clk40+	B1	Ccb_clk40-	C1	GND	D1	Mpc_hreset	E1	Mpc_rsv0
A2		B2		C2	GND	D2	Mpc_rsv1	E2	Mpc_rsv2
A3		B3		C3	GND	D3		E3	Mpc_cfg_d
A4		B4		C4	GND	D4	Clk80_mpc+	E4	Clk80_mpc-
A5	Clk_enable	B5	Ccb_rsv4	C5	GND	D5		E5	
A6	Ccm_cmd0	B6	Ccb_cmd1	C6	GND	D6	Ccb_cmd2	E6	Ccb_cmd3
A7	Ccb_cmd4	B7	Ccb_cmd5	C7	GND	D7	Ccb_evcnres	E7	Ccb_bcntres
A8	Ccb_cmd_str	B8	Ccb_bx0	C8	GND	D8	Ccb_l1a	E8	Ccb_dstrobe
A9	Ccb_data0	B9	Ccb_data1	C9	GND	D9	Ccb_data2	E9	Ccb_data3
A10	Ccb_data4	B10	Ccb_data5	C10	GND	D10	Ccb_data6	E10	Ccb_data7
A11	Ccb_ttcrx_rd	B11	Ccb_rsv1	C11	GND	D11	Ccb_rsv2	E11	Ccb_rsv3
A12	Lct8_vpf	B12	Lct8_qual0	C12	GND	D12	Lct8_qual1	E12	Lct8_qual2
A13	Lct8_qual3	B13	Lct8_qual4	C13	GND	D13	Lct8_qual5	E13	Lct8_qual6
A14	Lct8_qual7	B14	Lct8_qual8	C14	GND	D14	Lct8_hs0	E14	Lct8_hs1
A15	Lct8_hs2	B15	Lct8_hs3	C15	GND	D15	Lct8_hs4	E15	Lct8_hs5
A16	Lct8_hs6	B16	Lct8_hs7	C16	GND	D16	Lct8_wg0	E16	Lct8_wg1
A17	Lct8_wg2	B17	Lct8_wg3	C17	GND	D17	Lct8_wg4	E17	Lct_wg5
A18	Lct8_wg6	B18	Lct8_accmu	C18	GND	D18	Lct8_bxn0	E18	Lct8_bc0
A19	Lct8_rsv0	B19	Lct8_rsv1	C19	GND	D19	Lct8_rsv2	E19	Lct8_rsv3
A20	Lct2_vpf	B20	Lct2_qual0	C20	GND	D20	Lct2_qual1	E20	Lct2_qual2
A21	Lct2_qual3	B21	Lct2_qual4	C21	GND	D21	Lct2_qual5	E21	Lct2_qual6
A22	Lct2_qual7	B22	Lct2_qual8	C22	GND	D22	Lct2_hs0	E22	Lct2_hs1
A23	Lct2_hs2	B23	Lct2_hs3	C23	GND	D23	Lct2_hs4	E23	Lct2_hs5
A24	Lct2_hs6	B24	Lct2_hs7	C24	GND	D24	Lct2_wg0	E24	Lct2_wg1
A25	Lct2_wg2	B25	Lct2_wg3	C25	GND	D25	Lct2_wg4	E25	Lct2_wg5

Table 5

Pin assignment of the X37 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Lct2_wg6	B1	Lct2_accmu	C1	GND	D1	Lct2_bxn0	E1	Lct2_bc0
A2	Lct2_rsv0	B2	Lct2_rsv1	C2	GND	D2	Lct2_rsv2	E2	Lct2_rsv3
A3	Lct2_winner	B3	Lct4_winner	C3	GND	D3	Lct6_winner	E3	Lct8_winner
A4	Lct6_vpf	B4	Lct6_qual0	C4	GND	D4	Lct6_qual1	E4	Lct6_qual2
A5	Lct6_qual3	B5	Lct6_qual4	C5	GND	D5	Lct6_qual5	E5	Lct6_qual6
A6	Lct6_qual7	B6	Lct6_qual8	C6	GND	D6	Lct6_hs0	E6	Lct6_hs1
A7	Lct6_hs2	B7	Lct6_hs3	C7	GND	D7	Lct6_hs4	E7	Lct6_hs5
A8	Lct6_hs6	B8	Lct6_hs7	C8	GND	D8	Lct6_wg0	E8	Lct6_wg1
A9	Lct6_wg2	B9	Lct6_wg3	C9	GND	D9	Lct6_wg4	E9	Lct6_wg5
A10	Lct6_wg6	B10	Lct6_accmu	C10	GND	D10	Lct6_bxn0	E10	Lct6_bc0
A11	Lct6_rsv0	B11	Lct6_rsv1	C11	GND	D11	Lct6_rsv2	E11	Lct6_rsv3

Table 6

Pin assignment of the X38 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Lct4_vpf	B1	Lct4_qual0	C1	GND	D1	Lct4_qual1	E1	Lct4_qual2
A2	Lct4_qual3	B2	Lct4_qual4	C2	+1.5_1	D2	Lct4_qual5	E2	Lct4_qual6
A3	Lct4_qual7	B3	Lct4_qual8	C3	GND	D3	Lct4_hs0	E3	Lct4_hs1
A4	Lct4_hs2	B4	Lct4_hs3	C4	+1.5_1	D4	Lct4_hs4	E4	Lct4_hs5
A5	Lct4_hs6	B5	Lct4_hs7	C5	GND	D5	Lct4_wg0	E5	Lct4_wg1
A6	Lct4_wg2	B6	Lct4_wg3	C6	+1.5_1	D6	Lct4_wg4	E6	Lct4_wg5
A7	Lct4_wg6	B7	Lct4_accmu	C7	GND	D7	Lct4_bxn0	E7	Lct4_bc0
A8	Lct4_rsv0	B8	Lct4_rsv1	C8	+1.5_1	D8	Lct4_rsv2	E8	Lct4_rsv3
A9	Lct5_vpf	B9	Lct5_qual0	C9	GND	D9	Lct5_qual1	E9	Lct5_qual2
A10	Lct5_qual3	B10	Lct5_qual4	C10	+1.5_1	D10	Lct5_qual5	E10	Lct5_qual6
A11	Lct5_qual7	B11	Lct5_qual8	C11	GND	D11	Lct5_hs0	E11	Lct5_hs1
A12	Lct5_hs2	B12	Lct5_hs3	C12	+1.5_1	D12	Lct5_hs4	E12	Lct5_hs5
A13	Lct5_hs6	B13	Lct5_hs7	C13	GND	D13	Lct5_wg0	E13	Lct5_wg1
A14	Lct5_wg2	B14	Lct5_wg3	C14	+1.5_1	D14	Lct5_wg4	E14	Lct5_wg5
A15	Lct5_wg6	B15	Lct5_accmu	C15	GND	D15	Lct5_bxn0	E15	Lct5_bc0
A16	Lct5_rsv0	B16	Lct5_rsv1	C16	+1.5_1	D16	Lct5_rsv2	E16	Lct5_rsv3
A17	Lct3_vpf	B17	Lct3_qual0	C17	GND	D17	Lct3_qual1	E17	Lct3_qual2
A18	Lct3_qual3	B18	Lct3_qual4	C18	+1.5_1	D18	Lct3_qual5	E18	Lct3_qual6
A19	Lct3_qual7	B19	Lct3_qual8	C19	GND	D19	Lct3_hs0	E19	Lct3_hs1
A20	Lct3_hs2	B20	Lct3_hs3	C20	+1.5_1	D20	Lct3_hs4	E20	Lct3_hs5
A21	Lct3_hs6	B21	Lct3_hs7	C21	GND	D21	Lct3_wg0	E21	Lct3_wg1
A22	Lct3_wg2	B22	Lct3_wg3	C22	+1.5_1	D22	Lct3_wg4	E22	Lct3_wg5
A23	Lct3_wg6	B23	Lct3_accmu	C23	GND	D23	Lct3_bxn0	E23	Lct3_bc0
A24	Lct3_rsv0	B24	Lct3_rsv1	C24	+1.5_1	D24	Lct3_rsv2	E24	Lct3_rsv3
A25	Lct1_winner	B25	Lct3_winner	C25	GND	D25	Lct5_winner	E25	Lct7_winner

Table 7

Pin assignment of the X39 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Lct7_vpf	B1	Lct7_qual0	C1	GND	D1	Lct7_qual1	E1	Lct7_qual2
A2	Lct7_qual3	B2	Lct7_qual4	C2	+1.5_2	D2	Lct7_qual5	E2	Lct7_qual6
A3	Lct7_qual7	B3	Lct7_qual8	C3	GND	D3	Lct7_hs0	E3	Lct7_hs1
A4	Lct7_hs2	B4	Lct7_hs3	C4	+1.5_2	D4	Lct7_hs4	E4	Lct7_hs5
A5	Lct7_hs6	B5	Lct7_hs7	C5	GND	D5	Lct7_wg0	E5	Lct7_wg1
A6	Lct7_wg2	B6	Lct7_wg3	C6	+1.5_2	D6	Lct7_wg4	E6	Lct7_wg5
A7	Lct7_wg6	B7	Lct7_accmu	C7	GND	D7	Lct7_bxn0	E7	Lct7_bc0
A8	Lct7_rsv0	B8	Lct7_rsv1	C8	+1.5_2	D8	Lct7_rsv2	E8	Lct7_rsv3
A9	Lct1_vpf	B9	Lct1_qual0	C9	GND	D9	Lct1_qual1	E9	Lct1_qual2
A10	Lct1_qual3	B10	Lct1_qual4	C10	+1.5_2	D10	Lct1_qual5	E10	Lct1_qual6
A11	Lct1_qual7	B11	Lct1_qual8	C11	GND	D11	Lct1_hs0	E11	Lct1_hs1

A12	Lct1_hs2	B12	Lct1_hs3	C12	+1.5_2	D12	Lct1_hs4	E12	Lct1_hs5
A13	Lct1_hs6	B13	Lct1_hs7	C13	GND	D13	Lct1_wg0	E13	Lct1_wg1
A14	Lct1_wg2	B14	Lct1_wg3	C14	+1.5_2	D14	Lct1_wg4	E14	Lct1_wg5
A15	Lct1_wg6	B15	Lct1_accmu	C15	GND	D15	Lct1_bxn0	E15	Lct1_bc0
A16	Lct1_rsv0	B16	Lct1_rsv1	C16	+1.5_2	D16	Lct1_rsv2	E16	Lct1_rsv3
A17	Lct9_vpf	B17	Lct9_qual0	C17	GND	D17	Lct9_qual1	E17	Lct9_qual2
A18	Lct9_qual3	B18	Lct9_qual4	C18	+1.5_2	D18	Lct9_qual5	E18	Lct9_qual6
A19	Lct9_qual7	B19	Lct9_qual8	C19	GND	D19	Lct9_hs0	E19	Lct9_hs1
A20	Lct9_hs2	B20	Lct9_hs3	C20	+1.5_2	D20	Lct9_hs4	E20	Lct9_hs5
A21	Lct9_hs6	B21	Lct9_hs7	C21	GND	D21	Lct9_wg0	E21	Lct9_wg1
A22	Lct9_wg2	B22	Lct9_wg3	C22	+1.5_2	D22	Lct9_wg4	E22	Lct9_wg5
A23	Lct9_wg6	B23	Lct9_accmu	C23	GND	D23	Lct9_bxn0	E23	Lct9_bc0
A24	Lct9_rsv0	B24	Lct9_rsv1	C24	+1.5_2	D24	Lct9_rsv2	E24	Lct9_rsv3
A25	Lct9_winner	B25		C25	GND	D25		E25	

The BC0 signal that is transmitted to the SP, is a logical OR of 9 BC0 inputs from all the TMB's; it is propagated through the MPC2004 independently from the results of sorting.

3. "Transparent" Mode of Operation

In this mode the MPC2004 may transmit any (out of 18) incoming LCT to any (out of 3) optical link without sorting. The CSR4 (see Section 6.5) defines the mode of operation and the sources for optical links in "transparent" mode. When CSR4[0]=0, the MPC2004 is in "sorter" mode. This is default state after power cycling. When CSR4[0]=1, the MPC2004 is in "transparent" mode. Then CSR4[15..1] bits specify the sources of data for optical links (see Tables 16-18). Muon_1 and Muon_2 correspond to LCT0 and LCT1 respectively from TMB1 on slot 2 in the peripheral crate (or from FIFO_A1[15..0] and FIFO_A1[31..16] respectively). Muon_3 and Muon_4 correspond to LCT0 and LCT1 respectively from TMB2 on slot 4 in the peripheral crate (or from FIFO_A2[15..0] and FIFO_A2[31..16] respectively) and so on. The LCTs with "Quality"=0 are not cancelled in "transparent" mode and will be sent to SP.

In "transparent" mode the MPC2004 generates winner bits to those TMB's, that were selected by CSR4[15..1] if "valid pattern flag" of the selected muon is "1". The order of "winner" bits is the same in both modes: if LCT0 was selected, the "winner" bit is transmitted in the first 80Mhz frame. If LCT1 was selected, the "winner" bit is transmitted in the second 80Mhz frame. The internal latency of the MPC processing is the same in both modes.

In a "sorter" mode the "vpf" bit from the first best selected muon acts as a "write enable" signal for all FIFO_B buffers. This assures that all three FIFO_B buffers will contain an equal number of words. But in "transparent" mode the "vpf" bit of every selected by CSR4[15..1] bits pattern acts as a "write enable" for its own FIFO_B buffer. So the number of words in FIFO_B buffers may be different.

4. Interface to Sector Processor

The three best patterns, or "muons" (or two in case of Station 1) selected by sorting unit are sent at 80Mhz from the processing FPGA to three 16-bit TLK2501 serializers, one

pattern per serializer. The serializer performs a parallel-to-serial data conversion with 8B/10B decoding. A serialized data is sent to Finisar FTRJ-8519-1-2.5 [7] small form factor (SFF) optical transmitters and further over ~100 m optical cables to SP located in the Track Finder crate in the counting room.

The TLK2501 serializer performs both serial-to-parallel and parallel-to-serial data conversion. The transmitter latches 16-bit parallel data at a reference clock rate and internally encodes it using 8B/10B format. The resulting 20-bit word is transmitted differentially at 20 times the reference clock frequency. The receiver section on a SP board performs a serial-to-parallel conversion on the input data, synchronizes the resulting 20-bit wide parallel word to the extracted reference clock and applies the 8B/10B decoding. The 80Mhz to 125Mhz frequency range for the reference clock allows us to transfer data at 80.16Mhz which is exactly double the LHC operating frequency of 40.08Mhz. The device has a built-in 8-bit pseudo-random bit stream generator and some other useful features such as a loss of signal detection circuit and power down mode. Parallel data, control and status pins are 3.3V compatible.

Finisar FTRJ-8519-1-2.5 2x5 pinned SFF transceivers provides bidirectional communication at data rates up to 2.125Gbps (1.6Gbps simplex mode transmission is required in our case). The laser technology is an 850 nm multimode VCSEL. It allows fiber lengths up to 300 m. The transceiver operates at extended voltages (3.15V to 3.60V) and temperature (-10C to +85C) ranges and dissipates less than 750mW. One advantage of the FTRJ-8519-1-2.5 module over similar optical transceivers available from other vendors is a metal enclosure for lower electromagnetic interference.

As described above, each selected by MPC2004 pattern comprises 32 bit. It is transmitted to SP in two 16-bit frames at 80Mhz. The frame format is shown in Table 8. It is identical to TMB-to-MPC data format. However, two signals, BX0 and ER may be generated by the MPC2004 and inserted into data stream to SP instead of or together with (using logical OR) the corresponding bits from TMB. For details see Section 4.1.

Table 8

MPC-to-SP Data Format

Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vpf	**Quality[3..0]**				**CLCT Pattern ID[3..0]**				**Wire Group ID[6..0]**						
Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip Pattern_ID[7..0]**							

CLCT Half-Strip Pattern ID is between 0 and 159
CLCT Pattern encodes the number of layers and whether the pattern consists of half-strips or di-strips
Wire Group ID is between 0 and 111 and indicates the position of the pattern within the chamber
L/R – Bend Angle Bit indicates whether the track is heading towards lower or higher strip number
VPF – Valid Pattern Flag indicates a valid LCT that has been found by TMB and being sent in the current clock cycle
ER - Synchronization Error
BX0 – The less significant bits of the Bunch Crossing Counter.
BC0 – Bunch Crossing Zero Flag arriving from the TMB

4.1. BX0 and SYER sources on MPC board

The MPC2004 maintains its own bunch crossing counter that can be set to predefined value upon arriving of the L1Reset or special "Reset Bunch Counter" broadcast commands from the CCB. This predefined value is kept in the CSR5. The bunch crossing counter starts counting on signal BC1 (next clock tick after arriving BC0 from the CCB) after receiving of "Start Trigger" broadcast command. It stops counting after receiving "Stop Trigger" broadcast command from the CCB.

The lowest bit of the bunch crossing counter may be inserted into data stream to SP instead of BXN[0] bit from the "winning" TMB. If CSR0[3]=1, then the BXN[0] from "winning" TMB's are transmitted to SP (for every link). If CSR0[3]=0, then the lowest bit of the internal bunch crossing counter on MPC2004 board is transmitted to SP (for all three links).

The MPC2004 may generate the SYNC_ER signal to be transmitted to SP. It compares the lowest bit of the its bunch crossing counter against bit BXN[0] of each winner LCT arriving from the TMB. If they mismatch and CSR0[11]=0, then the Sync_ER from this comparator will be generated. Upon arrival of the BC0 signal from the TMB the internal bunch crossing counter is checked and (if CSR0[2]=0) in case of mismatch the Sync_Er will be generated. The MPC2004 may either translate the Sync_Er from the TMB to SP (if CSR0[10]=0) or insert its own Sync_Er sources using logical "OR" for all three sources with three independent masks.

5. VME Interface

The MPC2004 can be accessed in the VME crate using geographical addressing that utilizes the address pins GA<4-0> available on the VME64x backplane. The MPC2004 resides on slot 12 of the peripheral EMU backplane, so its base geographical address is 600000(hex). The board responds to AM codes 39(hex), 3D(hex) and supports A24D16 slave operations. It does not respond to byte-addressing modes, so all valid addresses must be even numbers. Decoded addresses and VME commands are listed in Table 9. Input and Output FIFO buffers and Control and Status Registers (CSR) are described in Sections 6 and 7 respectively.

The main part of the VME interface (data drivers, address latches, address comparators, DACK response logic, CSR0) is implemented in discrete logic. This means that the board is accessible even without mezzanine card that carries the Xilinx FPGA.

Table 9

Address (hex)	Access	Function
600000	Read/Write	CSR0
600002	Write	Hard_Reset command to FPGA
600004	Write	Soft_Reset command to FPGA
600006	Write	Reset DLL in the FPGA
600080	Read/Write	FIFO_A1[15..0]. Corresponds to TMB1_LCT0

600082	Read/Write	FIFO_A1[31..16]. Corresponds to TMB1_LCT1
600084	Read/Write	FIFO_A2[15..0]. Corresponds to TMB2_LCT0
600086	Read/Write	FIFO_A2[31..16]. Corresponds to TMB2_LCT1
600088	Read/Write	FIFO_A3[15..0]. Corresponds to TMB3_LCT0
60008A	Read/Write	FIFO_A3[31..16]. Corresponds to TMB3_LCT1
60008C	Read/Write	FIFO_A4[15..0]. Corresponds to TMB4_LCT0
60008E	Read/Write	FIFO_A4[31..16]. Corresponds to TMB4_LCT1
600090	Read/Write	FIFO_A5[15..0]. Corresponds to TMB5_LCT0
600092	Read/Write	FIFO_A5[31..16]. Corresponds to TMB5_LCT1
600094	Read/Write	FIFO_A6[15..0]. Corresponds to TMB6_LCT0
600096	Read/Write	FIFO_A6[31..16]. Corresponds to TMB6_LCT1
600098	Read/Write	FIFO_A7[15..0]. Corresponds to TMB7_LCT0
60009A	Read/Write	FIFO_A7[31..16]. Corresponds to TMB7_LCT1
60009C	Read/Write	FIFO_A8[15..0]. Corresponds to TMB8_LCT0
60009E	Read/Write	FIFO_A8[31..16]. Corresponds to TMB8_LCT1
6000A0	Read/Write	FIFO_A9[15..0]. Corresponds to TMB9_LCT0
6000A2	Read/Write	FIFO_A9[31..16]. Corresponds to TMB9_LCT1
6000A4	Read/Write	FIFO_B1[15..0]. Corresponds to 1st best selected LCT
6000A6	Read/Write	FIFO_B2[15..0]. Corresponds to 2nd best selected LCT
6000A8	Read/Write	FIFO_B3[15..0]. Corresponds to 3rd best selected LCT
6000AA	Read/Write	CSR1 (date of the current firmware version)
6000AC	Read/Write	CSR2 (control)
6000AE	Read	CSR3 (FIFO Status)
6000B0	Read	L1ACC Counter
6000B2	Write	Transmit 511 words of data from all FIFO_A buffers in “Test” mode
6000B4	Write	
6000B6	Write	Send TxEn “0” pulse to all three TLK2501 transmitters
6000B8	Read/Write	CSR4 (control, “transparent” mode)
6000BA	Read/Write	CSR5 (bunch counter value)
6000BC	Read	CSR6 (access to DS2401 serial number)
6000BE		
6000C0	Write	Generate 800 us “Reset pulse” on 1-Wire bus to initialize the serial ID chip (write only)
6000C2	Write	Generate 3 us “Read pulse” on 1-Wire bus to read data from the serial ID chip (write only)
6000C4	Write	Reset CSR6 (write only)
6000C6	Write	Generate “Write-zero” 50 us pulse on 1-Wire bus to send a command to serial ID chip (write only)
6000C8	Write	Generate “Write-one” 12 us pulse on 1-Wire bus to send a command to serial ID chip (write only)
6000CA		
6000CC		
6000CE		

6. FIFO Buffers

Two groups of FIFO Buffers (FIFO_A and FIFO_B) are implemented in the main FPGA in order to test the MPC2004 internal functionality and its communications with Trigger Motherboards and Sector Processor. Both buffers are 511-word deep and available from VME for read and write (Table 8). Since two muon patterns are packed into FIFO_A in two frames, each FIFO effectively comprises 255 patterns. Each buffer represents data corresponding to one TMB board, or two muon patterns. FIFO_A1 corresponds to

TMB1, FIFO_A2 corresponds to TMB2 and so on. Its format is shown in Table 10. In a "Test" mode the test patterns representing 18 muons can be send out simultaneously from all FIFO_A buffers at 80Mhz upon specific VME command. They pass through the sorting logic that selects three best and transmits them to SP and fed into FIFO_B also at 80MHz. FIFO_B format is shown in Table 11. In a "Trigger" mode the selected patterns from TMB's act as a data sources until FIFO_B is full.

One important feature of all FIFO_B buffers is that the data from FIFO_A ("Test" mode) or TMB's ("Trigger" mode) can be saved in FIFO_B only if there is at least one valid muon pattern, or pattern with vpf=1. This allows acquiring into FIFO_B the data, representing only valid patterns. The vpf bit from the first best selected muon acts as a "write enable" signal for all FIFO_B buffers. This means that if there is just one valid pattern coming after sorting from FIFO_A or TMB, it will be stored in FIFO_B1 and "0" will be written into FIFO_B[2..3]. This assures that all three FIFO_B buffers will contain an equal number of words inside. As for VME access, any data can be loaded and read back out of any FIFO_B buffer independently.

FULL and EMPTY flags (common to all FIFO_A and FIFO_B buffers) are available for read from CSR2. After asynchronous FIFO reset all these flags are active "1".

Table 10

FIFO_A Data Format

FIFO_A Frame 1 (LCT0)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
vpf	**Quality[3..0]**				**CLCT Pattern[3..0]**				**Wire Group ID[6..0]**						
FIFO_A Frame 1 (LCT1)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
vpf	**Quality[3..0]**				**CLCT Pattern[3..0]**				**Wire Group ID[6..0]**						
FIFO_A Frame 2 (LCT0)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip ID[7..0]**							
FIFO_A Frame 2 (LCT1)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip ID[7..0]**							

Table 11

FIFO_B Data Format

FIFO_B Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vpf	**Quality[3..0]**				**CLCT Pattern ID[3..0]**				**Wire Group ID[6..0]**						
FIFO_B Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip Pattern_ID[7..0]**							

7. Control and Status Registers

The 16-bit CSR0 is implemented in discrete logic and available for write and read over VME even if the mezzanine card is not installed. Bit assignment is shown in Table 12. The other registers are implemented inside the FPGA (see Tables 13-19).

7.1. CSR0 (discrete logic)

Table 12

Bit and access	Function
0 (R/W)	FPGA_Mode (Trigger mode if "0", Test mode (FIFO_A is a source of data) if "1")
1(R/W)	Not used
2 (R/W)	MASKBC0 (Mask Sync_Er bit from the output of the comparator that checks the BX counter upon arrival of the BC0 from TMB. Enabled if "0" and disabled if "1")
3 (R/W)	MASKBX0 (BXN[0] from TMB data stream is transmitted to SP if "1". Lowest bit of internal bunch crossing counter is transmitted to SP if "0").
4 (R/W)	Not used
5 (R/W)	TDI (JTAG signal for FPGA/EPROM access)
6 (R/W)	TMS (JTAG signal for FPGA/EPROM access)
7 (R/W)	TCK (JTAG signal for FPGA/EPROM access)
8 (R)	TDO (JTAG signal for FPGA/EPROM access)
9 (R/W)	TxEn signal for TLK2501 transmitters
10 (R/W)	MASKTMB (Mask SYNC_ER bits from each winning LCTs or FIFO_A (enabled if "0" and disabled if "1")
11 (R/W)	MASKCOMP (Mask Sync_Er bit from all outputs of BXN comparators (enabled if "0" and disabled if "1")
12 (R)	FPGA Configuration Done (read only, active "1")
13 (R/W)	If "0", the input FPGA clock should be adjusted with the CSR2[15..8] If "1", the input FPGA clock is adjusted automatically in the middle of the "safe window"
14 (R/W)	Enable TLK2501 serializers. If "0", all TLK2501 are in power-down mode
15 (R/W)	PRBSEN (Enable PRBS test mode for all TLK2501 serializers)

7.2. CSR1 (FPGA, contains the date of the firmware version)

Table 13

Bit and access	Function
0 (R)	Day, LSB
1(R)	Day
2 (R)	Day
3 (R)	Day
4 (R)	Day, MSB
5 (R)	Month, LSB
6 (R)	Month
7 (R)	Month
8 (R)	Month, MSB
9 (R)	Year, LSB (*)
10 (R)	Year (*)
11 (R)	Year, MSB (*)
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

(*) The code at CSR1<11..9> should be added to 2000 to get an actual year. For example, CSR1=1252(dec) corresponds to July 4, 2002.

7.3. CSR2 (FPGA, control register)

Table 14

Bit and access	Function
0 (R/W)	When "0", all TLK2501 transmitters are in "Normal data character" mode. When "1", all TLK2501 are in IDLE mode, unless there is a Valid Pattern or BC0 from TMB
1(R/W)	Not used
2 (R/W)	Not used
3 (R/W)	Not used
4 (R/W)	Not used
5 (R/W)	Not used
6 (R/W)	Not used
7 (R/W)	Not used
8 (R/W)	Delay of the 40Mhz input clock for the FPGA, LSB (*)
9 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
10 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
11 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
12 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
13 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
14 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
15 (R/W)	Delay of the 40Mhz input clock for the FPGA, MSB (*)

(*) - 1 step = 0.25 ns. Implemented using 3D7408-0.25 programmable delay chip from Data Delay Devices

7.4. CSR3 (FPGA, FIFO status register)

Table 15

Bit and access	Function
0 (R)	FIFO_A FULL. Active "1" if at least one out of nine FIFO_A buffers is full
1(R)	FIFO_A EMPTY. Active "1" if ALL nine FIFO_A buffers are empty. Also "1" after reset
2 (R)	FIFO_B FULL. Active "1" if at least one out of three FIFO_B buffers is full
3 (R)	FIFO_B EMPTY. Active "1" if ALL three FIFO_B buffers are empty. Also "1" after reset
4 (R)	"0"
5 (R)	"0"
6 (R)	"0"
7 (R)	"0"
8 (R)	"0"
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

7.5. CSR4 (FPGA, controls the "transparent" mode)

Table 16

Bits in CSR4																Source of data to optolink 1 (1st best) and FIFO_B1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	"sorter" mode
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	All sources disabled
x	x	x	x	x	x	x	x	x	x	0	0	0	0	1	1	TMB1_LCT0
x	x	x	x	x	x	x	x	x	x	0	0	0	1	0	1	TMB1_LCT1
x	x	x	x	x	x	x	x	x	x	0	0	0	1	1	1	TMB2_LCT0
x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	1	TMB2_LCT1
x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	TMB3_LCT0
x	x	x	x	x	x	x	x	x	x	0	0	1	1	0	1	TMB3_LCT1
x	x	x	x	x	x	x	x	x	x	0	0	1	1	1	1	TMB4_LCT0
x	x	x	x	x	x	x	x	x	x	0	1	0	0	0	1	TMB4_LCT1
x	x	x	x	x	x	x	x	x	x	0	1	0	0	1	1	TMB5_LCT0
x	x	x	x	x	x	x	x	x	x	0	1	0	1	0	1	TMB5_LCT1
x	x	x	x	x	x	x	x	x	x	0	1	0	1	1	1	TMB6_LCT0
x	x	x	x	x	x	x	x	x	x	0	1	1	0	0	1	TMB6_LCT1
x	x	x	x	x	x	x	x	x	x	0	1	1	0	1	1	TMB7_LCT0
x	x	x	x	x	x	x	x	x	x	0	1	1	1	0	1	TMB7_LCT1
x	x	x	x	x	x	x	x	x	x	0	1	1	1	1	1	TMB8_LCT0
x	x	x	x	x	x	x	x	x	x	1	0	0	0	0	1	TMB8_LCT1
x	x	x	x	x	x	x	x	x	x	1	0	0	0	1	1	TMB9_LCT0
x	x	x	x	x	x	x	x	x	x	1	0	0	1	0	1	TMB9_LCT1

Table 17

Bits in CSR4																Source of data to optolink 2 (2nd best) and FIFO_B2
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	"sorter" mode
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	All sources disabled
x	x	x	x	x	0	0	0	0	1	x	x	x	x	x	1	TMB1_LCT0
x	x	x	x	x	0	0	0	1	0	x	x	x	x	x	1	TMB1_LCT1
x	x	x	x	x	0	0	0	1	1	x	x	x	x	x	1	TMB2_LCT0
x	x	x	x	x	0	0	1	0	0	x	x	x	x	x	1	TMB2_LCT1
x	x	x	x	x	0	0	1	0	1	x	x	x	x	x	1	TMB3_LCT0
x	x	x	x	x	0	0	1	1	0	x	x	x	x	x	1	TMB3_LCT1
x	x	x	x	x	0	0	1	1	1	x	x	x	x	x	1	TMB4_LCT0
x	x	x	x	x	0	1	0	0	0	x	x	x	x	x	1	TMB4_LCT1
x	x	x	x	x	0	1	0	0	1	x	x	x	x	x	1	TMB5_LCT0
x	x	x	x	x	0	1	0	1	0	x	x	x	x	x	1	TMB5_LCT1
x	x	x	x	x	0	1	0	1	1	x	x	x	x	x	1	TMB6_LCT0
x	x	x	x	x	0	1	1	0	0	x	x	x	x	x	1	TMB6_LCT1
x	x	x	x	x	0	1	1	0	1	x	x	x	x	x	1	TMB7_LCT0
x	x	x	x	x	0	1	1	1	0	x	x	x	x	x	1	TMB7_LCT1
x	x	x	x	x	0	1	1	1	1	x	x	x	x	x	1	TMB8_LCT0
x	x	x	x	x	1	0	0	0	0	x	x	x	x	x	1	TMB8_LCT1
x	x	x	x	x	1	0	0	0	1	x	x	x	x	x	1	TMB9_LCT0
x	x	x	x	x	1	0	0	1	0	x	x	x	x	x	1	TMB9_LCT1

Table 18

Bits in CSR4																Source of data to optolink 3 (3rd best) and FIFO_B3
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	"sorter" mode
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	All sources disabled
0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	1	TMB1_LCT0
0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	1	TMB1_LCT1
0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	1	TMB2_LCT0
0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	1	TMB2_LCT1
0	0	1	0	1	x	x	x	x	x	x	x	x	x	x	1	TMB3_LCT0
0	0	1	1	0	x	x	x	x	x	x	x	x	x	x	1	TMB3_LCT1
0	0	1	1	1	x	x	x	x	x	x	x	x	x	x	1	TMB4_LCT0
0	1	0	0	0	x	x	x	x	x	x	x	x	x	x	1	TMB4_LCT1
0	1	0	0	1	x	x	x	x	x	x	x	x	x	x	1	TMB5_LCT0
0	1	0	1	0	x	x	x	x	x	x	x	x	x	x	1	TMB5_LCT1
0	1	0	1	1	x	x	x	x	x	x	x	x	x	x	1	TMB6_LCT0
0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	1	TMB6_LCT1
0	1	1	0	1	x	x	x	x	x	x	x	x	x	x	1	TMB7_LCT0
0	1	1	1	0	x	x	x	x	x	x	x	x	x	x	1	TMB7_LCT1
0	1	1	1	1	x	x	x	x	x	x	x	x	x	x	1	TMB8_LCT0
1	0	0	0	0	x	x	x	x	x	x	x	x	x	x	1	TMB8_LCT1
1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	1	TMB9_LCT0
1	0	0	1	0	x	x	x	x	x	x	x	x	x	x	1	TMB9_LCT1

7.6. CSR5 (FPGA, BX counter value)

Register CSR5 contains the value, that is loaded into bunch counter register upon arrival of L1Reset broadcast command or special "Reset Bunch Counter" broadcast command (code = 32h, see Section 1) from the TTC system.

7.7. CSR6 (FPGA, access to DS2401 serial number)

Table 19

Bit	Access	Function
0	R	« 0 » indicates the « Presence pulse » from serial ID chip after the « Reset pulse »
1	R	Data bit from serial ID chip DS2401
2	R	Status of the initialization. When « 1 » after the « Reset pulse » , the CSR6[0] is valid
3	R	Status of the read cycle. When « 1 » after the « Read pulse », the CSR6[1] is valid
4	R	Status of the command cycle. When « 1 » after the « Write-one » or « Write-zero » command, the next command can be sent
5	R	« 0 »
6	R	« 0 »
7	R	« 0 »
8	R	« 0 »
9	R	« 0 »
10	R	« 0 »
11	R	« 0 »
12	R	« 0 »
13	R	« 0 »
14	R	« 0 »
15	R	« 0 »

8. Mezzanine Board and JTAG Access to FPGA and EPROM

A mezzanine card comprises one Xilinx XCV600E-8FG680C and one XC18V04 EPROM which are accessible over JTAG bus (FPGA is the first device in a JTAG chain and the EPROM is the second one). They can be accessed from Xilinx Parallel Cable IV (14-pin connector is located on the front panel) or from CSR0[8..5]. Switch S8-1 defines which of these two options is activated (Xilinx cable if S8-1 is "on" and CSR0[8..5] if S8-1 is "off")

Two clock signals for the FPGA are provided from the main MPC board. Either CCB clock obtained from the backplane or an internal 40.08Mhz clock from on-board oscillator (80.16Mhz divided by two) can be used. One of these clocks can be delayed on the main board using 3D7408-0.25 delay line [8] from Data Delay Devices. The delay value can be set using CSR2[15..8].

9. Serial Number Access

There is a Silicon Serial Number DS2401 [9] chip that consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol, read and write least significant bit first. The protocol details and timing diagrams are given in [9]. An access to serial number chip consists of three phases: Initialization, ROM Function Command, and Read Data.

The Initialization sequence consists of a "Reset pulse" transmitted by the master followed by a "Presence pulse" transmitted by the DS2401. The "Presence pulse" lets the bus master know that the DS2401 is on the bus and ready to operate. For the Initialization, the "Reset pulse" should be sent, then CSR6[2] should be checked, and, when the CSR6[2]=1, the CSR6[0] should be checked. If CSR6[0]=0 at this moment, that means that the "Presence pulse" was sent and the next step can be performed.

The ROM Function Command phase consists of sending a Read ROM command [33h] or [0Fh] to DS2401. The first bit ("Write-one") should be sent, then CSR6[4] scanned, and, when CSR6[4]=1, the next bit of command should be sent. Since all commands are 8-bit long, eight write operations are necessary.

The Read Data phase consists of 64 read cycles. Each cycle starts with sending a "Read pulse", then CSR6[3] is scanned, and, when CSR6[3]=1, the valid data bit should be received from CSR6[1]. Note the first data bit should be "1" and the next seven bits should be "0" (they represent the Family Code 01h). Bits 49-56 are also "0" and bits 57-64 represent the CRC code.

10. Fuses

Fuse F10 monitors +5V power from VME J1 backplane. Fuse F7 monitors +1.8V power for the mezzanine FPGA. Fuse F9 monitorss +2.5V power for TLK2501 transceivers. All these fuses are required at any time.

Fuse F8 monitors +3.3V power from J1 VME64x backplane while fuse F11 monitors +3.3V from on-board voltage regulator U65. Only one (either F8 or F11) fuse should be installed at a time. For VME64x backplane the F8 is required.

Fuses F1-F4 monitor reference voltages for GTLP transceivers (+1.0V) and GTLP terminators (+1.5V). Fuses F1 and F3 monitor these powers from custom backplane while F2 and F4 monitor powers from on-board voltage regulator U64. Only one pair (F1+F3 or F2+F4) should be installed at a time. If custom EMU peripheral backplane is being used, the pair of F1+F3 is required.

11. Switches

Switch S1 is needed to select the source of the master clock. If S1-1 is “on”, the source is 40.08 clock from the CCB. If S1-2 is “on”, the source is an on-board quartz oscillator (80.157 Mhz divided by 2). The default option is when S1-1 is “on”.

Switch S2 provides either master (if S2-1 is “on”) or delayed master (if S2-2 is “on”) clocks to the mezzanine FPGA. The source of this master clock is defined by S1. The delay value can be set by CSR2[15..8] with the step of 0.25 ns.

Switch S5 can be used to chose a permanent delay value for the 3D7408-0.25 delay element instead of programmable from CSR2[15..8]. Should be used for debugging purposes only.

Switch S8 is needed to chose the source of JTAG access to mezzanine FPGA. When S8-1 is “on”, the source is a JTAG cable connected over front panel. When S8-1 is “off” the CSR0[5..8] are used for JTAG access. S8-2 is needed to disable (when “on”) an on-board 80.16Mhz clock oscillator (required only for debugging purposes).

Switch S10 is used to define the A[15..8] bits of the base address. S10-1 corresponds to A8, S10-2 corresponds to A9 and so on. When any switch is set “on”, the respective bit is set to “0”. When any switch is “off”, the respective bit is set to “1”. The default option is when all S10 switches are set “on”.

S11 should be used only for debugging purposes. It allows to select the geographical addresses GA[4..0] when the VME64x backplane is not available.

S12 chooses the source of 80Mhz clock for all three TLK2501 serializers. If S12-1 is “on”, the source is an on-board oscillator. If S12-2 is “on”, the source is 80Mhz clock delivered by CCB board over backplane. If S12-3 is “on”, the source is on-board AV9170

clock generator. If S12-4 is “on”, the source is 80Mhz clock generated by the FPGA. Only one switch should be “on” at a time. It is recommended to use a direct CCB clock (S12-2 is “on”).

S13 chooses the options for 40Mhz clock generation for the FPGA. If S13-1 is “on”, the 40Mhz clock arrives from the source defined by S2. If S13-2 is “on”, the 40Mhz clock arrives from the AV9170 clock generator. Only one switch (S13-1 or S13-2) should be “on”. It is recommended to set S13-1 “on”. S13-3 and S13-4 provide a feedback input for the AV9170 clock generator. If S13-3 is “on”, the feedback input is a direct 40Mhz output from AV9170. If S13-4 is “on”, the feedback a 40Mhz output from AV9170 delayed by a clock buffer for ~2 ns. Only one switch (S13-3 or S13-4) should be “on” at a time. It is recommended to set S13-4 “on”.

12. Front Panel

There are on the front panel:

- Three optical modules for communication with the Sector Processor
- Three red LEDs “MUON[1..3] (D1-D3, with one-shots) that indicate “vpf” bits of three output patterns passing to SP and FIFO_B
- Green LED “DONE” (D4) indicates that the FPGA configuration and initialization were done properly and the DLL is locked
- Yellow LED “TEST” (D5) indicates the “Test” mode, when FIFO_A is a data source for the sorter logic
- Red LED “HRES” (D6, with one-shot) indicates the Hard_Reset command (either from CCB or from write to VME address 600002h)
- Yellow LED “TCK” (D7) indicates active TCK signal from CSR0[7]
- Yellow LED “DACK” (D9, with one-shot) indicates an access to MPC over VME
- Red LED “SRES” (D8, with one-shot) indicates the Soft_Reset command (either from VME SYSRESET line or from write to VME address 600004h)
- Green LEDs “+5V” (D18), “+3.3V” (D19), “+2.5V” (D20), “+1.8V” (D21), “+1.5VA” (D22) and “+1.5VB” (D23) indicate active on-board power supplies
- Red LED “IDLE” (D10, with one-shot) indicates that all three TLK2501 serializers are switched into IDLE mode
- Red LED “RNTS” (Run Test) (D11, with one shot) indicates that data transmission from FIFO_A buffer was initiated upon VME or CCB command
- Red LED “L1RS” (L1 Reset) (D12, with one-shot) indicates that L1 Reset command had been decoded
- Red LED “FAEM” (FIFO_A Empty) (D13) indicates that all nine FIFO_A buffers are empty
- Red LED “FBEM” (FIFO_B Empty) (D14) indicates that all three FIFO_B buffers are empty
- Red LED “FAFL” (FIFO_A Full) (D15) indicated that at least one out of nine FIFO_A buffers is full
- Red LED “FBFL” (FIFO_B Full) (D16) indicated that at least one out of three FIFO_B buffers is full

- Red LED "CLK40" (D17) indicates that the 40Mhz clock is valid (when blinking at ~5 Hz)

References

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[5] A.Madorsky. Pin assignment for the boards in the peripheral crate. Available at: http://www.phys.ufl.edu/~madorsky/backplane/PinAssignment.doc
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History

03/17/2005. Initial release.
05/16/2005. Minor changes in text.
10/20/2005. Additions to Section 2. Bit CSR0[13] was specified (Table 12).
11/24/2005. Addition to Section 2 (Transparent BC0).