Spartan-6 Muon Port Card Mezzanine for the CSC Upgrade

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Introduction

This document describes the functionality of the 2nd revision of the Spartan-6 Muon Port Card [1] mezzanine board for the CSC Upgrade at CMS. While providing all the features of the old Virtex-E mezzanine [2], the new board has an additional 12-channel optical link to allow higher data transmission to the upgraded CSC Track Finder. Simplified block diagram of the MPC2004 board with the new mezzanine as well as two pictures of the mezzanine itself (top and bottom views) are shown in Figures 1 and 2 respectively.

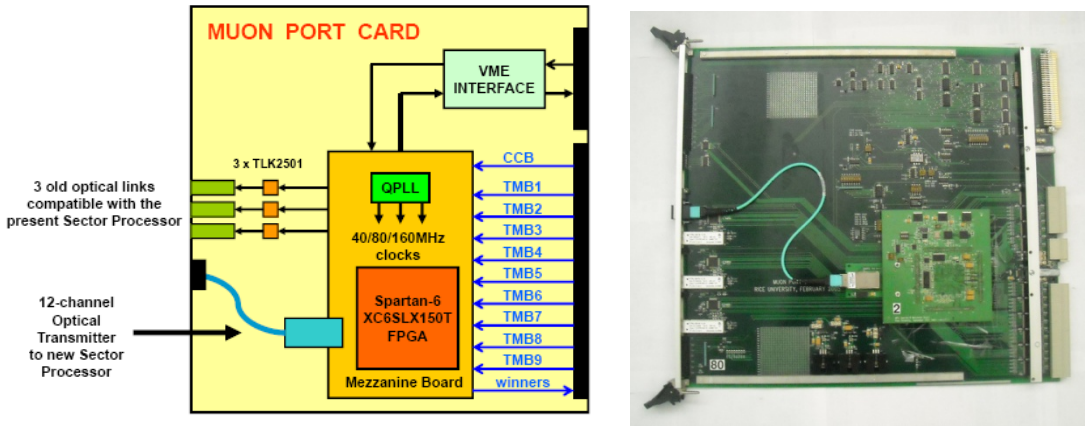


Figure 1: Block Diagram and a picture of the upgraded Muon Port Card

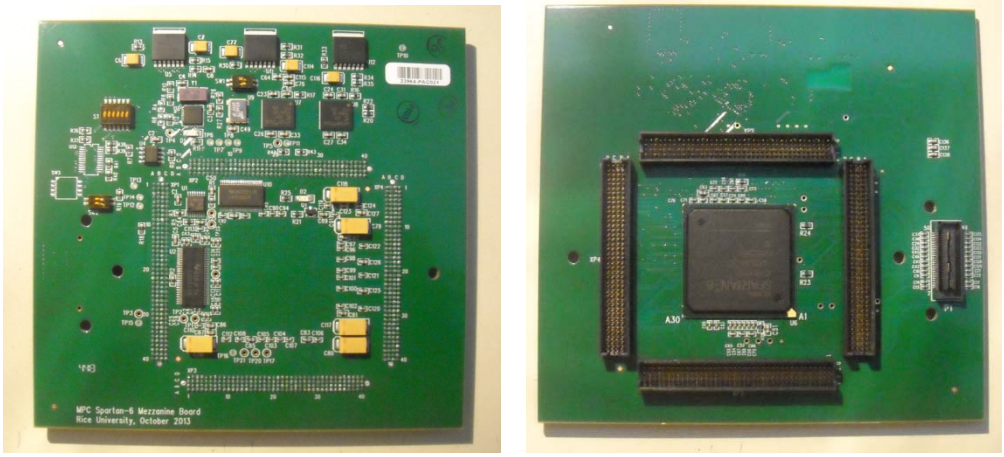


Figure 2: Spartan-6 Mezzanine Board (top and bottom views)

1. FPGA and EPROM

Xilinx XC6SLX150T-3FGG900C FPGA and two Xilinx XCF32PFSG48C PROMs reside on the mezzanine board. They are accessible via the JTAG bus either from Xilinx cable (MPC front panel) or from the VME using CSR0[8..5] bits. Switch S8-1 on the main MPC2004 board defines which of these two options is activated (Xilinx cable if S8-1 is "on" and CSR0[8..5] if S8-1 is "off"). Switch SW2 on the mezzanine board specifies the FPGA configuration mode (Table 1).

Table 1

SW2-1	SW2-2	FPGA configuration mode	M[1:0]	Data Bus width	CCLK direction
on	**on**	**Master SelectMAP (default)**	**00**	**8**	**Output**

Two XCF32P PROMs are placed in a serial chain with the FPGA (Fig.3). The FPGA may be bypassed (Table 2).

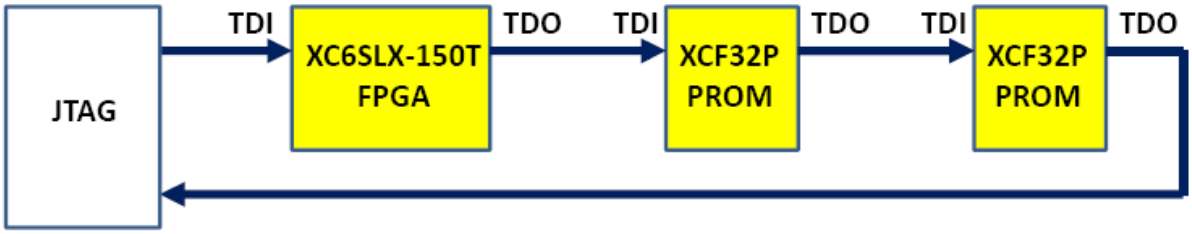


Figure 3: Default JTAG chain on the mezzanine board

Table 2

SW1-1	SW1-2	FPGA chain
off	**off**	**Do not use**
on	**off**	**PROM1 + PROM2**
off	**on**	**FPGA + PROM1 + PROM2 (default option)**
on	**on**	**Do not use**

The default configuration mode is the Master SelectMAP with the configuration clock provided by the FPGA. The **BitGen** startup clock setting is set to maximum (26MHz) in the project settings. Spartan-6 FPGA also support the ability to dynamically switch to an external clock source during master mode configuration, where faster and stable configuration times are needed. This clock comes from an external oscillator (by default, 40MHz) connected to a USERCLK input of the FPGA (pin AG16). To enable the external clock source during master mode configuration, the **ExtMasterCclk_en** option in **BitGen** must be enabled. The total amount of non-compressed configuration bits for the XC6SLX150T device is ~34 Mbits. Typical FPGA configuration times with the different clock sources are listed in Table 3.

Table 3

Clock source	Configuration time, milliseconds
FPGA internal 26MHz	**155**
External 40MHz oscillator (default mode)	**110**

All the communications between the FPGA and the main MPC2004 board are implemented via the four Samtec MOLC-140-61-L-Q-LC 4-row 140-pin elongated connectors XP1-XP4.

Their pin assignment is given in the Appendix A and is backward compatible with the previous Virtex-E mezzanine board.

2. Sorter Unit and Interface to Trigger Motherboard

The TMB can send to MPC2004 up to two Local Charged Tracks (LCT) every 25 ns. Each LCT is represented by 32 bits that are transmitted in two frames at 80 MHz. The frame format is shown in Table 1. LCTs from any TMB (or from any FIFO_A) can be masked out (disabled) using the CSR7 register. This register is implemented in the discrete logic; it can be read out via VME through the FPGA only. When disabled (CSR7(i)=0, i=0..8), the selected TMB(i) is ignored by the sorting unit of the Muon Port Card. By default (after power cycling) CSR7(15:0)="1", so all the TMBs are enabled. The MPC performs sorting at 80MHz, as described below in this section.

The sorting unit accepts 18 4-bit patterns "Quality[3..0]" that represent the "quality" of each incoming LCT. For compatibility with the original MPC2004 and CSC Track Finder designs the new Spartan-6 FPGA performs sorting "3 best LCTs out of 18" and sends the three best patterns in ranked order to the TLK2501 serializers residing on the main board.

LCTs with "Quality"=0 and "vpf"=0 are cancelled by the sorter unit. LCTs with "quality=0" and "vpf=1" do participate in sorting. If several patterns happen to have the same valid "Quality" value, then the pattern arriving from the TMB with the largest slot number in the crate will have the precedence. If two LCT from the same TMB are selected and both have the same "quality" value, then the LCT0 will have the precedence over LCT1. Selected 32-bit patterns are multiplexed into two 16-bit frames on the FPGA outputs and sent directly to TLK2501 serializers in ranked order (see Section 3).

Table 1

TMB-to-MPC data Format (i=1..9)

		First frame transmitted at 80Mhz		Second frame transmitted at 80Mhz	
Line	**Old Name**	**Signal**	**LCT**	**Signal**	**LCT**
TMBi[0]	**Lcti_vpf**	**Wire Group_0**	**0**	**½-strip_0**	**0**
TMBi[1]	**Lcti_qual0**	**Wire Group_1**	**0**	**½-strip_1**	**0**
TMBi[2]	**Lcti_qual1**	**Wire Group_2**	**0**	**½-strip_2**	**0**
TMBi[3]	**Lcti_qual2**	**Wire Group_3**	**0**	**½-strip_3**	**0**
TMBi[4]	**Lcti_qual3**	**Wire Group_4**	**0**	**½-strip_4**	**0**
TMBi[5]	**Lcti_qual4**	**Wire Group_5**	**0**	**½-strip_5**	**0**
TMBi[6]	**Lcti_qual5**	**Wire Group_6**	**0**	**½-strip_6**	**0**
TMBi[7]	**Lcti_qual6**	**CLCT Pattern_ID0**	**0**	**½-strip_7**	**0**
TMBi[8]	**Lcti_qual7**	**CLCT Pattern_ID1**	**0**	**L/R Bend Angle**	**0**
TMBi[9]	**Lcti_qual8**	**CLCT Pattern_ID2**	**0**	**SYNC_ER**	**0**
TMBi[10]	**Lcti_hs0**	**CLCT Pattern_ID3**	**0**	**BXN[0]**	**0**
TMBi[11]	**Lcti_hs1**	**Quality_0**	**0**	**BC0**	**0**
TMBi[12]	**Lcti_hs2**	**Quality_1**	**0**	**CSC_ID0**	**0**
TMBi[13]	**Lcti_hs3**	**Quality_2**	**0**	**CSC_ID1**	**0**
TMBi[14]	**Lcti_hs4**	**Quality_3**	**0**	**CSC_ID2**	**0**
TMBi[15]	**Lcti_hs5**	**Valid Pattern Flag**	**0**	**CSC_ID3**	**0**
TMBi[16]	**Lcti_hs6**	**Wire Group_0**	**1**	**½-strip_0**	**1**
TMBi[17]	**Lcti_hs7**	**Wire Group_1**	**1**	**½-strip_1**	**1**

TMBi[18]	**Lcti_wg0**	**Wire Group_2**	**1**	**½-strip_2**	**1**
TMBi[19]	**Lcti_wg1**	**Wire Group_3**	**1**	**½-strip_3**	**1**
TMBi[20]	**Lcti_wg2**	**Wire Group_4**	**1**	**½-strip_4**	**1**
TMBi[21]	**Lcti_wg3**	**Wire Group_5**	**1**	**½-strip_5**	**1**
TMBi[22]	**Lcti_wg4**	**Wire Group_6**	**1**	**½-strip_6**	**1**
TMBi[23]	**Lcti_wg5**	**CLCT Pattern_ID0**	**1**	**½-strip_7**	**1**
TMBi[24]	**Lcti_wg6**	**CLCT Pattern_ID1**	**1**	**L/R Bend Angle**	**1**
TMBi[25]	**Lcti_accmu**	**CLCT Pattern_ID2**	**1**	**SYNC_ER**	**1**
TMBi[26]	**Lcti_bx0**	**CLCT Pattern_ID3**	**1**	**BXN[0]**	**1**
TMBi[27]	**Lcti_bx1**	**Quality_0**	**1**	**BC0**	**1**
TMBi[28]	**Lcti_rsv0**	**Quality_1**	**1**	**CSC_ID0**	**1**
TMBi[29]	**Lcti_rsv1**	**Quality_2**	**1**	**CSC_ID1**	**1**
TMBi[30]	**Lcti_rsv2**	**Quality_3**	**1**	**CSC_ID2**	**1**
TMBi[31]	**Lcti_rsv3**	**Valid Pattern Flag**	**1**	**CSC_ID3**	**1**

If a particular LCT from the TMB has been accepted by MPC2004, then a “winner” bit is sent from MPC2004 back to corresponding TMB. The total number of “winner” bits is 18, and they are sent back to TMB’s in two 80Mhz frames. The “1” in the first frame indicates that an LCT0 from the particular TMB was accepted. The “1” in the second frame indicates that an LCT1was accepted.

In parallel all the 18 LCTs are multiplexed into 4 frames at 160MHz and send to eight embedded GTP serializers inside the Spartan-6 FPGA. Multiplexing scheme is shown in section 3.

3. Operation at 160MHz

At 160MHz all the incoming LCTs are transmitted to eight optical links without sorting. The serial data rate is then 3.2Gbps, 8B/10B encoding/decoding included. The data format is shown in Appendix B. Similar data format is applied to 8 FIFO_B_NEW buffers (see Section 6 for more details). Three “old” links (residing on the main MPC board) always run at 80MHz (1.6Gbps).

4. Clock Generation and Distribution

The Spartan-6 mezzanine receives the master 40.08MHz clock from the main MPC2004 board (line GCLK0). The low-jitter 160.32MHz clock for all MGT serial gigabit links is obtained by the CERN designed QPLL [3] ASIC. QPLL is a quartz crystal based Phase-Locked Loop. Its function is to act as a low-jitter filter for clock signals operating synchronously with the LHC bunch-crossing clock. The QPLL with a 160.31744MHz oscillator produces three clock signals of 160MHz, 80MHz and 40MHz (rounded values) in LVDS levels. 160Mhz clocks are delivered to the MGTREFCLK inputs of every MGT bank of the FPGA.

GCLK0 is used by default in the firmware. On the main MPC2004 board the GCLK0 must be adjusted in respect to master CCB clock for reliable latching of 80Mhz data streams from all nine TMB boards into the FPGA. CSR2[15..8] bits are used for this when CSR0[13]=0. During initial production tests of the Spartan-6 mezzanine FPGA in January 2014 it was

found that for nine TMB2005 boards residing in the peripheral EMU crate the average "safe window" of data latching is when the CSR2[15..8]=(20…34)h, or 5 ns. It may change slightly from board to board. If CSR0[13]=1, then the clock will be set to a predefined value precisely in the middle of the "safe window" (which corresponds to CSR2[15..8]=2Bh). In this case there is no need to program the CSR2.

5. Serialization and Optical Interface to the Sector Processor

The new Spartan-6 mezzanine supports both "old" 3-link and "new" 12-link optical interfaces to the present and future Sector Processors. The three best patterns, or "muons" (or two in case of Station 1) selected by sorting unit are sent at 80Mhz from the processing FPGA to three 16-bit "old" TLK2501 serializers, residing on the main MPC2004 board, one pattern per serializer. The serializer performs a parallel-to-serial data conversion with 8B/10B decoding. Serialized data is sent to Finisar FTRJ-8519-1-2.5 small form factor (SFF) optical transmitters and further over ~100 m optical cables to SP located in the Track Finder crate in the counting room.

The "new" interface allows to transmit all 18 LCTs via the eight embedded GTP links available in the Spartan-6 FPGA. The LCTs are multiplexed at 160MHz and serial data rate is 3.2Gbps per channel. The Avago AFBR-810B [4] 12-channel optical transmitter is used for communication with the SP. The other four channels are connected to regular LVDS outputs of the FPGA for future use at lower speed. The Avago device resides a small plug-in board attached to the mezzanine and facing the front panel of the MPC2004. A picture of the plug-in board with the optical transmitter attached is shown on Figure 4. Pin assignment of the 50-pin connector is given in Table 4. The mezzanine connector is a Sampec QSS-025-01-L-D-A part and the plug-in connector is a Samtec QTS-025-01-L-D-A part. Avago AFBR-810B optical module is a pluggable device. The host electrical connector is a 100 (10 x 10) position Ball Grid Array (BGA) plug available from several manufacturers; for example FCI 84512-101. Pin assignment is shown in Fig.5.

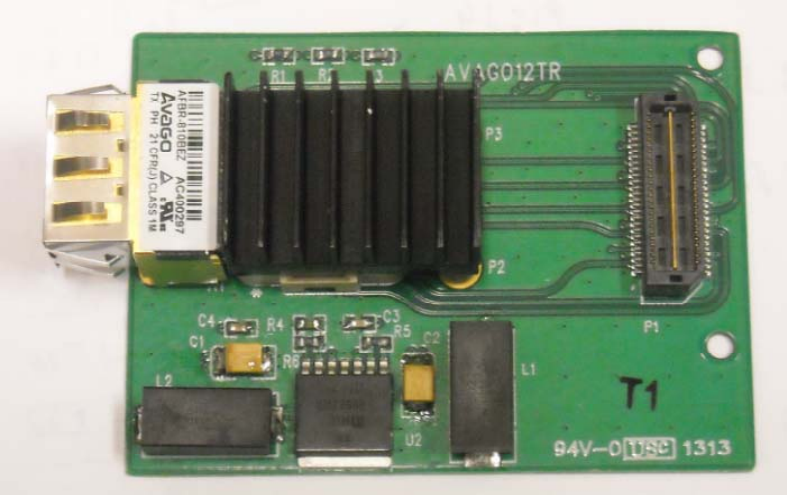


Figure 4: Avago AFBR-810B optical transmitter

Table 4

Pin	Signal	Type (w.r.t. optomodule)	Pin	Signal	Type (w.r.t. optomodule)
1	GND	Power	2	GND	Power
3	TR2+	Receiver	4	TR1-	Receiver
5	TR2-	Receiver	6	TR1+	Receiver
7	+3.3V	Power	8	+3.3V	Power
9	/FAULT[1]	Output	10	/RESET[4]	Input
11	GND	Power	12	GND	Power
13	TR3+	Receiver	14	TR0-	Receiver
15	TR3-	Receiver	16	TR0+	Receiver
17	+3.3V	Power	18	+3.3V	Power
19	+3.3V	Power	20	+3.3V	Power
21	TR11-	Receiver	22	TR6+	Receiver
23	TR11+	Receiver	24	TR6-	Receiver
25	GND	Power	26	GND	Power
27	GND	Power	28	GND	Power
29	TR10-	Receiver	30	TR7+	Receiver
31	TR10+	Receiver	32	TR7-	Receiver
33	+3.3V	Power	34	+3.3V	Power
35	+3.3V	Power	36	+3.3V	Power
37	TR9-	Receiver	38	TR4+	Receiver
39	TR9+	Receiver	40	TR4-	Receiver
41	SCL[2]	Input	42	SDA[3]	Input
43	+3.3V	Power	44	+3.3V	Power
45	TR8+	Receiver	46	TR5+	Receiver
47	TR8-	Receiver	48	TR5-	Receiver
49	GND	Power	50	GND	Power

[1] – Interrupt signal to the FPGA with a 4 kOhm pull-up.
[2] – Serial control interface; clock line with a 4 kOhm pull-up. Connected to the FPGA.
[3] – Serial control interface; data line with a 4 kOhm pull-up. Connected to the FPGA.
[4] – Module reset upon fault; HIGH = normal operation; toggle LOW to clear fault. This input is provided from the FPGA.

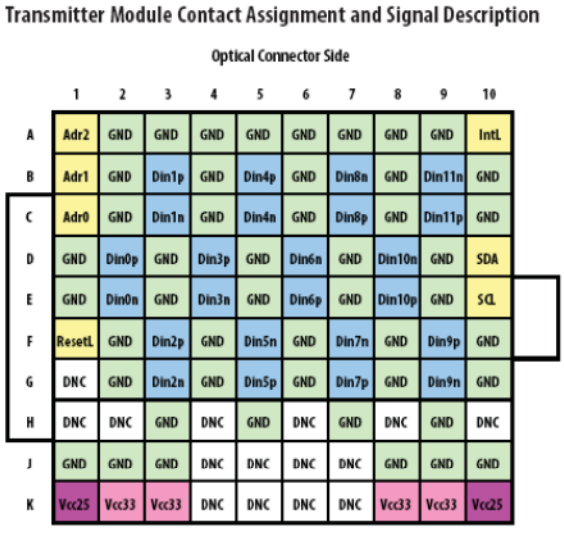


Figure 5: Host Board Pattern for the Avago AFBR-810B Transmitter

As described above, each selected by MPC2004 pattern comprises 32 bit. At 80 MHz it is transmitted to SP in two 16-bit frames. The frame format is shown in Table 5.

Table 5

MPC-to-SP Data Format ("Old" links)

Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vpf	**Quality[3..0]**				**CLCT Pattern ID[3..0]**				**Wire Group ID[6..0]**						
Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip Pattern_ID[7..0] ***							

CLCT Half-Strip Pattern ID is between 0 and 159
CLCT Pattern encodes the number of layers and whether the pattern consists of half-strips or di-strips
Wire Group ID is between 0 and 111 and indicates the position of the pattern within the chamber
L/R – Bend Angle Bit indicates whether the track is heading towards lower or higher strip number
VPF – Valid Pattern Flag indicates a valid LCT that has been found by TMB and being sent in the current clock cycle
ER - Synchronization Error
BX0 – The less significant bits of the Bunch Crossing Counter.
BC0 – Bunch Crossing Zero Flag arriving from the TMB

Upon arrival of the L1Reset command, a 3.2 us (=128 bunch crossings) pulse of negative polarity is generated on TX_EN pin of all TLK2501 serializers thus setting them into "IDLE" mode required for the periodical synchronization. Immediately after the rising edge of this pulse the unique pattern is sent on all SP links during four bunch crossings (100 ns). The pattern is sent in both frames and comprises a 6-bit Board_ID[5..0] and a Link_ID. The Board_ID[5..0] is programmable and available from the CSR0. Link_ID[1..0] is fixed in firmware. For "old" optical links it is 2-bit wide and equal to "1" for Link1 ("Muon_1"), "2" for Link2 ("Muon_2") and "3" for Link3 ("Muon_3"). For the 12 "new" optical links the Link_ID is 4-bit wide. A timing diagram is shown in Fig. 6. Data formats for the "old" and "new" links are shown in Table 6.

Note that the CSR0[9] (when "0") unconditionally sets all the serializers into "IDLE" mode. For normal operation it should be set to "1". The CSR2[0] (when "0") sets all serializers into normal data transmission mode. If CSR2[0]=1, all serializers are in "IDLE" mode unless there is a valid pattern or BC0 signal from TMB's.

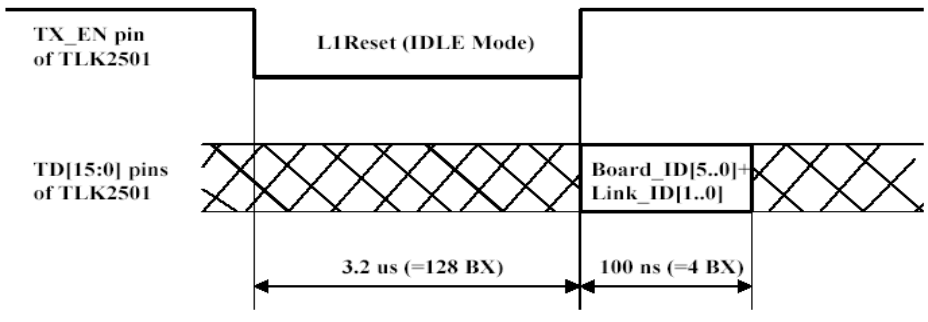


Figure 6: Timing diagram of the synchronization procedure for three "old" links

Table 6

Data formats in the "IDLE" mode

Three "old" links																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	Board_ID						Link_ID	
8 "new" links																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Board_ID						Link_ID			

6. FIFO Buffers

Two groups of FIFO Buffers (FIFO_A and FIFO_B) are implemented in the main FPGA in order to test the MPC2004 internal functionality and its communications with the Trigger Motherboards and Sector Processor. 3 FIFO_B_OLD keep the results of sorting for three old optical links. 12 FIFO_B_NEW buffers keep the output patterns for the 12 new optical links. All buffers are 511-word deep and available from VME for read and write. Since two muon patterns are packed into FIFO_A in two frames at 80MHz, each FIFO effectively comprises 255 patterns. Each buffer represents data corresponding to one TMB board, or two muon patterns. FIFO_A1 corresponds to TMB1, FIFO_A2 corresponds to TMB2 and so on. Its format is shown in Table 7. In a "Test" mode the test patterns representing 18 muons are sent out simultaneously from all FIFO_A buffers at 80Mhz upon specific TTC or VME commands. They pass through the sorting unit that selects the 3/12 best patterns and transmits them to the SP and FIFO_B_OLD buffers. FIFO_B_OLD format is shown in Table 8, same for "old" and "new" links at 80MHz. FIFO_B_NEW format is similar to data format described in Appendix B.

One important feature of all FIFO_B buffers is that the data from FIFO_A ("Test" mode) or TMB's ("Trigger" mode) can be saved in FIFO_B_OLD only if there is at least one valid muon pattern, or pattern with "vpf"=1. The "vpf" bit from the first best selected muon acts as a "write enable" signal for all FIFO_B_OLD buffers. This means that if there is just one valid pattern coming after sorting from FIFO_A or TMB, it will be stored in FIFO_B1_OLD and "0" will be written into FIFO_B[2..3]_OLD. This mechanism assures that all three FIFO_B_OLD buffers will contain an equal number of words inside. As for VME access, any data can be loaded and read back out of any FIFO_B buffer independently.

Eight FIFO_B_NEW buffers contain 18 LCTs packed in four frames. In the present implementation the data patterns are loaded to FIFO_B on a dedicated 3.2 microsecond long command (with the appropriate internal delay to prevent writing invalid "0" words into the FIFO_B_NEW) from the CCB or VME that starts data injection from FIFO_A.

FIFO_C[8:1]_NEW[15:0] allows to store data from the RX_DATA_OUT[15:0] outputs of all GTP receivers. This might be useful in the internal "loopback" mode (see CSR5).

The FULL and EMPTY flags (common to all FIFO_A and FIFO_B_OLD buffers) are available for read from CSR2. After an asynchronous FIFO reset all "EMPTY" flags are active "1" and "FULL" flags are "0".

Table 7

FIFO_A Data Format

FIFO_A Frame 1 (LCT1)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
vpf	**Quality[3..0]**				**CLCT Pattern[3..0]**				**Wire Group ID[6..0]**						
FIFO_A Frame 1 (LCT0)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
vpf	**Quality[3..0]**				**CLCT Pattern[3..0]**				**Wire Group ID[6..0]**						
FIFO_A Frame 2 (LCT1)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip ID[7..0]**							
FIFO_A Frame 2 (LCT0)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip ID[7..0]**							

Table 8

FIFO_B_OLD Data Format (80MHz)

FIFO_B Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vpf	**Quality[3..0]**				**CLCT Pattern ID[3..0]**				**Wire Group ID[6..0]**						
FIFO_B Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip Pattern_ID[7..0]**							

7. VME Interface

The MPC2004 can be accessed in the VME crate using geographical addressing that utilizes the address pins GA<4-0> available on the VME64x backplane. The MPC2004 resides on slot 12 of the peripheral EMU backplane, so its base geographical address is 600000(hex). The board responds to AM codes 39(hex), 3D(hex) and supports A24D16 slave operations. It does not respond to byte-addressing modes, so all valid addresses must be even numbers. Decoded addresses and VME commands are listed in Table 9.

The main part of the VME interface (data drivers, address latches, address comparators, DACK response logic, CSR0) is implemented in discrete logic. This means that the board is accessible even without mezzanine card that carries the Xilinx FPGA. The addresses marked in red are available for the new mezzanine only. The other VME functions are compatible with the "old" Virtex-E FPGA.

Table 9

Address (hex)	Access	Function
600000	Read/Write	CSR0 (implemented on the main MPC2004 board)
600002	Write	Hard_Reset command to FPGA (decoded on the main MPC board)
600004	Write	Soft_Reset command to FPGA (decoded on the main MPC board)
600006	Write	CSR7 (TMB mask register). Read through the FPGA, address 6000CA
600080 (0)	Read/Write	FIFO_A1[15..0]. Corresponds to TMB1_LCT1

600082 (1)	Read/Write	FIFO_A1[31..16]. Corresponds to TMB1_LCT0
600084 (2)	Read/Write	FIFO_A2[15..0]. Corresponds to TMB2_LCT1
600086 (3)	Read/Write	FIFO_A2[31..16]. Corresponds to TMB2_LCT0
600088 (4)	Read/Write	FIFO_A3[15..0]. Corresponds to TMB3_LCT1
60008A (5)	Read/Write	FIFO_A3[31..16]. Corresponds to TMB3_LCT0
60008C (6)	Read/Write	FIFO_A4[15..0]. Corresponds to TMB4_LCT1
60008E (7)	Read/Write	FIFO_A4[31..16]. Corresponds to TMB4_LCT0
600090 (8)	Read/Write	FIFO_A5[15..0]. Corresponds to TMB5_LCT1
600092 (9)	Read/Write	FIFO_A5[31..16]. Corresponds to TMB5_LCT0
600094 (10)	Read/Write	FIFO_A6[15..0]. Corresponds to TMB6_LCT1
600096 (11)	Read/Write	FIFO_A6[31..16]. Corresponds to TMB6_LCT0
600098 (12)	Read/Write	FIFO_A7[15..0]. Corresponds to TMB7_LCT1
60009A (13)	Read/Write	FIFO_A7[31..16]. Corresponds to TMB7_LCT0
60009C (14)	Read/Write	FIFO_A8[15..0]. Corresponds to TMB8_LCT1
60009E (15)	Read/Write	FIFO_A8[31..16]. Corresponds to TMB8_LCT0
6000A0 (16)	Read/Write	FIFO_A9[15..0]. Corresponds to TMB9_LCT1
6000A2 (17)	Read/Write	FIFO_A9[31..16]. Corresponds to TMB9_LCT0
6000A4 (18)	Read/Write	FIFO_B1_OLD[15..0]. Corresponds to 1st best selected LCT
6000A6 (19)	Read/Write	FIFO_B2_OLD[15..0]. Corresponds to 2nd best selected LCT
6000A8 (20)	Read/Write	FIFO_B3_OLD[15..0]. Corresponds to 3rd best selected LCT
6000AA (21)	Read	CSR1 (date of the current firmware version)
6000AC (22)	Read/Write	CSR2 (control)
6000AE (23)	Read	CSR3 (FIFO Status)
6000B0 (24)	Read	L1ACC Counter
6000B2 (25)	Write	Transmit 511 words of data from all FIFO_A buffers in “Test” mode
6000B2 (25)	Read	CSR9 (status)
6000B4 (26)	Read/Write	CSR10 (pattern to be transmitted directly to GTPs when CSR2[1]=1
6000B6 (27)	Write	Send a 3.2 us TxEn “0” pulse to all three TLK2501 transmitters
6000B8 (28)	Read/Write	CSR4 (GTP PRBS control register)
6000BA (29)	Read/Write	CSR5 (GTP control register)
6000BC (30)	Read	CSR6 (access to DS2401 serial number)
6000BE (31)	Read	CSR12 (external PRBS error counter for GTP1…GTP8; selected by CSR4[13:11])
6000C0 (32)	Write	Generate 800 us “Reset” pulse on a 1-Wire bus to initialize the DS2401
6000C2 (33)	Write	Generate 2 us “Read” pulse on a 1-Wire bus to read data from DS2401
6000C4 (34)	Write	Reset CSR6
6000C6 (35)	Write	Generate “Write-zero” 50 us pulse on a 1-Wire bus to DS2401
6000C8 (36)	Write	Generate “Write-one” 12 us pulse on a 1-Wire bus to DS2401
6000CA (37)	Read	CSR7 (readable through the FPGA only)
6000CC (38)	Write	CSR11 (reset various sources, see section 8.12 below)
6000CE (39)	Read	CSR8 (Byte alignment status of all GTPs)
6000D0 (40)	Write/Read	
6000D2 (41)	Write/Read	
6000D4 (42)	Read	FIFO_C1_NEW[15:0] (RX_DATA_OUT[15:0] from GTP1
6000D6 (43)	Read	FIFO_C2_NEW[15:0] (RX_DATA_OUT[15:0] from GTP2
6000D8 (44)	Read	FIFO_C3_NEW[15:0] (RX_DATA_OUT[15:0] from GTP3
6000DA (45)	Read	FIFO_C4_NEW[15:0] (RX_DATA_OUT[15:0] from GTP4
6000DC (46)	Read	FIFO_C5_NEW[15:0] (RX_DATA_OUT[15:0] from GTP5
6000DE (47)	Read	FIFO_C6_NEW[15:0] (RX_DATA_OUT[15:0] from GTP6
6000E0 (48)	Read	FIFO_C7_NEW[15:0] (RX_DATA_OUT[15:0] from GTP7
6000E2 (49)	Read	FIFO_C8_NEW[15:0] (RX_DATA_OUT[15:0] from GTP8
6000E4 (50)	Read/Write	FIFO_B1_NEW[15..0]
6000E6 (51)	Read/Write	FIFO_B2_NEW[15..0]
6000E8 (52)	Read/Write	FIFO_B3_NEW[15..0]

6000EA (53)	Read/Write	FIFO_B4_NEW[15..0]
6000EC (54)	Read/Write	FIFO_B5_NEW[15..0]
6000EE (55)	Read/Write	FIFO_B6_NEW[15..0]
6000F0 (56)	Read/Write	FIFO_B7_NEW[15..0]
6000F2 (57)	Read/Write	FIFO_B8_NEW[15..0]
6000F4 (58)	Write	Reset DCM producing adjustable 160Mhz and 320MHz clocks for all GTPs
6000F6 (59)	Write	PSEN input of the DCM producing an adjustable 160MHz and 320MHz clocks for all GTPs
6000F8 (60)	Write	Generate positive pulse on RXSLIDE pin of all GTPs
6000FA (61)	R.W	
6000FC (62)	R/W	
6000FE (63)	R/W	
6000FE (63)	R/W	

8. Control and Status Registers

The 16-bit CSR0 is implemented in a discrete logic on the main MPC2004 board and available for write and read over VME even if the mezzanine card is not installed. Bit assignment is shown in Table 11. The other registers are implemented inside the FPGA (see Tables 10-20).

8.1. CSR0 (600000h, discrete logic, main MPC2004 board)

Table 10

Bit and access	Function
0 (R/W)	FPGA_Mode (Trigger mode if "0", Test mode (FIFO_A is a source of data) if "1")
1(R/W)	Board_ID[0]
2 (R/W)	Board_ID[1]
3 (R/W)	Board_ID[2]
4 (R/W)	Board_ID[3]
5 (R/W)	TDI (JTAG signal for FPGA/EPROM access)
6 (R/W)	TMS (JTAG signal for FPGA/EPROM access)
7 (R/W)	TCK (JTAG signal for FPGA/EPROM access)
8 (R)	TDO (JTAG signal for FPGA/EPROM access)
9 (R/W)	TxEn signal for TLK2501 transmitters ("1" for normal data transfer mode)
10 (R/W)	Board_ID[4]
11 (R/W)	Board_ID[5]
12 (R)	FPGA Configuration Done (read only, active "1")
13 (R/W)	If "0", the input FPGA clock should be adjusted with the CSR2[15..8] If "1", the input FPGA clock is adjusted automatically in the middle of the "safe window"
14 (R/W)	Enable TLK2501 serializers when "1". If "0", all TLK2501 are in power-down mode
15 (R/W)	PRBSEN (Enable PRBS test mode for all TLK2501 serializers when "1")

8.2. CSR1 (6000AAh, FPGA, contains the date of the firmware version)

Table 11

Bit and access	Function
0 (R)	Day, LSB
1(R)	Day
2 (R)	Day
3 (R)	Day

4 (R)	Day, MSB
5 (R)	Month, LSB
6 (R)	Month
7 (R)	Month
8 (R)	Month, MSB
9 (R)	Year, LSB (*)
10 (R)	Year
11 (R)	Year
12 (R)	Year, MSB (*)
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

(*) The code at CSR1<11..9> should be added to 2000 to get an actual year. For example, CSR1=1507(hex) corresponds to August 7, 2010.

8.3. CSR2 (6000ACh, FPGA, control register, by default set to "0")

Table 12

Bit and access	Function
0 (R/W)	When "0", all TLK2501 transmitters are in "Normal data character" mode. When "1", all TLK2501 are in IDLE mode, unless there is a Valid Pattern or BC0 from TMB
1(R/W)	When "1", the pattern from the CSR10 is directly transmitted to TX_DATAIN[15:0] lines of all GTPs
2 (R/W)	Allows to increase (when "1") and decrease (when "0") the phase shift of the 160Mhz and 320Mhz clocks by writing any data "n" times to address 6000F6h.
3 (R/W)	Not used
4 (R/W)	Not used
5 (R/W)	Not used
6 (R/W)	Not used
7 (R/W)	Not used
8 (R/W)	Delay of the 40Mhz input clock for the FPGA, LSB (*)
9 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
10 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
11 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
12 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
13 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
14 (R/W)	Delay of the 40Mhz input clock for the FPGA (*)
15 (R/W)	Delay of the 40Mhz input clock for the FPGA, MSB (*)

(*) - 1 step = 0.25 ns. Implemented using 3D7408-0.25 programmable delay chip from Data Delay Devices

8.4. CSR3 (6000AEh, FPGA, FIFO status register)

Table 13

Bit and access	Function
0 (R)	FIFO_A FULL. Active "1" if at least one out of nine FIFO_A buffers is full
1(R)	FIFO_A EMPTY. Active "1" if ALL nine FIFO_A buffers are empty. Also "1" after reset
2 (R)	FIFO_B_OLD FULL. Active "1" if at least one out of three FIFO_B buffers is full
3 (R)	FIFO_B_OLD EMPTY. Active "1" if ALL three FIFO_B buffers are empty. Also "1" after reset
4 (R)	"0"
5 (R)	"0"
6 (R)	"0"
7 (R)	"0"

8 (R)	“0”
9 (R)	“0”
10 (R)	“0”
11 (R)	“0”
12 (R)	“0”
13 (R)	“0”
14 (R)	“0”
15 (R)	“0”

8.5. CSR4 (6000B8h, GTP PRBS Control Register)

Table 14

Bit	Access	Function	
0	R/W	-	
1	R/W	RXENPRBSTST0/1[0]_IN, all GTPs	**000**: standard operation mode; **001**: PRBS-7; **010**: PRBS-15; **011**: PRBS-23; **100**: PRBS-31; **101**: PCI; **110**: square wave with 2UI period; **111**: square wave with 16UI/20UI period
2	R/W	RXENPRBSTST0/1[1]_IN, all GTPs	
3	R/W	RXENPRBSTST0/1[2]_IN, all GTPs	
4	R/W	TXENPRBSTST0/1[0]_IN, all GTPs	**000**: standard operation mode; **001**: PRBS-7; **010**: PRBS-15; **011**: PRBS-23; **100**: PRBS-31; **101**: PCI; **110**: square wave with 2UI period; **111**: square wave with 16UI/20UI period
5	R/W	TXENPRBSTST0/1[1]_IN, all GTPs	
6	R/W	TXENPRBSTST0/1[2]_IN, all GTPs	
7	R/W	RXEQMIX0/1[0]_IN, all GTPs	
8	R/W	RXEQMIX0/1[1]_IN, all GTPs	
9	R/W	-	
10	R/W	-	
11	R/W	Select PRBS external error counter for read	000: counter from GTP1; 001: counter from GTP2; 010: counter from GTP3; 011: counter from GTP4; 100: counter from GTP5; 001: counter from GTP6; 110: counter from GTP7; 111: counter from GTP8;
12	R/W	Select PRBS external error counter for read	
13	R/W	Select PRBS external error counter for read	
14	R/W	TXPRBSFORCEER0/1_IN, all GTPs	
15	R/W	-	

8.6. CSR5 (6000BAh, GTP Control Register)

Table 15

Bit	Access	Function	
0	R/W	RXENMCOMMAALIGNE0/1, all GTPs	
1	R/W	RXENPCOMMAALIGNE0/1, all GTPs	
2	R/W	RXENPMAPHASEALIGN0/1_IN, all GTPs (version with TX buffer disabled)	
3	R/W	RXPMASETPHASE0/1_IN, all GTPs (version with TX buffer disabled)	
4	R/W	TXENPMAPHASEALIGN0/1_IN, all GTPs (version with TX buffer disabled)	
5	R/W	TXPMASETPHASE0/1_IN, all GTPs (version with TX buffer disabled)	
6	R/W		
7	R/W	TXCHARISK0/1[0]_IN, all GTPs	
8	R/W	TXCHARISK0/1[1]_IN, all GTPs	
9	R/W	LOOPBACK0/1[0]_IN, all GTPs	**000**: normal operation; **001**: near-end PCS loopback; **010**: near-end PMA loopback; **011**: reserved; **100**: far-end PMA loopback; **101**: reserved; **110**: far-end PCS loopback
10	R/W	LOOPBACK0/1[1]_IN, all GTPs	
11	R/W	LOOPBACK0/1[2]_IN, all GTPs	
12	R/W	-	
13	R/W	-	
14	R/W	-	
15	R/W	-	

8.7. CSR6 (6000BCh, access to DS2401 serial number)

Table 16

Bit	Access	Function
0	R	“0” indicates the “Presence” pulse from the DS2401 after the “Reset” pulse
1	R	Data bit from DS2401
2	R	Status of the initialization. When “1” after the “Reset” pulse, the CSR6[0] is valid.
3	R	Status of the read cycle. When “1” after the “Read” pulse, the CSR6[1] is valid.
4	R	Status of the command cycle. When “1” after the “Write-one” or “Write-zero” command, the next command can be sent
5	R	“0”
6	R	“0”
7	R	“0”
8	R	“0”
9	R	“0”
10	R	“0”
11	R	“0”
12	R	“0”
13	R	“0”
14	R	“0”
15	R	“0”

8.8. CSR7 (6000CAh, discrete logic; readable through the FPGA)

Table 17

Bit	Access	Function
0	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB1
1	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB2
2	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB3
3	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB4
4	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB5
5	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB6
6	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB7
7	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB8
8	R/W	Enable (if « 1 ») or Disable (if « 0 ») TMB9
9	R/W	-
10	R/W	-
11	R/W	-
12	R/W	-
13	R/W	-
14	R/W	-
15	R/W	-

8.9. CSR8 (6000CEh, FPGA, GTP status register, read only)

Table 18

Bit	Access	Function
0	R	RXBYTEISALIGNED0_OUT output of GTP1
1	R	RXBYTEALIGNE0_OUT output of GTP1
2	R	RXCOMMADET0 latched output of GTP1
3	R	« 0 »
4	R	RXBYTEISALIGNED0_OUT output of GTP2
5	R	RXBYTEALIGNE0_OUT output of GTP2
6	R	RXCOMMADET0 latched output of GTP2
7	R	« 0 »

8	R	RXBYTEISALIGNED0_OUT output of GTP3
9	R	RXBYTEALIGNE0_OUT output of GTP3
10	R	RXCOMMADET0 latched output of GTP3
11	R	« 0 »
12	R	RXBYTEISALIGNED0_OUT output of GTP4
13	R	RXBYTEALIGNE0_OUT output of GTP4
14	R	RXCOMMADET0 latched output of GTP4
15	R	« 0 »

8.10. CSR9 (6000B2h, FPGA, status register, read only)

Table 19

Bit	Access	Function
0	R	QPLL_LOCKED status (160MHz clock); “1” = locked
1	R	INTL signal from the optical transmitter board
2	R	SEU error status from the QPLL (“1” – error)
3	R	All internal DCM blocks are locked (active « 1 »)
4	R	QPLL_LOCKED error counter bit[0]
5	R	QPLL_LOCKED error counter bit[1]
6	R	QPLL_LOCKED error counter bit[2]
7	R	QPLL_LOCKED error counter bit[3]
8	R	RESETDONE status output of DCM1
9	R	RESETDONE status output of DCM2
10	R	RESETDONE status output of DCM3
11	R	RESETDONE status output of DCM4
12	R	PLLKDET status output of DCM1
13	R	PLLKDET status output of DCM2
14	R	PLLKDET status output of DCM3
15	R	PLLKDET status output of DCM4

8.11. CSR10 **(6000B4h, FPGA, pattern to be transmitted to GTP TX_DATAIN[15:0] use idle pattern=50BCh)**

8.12. CSR11 (6000CCh, FPGA, reset various sources, write only)

Table 20

Bit	Access	Function
0	W	If “1” reset external PRBS error counters
1	W	If ‘1” reset GTP internal PRBS error counters
2	W	If “1” reset all GTP receivers
3	W	If « 1 » reset all GTP transmitters
4	W	If « 1 » reset all GTP blocks
5	W	If « 1 » reset COMMADETECT latches
6	W	If « 1 » reset QPLL
7	W	n/a
8	W	n/a
9	W	n/a
10	W	n/a
11	W	n/a
12	W	n/a
13	W	n/a
14	W	n/a
15	W	n/a

8.13. CSR12 (6000BEh, FPGA, read only, external PRBS counter from GTP1...GTP8)

9. Power distribution and power regulators

The sources of power for the mezzanine components are listed in Table 21 below.

Table 21

Voltage	Source	Load(s)
+3.3V	Main MPC2004 board through 30 pins in XP1…XP4	FPGA: VCCAUX, VCCO; CMOS logic, XCF32P PROMs, voltage regulators
+2.5VC	Micrel MIC69502 voltage regulator (U5)	QPLL
+1.2VGTP	Micrel MIC69502 voltage regulator (U11)	MGT power pins, 4 banks
+1.8V	Main MPC2004 board through 20 pins in XP1…XP4	XCF32P PROMs
+1.2VINT	Micrel MIC69502 voltage regulator (U12)	FPGA core (31 VCCINT pins)

Power consumption of the main MPC2004 with the Spartan-6 mezzanine FPGA installed and functional firmware is ~1A@5V and ~3A@3.3V. For comparison, with the old Virtex-E mezzanine FPGA, the numbers are ~1.5A@5V and ~1A@3.3V.

10. Switches and Jumpers

2-position switch SW1: see Section 1, Table 2. Default state: SW1-1 “off”, SW1-2 “on”.

2-position switch SW2: see Section 1, Table 1. Default state: SW2-1 “on”, SW2-2 “on”.

6-position switch S1 (default state all “off”):

- S1-1 “on”: connect SEL0 of both QPLLs to +2.5V; S1-1 “off”: SEL0 has an internal pull-down;
- S1-2 “on”: connect SEL1 of both QPLLs to +2.5V; S1-2 “off”: SEL1 has an internal pull-down;
- S1-3 “on”: connect SEL2 of both QPLLs to +2.5V; S1-3 “off”: SEL2 has an internal pull-down;
- S1-4 “on”: connect SEL3 of both QPLLs to GND; S1-4 “off”: SEL3 has an internal pull-up;
- S1-5 “on”: connect SEL4/Restart of both QPLLs to GND; S1-5 “off”: SEL4/Restart has an internal pull-up;
- S1-6 “on”: 160MHz clock for GTPs comes from the FPGA or CDC5801A clock multiplier; S1-6 “off”: 160MHz clock for GTPs comes from the QPLL.

11. Serial Number Access

There is a Silicon Serial Number DS2401 [5] chip that consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the 1-Wire protocol, read and write least significant bit first. The protocol details and timing diagrams are given in [5]. Access to serial number chip consists of three phases: Initialization, ROM Function Command, and Read Data.

The Initialization sequence consists of a “Reset pulse” transmitted by the master followed by a “Presence pulse” transmitted by the DS2401. The “Presence pulse” lets the bus master know that the DS2401 is on the bus and ready to operate. For the Initialization, the “Reset pulse” should be sent, then CSR6[2] should be checked, and, when the CSR6[2]=1, the CSR6[0] should be checked. If CSR6[0]=0 at this moment, that means that the “Presence pulse” was sent and the next step can be performed.

The ROM Function Command phase consists of sending a Read ROM command [33h] or [0Fh] to DS2401. The first bit (“Write-one”) should be sent, then CSR6[4] scanned, and, when CSR6[4]=1, the next bit of command should be sent. Since all commands are 8-bit long, eight write operations are necessary.

The Read Data phase consists of 64 read cycles. Each cycle starts with sending a “Read pulse”, then CSR6[3] is scanned, and, when CSR6[3]=1, the valid data bit should be received from CSR6[1]. Note the first data bit should be “1” and the next seven bits should be “0” (they represent the Family Code 01h). Bits 49-56 are also “0” and bits 57-64 represent the CRC code.

12. Test Points

Test points on the mezzanine card are described below in the Table 22.

Table 22

TP1	CLK160 Clock output, LVDS positive, not terminated
TP2	CLK160 Clock output, LVDS negative, not terminated
TP3	CLK80 Clock 80MHz to the main MPC2004 board (IO_76)
TP4	QPLL_RESET signal from the FPGA
TP5	40MHz clock from the main MPC2004 board (GCLK0)
TP6	TMS JTAG signal
TP7	TCK JTAG signal
TP8	TDO JTAG signal (output from PROM)
TP9	TDI JTAG signal (input to either FPGA or first PROM)
TP10	GND
TP11	PROGRAM_B
TP12	CLK40 40MHz clock output to the main MPC2004 board (IO_54)
TP13	CLK80 80MHz clock output to the main MPC2004 board (IO_22)
TP14	CLK160 160MHz clock output to the main MPC2004 board (IO_46)
TP15	RUNTEST output to the main MPC2004 board (IO_78)
TP16	CLK320 320MHz clock output of the FPGA
TP17	FPGA pin V7 (IO_L21N_3)
TP20	FPGA pin AA3 (IO_L41P_GCLK27_M3DQ4_3)
TP21	FPGA pin AB1 (IO_L42N_GCLK24_M3LDM_3)
TP22	FPGA pin AK29 (IO_L61N_1)
TP23	FPGA pin AJ29 (IO_61P_1)

13. Front Panel and LEDs

There are on the front panel:

- Three optical modules for communication with the Sector Processor
- One 12-channel Avago AFBR-810 optical transmitter
- Three red LEDs “MUON[1..3] (D1-D3, with one-shots) that indicate “vpf” bits of three output patterns passing to SP and FIFO_B
- Green LED “DONE” (D4) indicates that the FPGA configuration and initialization were done properly and the DLL is locked
- Yellow LED “TEST” (D5) indicates the “Test” mode, when FIFO_A is a data source for the sorter logic
- Red LED “HRES” (D6, with one-shot) indicates the Hard_Reset command (either from CCB or from write to VME address 600002h)
- Yellow LED “TCK” (D7) indicates active TCK signal from CSR0[7]
- Yellow LED “DACK” (D9, with one-shot) indicates an access to MPC over VME
- Red LED “SRES” (D8, with one-shot) indicates the Soft_Reset command (either from VME SYSRESET line or from write to VME address 600004h)
- Green LEDs “+5V” (D18), “+3.3V” (D19), “+2.5V” (D20), “+1.8V” (D21), “+1.5VA” (D22) and “+1.5VB” (D23) indicate active on-board power supplies
- Red LED “IDLE” (D10, with one-shot) indicates that all three TLK2501 serializers are switched into IDLE mode
- Red LED “RNTS” (D11, with one shot) indicates that the QPLL on Spartan-6 mezzanine card is locked
- Red LED “L1RS” (L1 Reset) (D12, with one-shot) indicates that L1 Reset command had been decoded
- Red LED “FAEM” (FIFO_A Empty) (D13) indicates that all nine FIFO_A buffers are empty
- Red LED “FBEM” (FIFO_B Empty) (D14) indicates that all three FIFO_B buffers are empty
- Red LED “FAFL” (FIFO_A Full) (D15) indicated that at least one out of nine FIFO_A buffers is full
- Red LED “FBFL” (FIFO_B Full) (D16) indicated that at least one out of three FIFO_B buffers is full
- Red LED “CLK40” (D17) indicates that the 40Mhz clock is valid (when blinking at ~5 Hz)

References

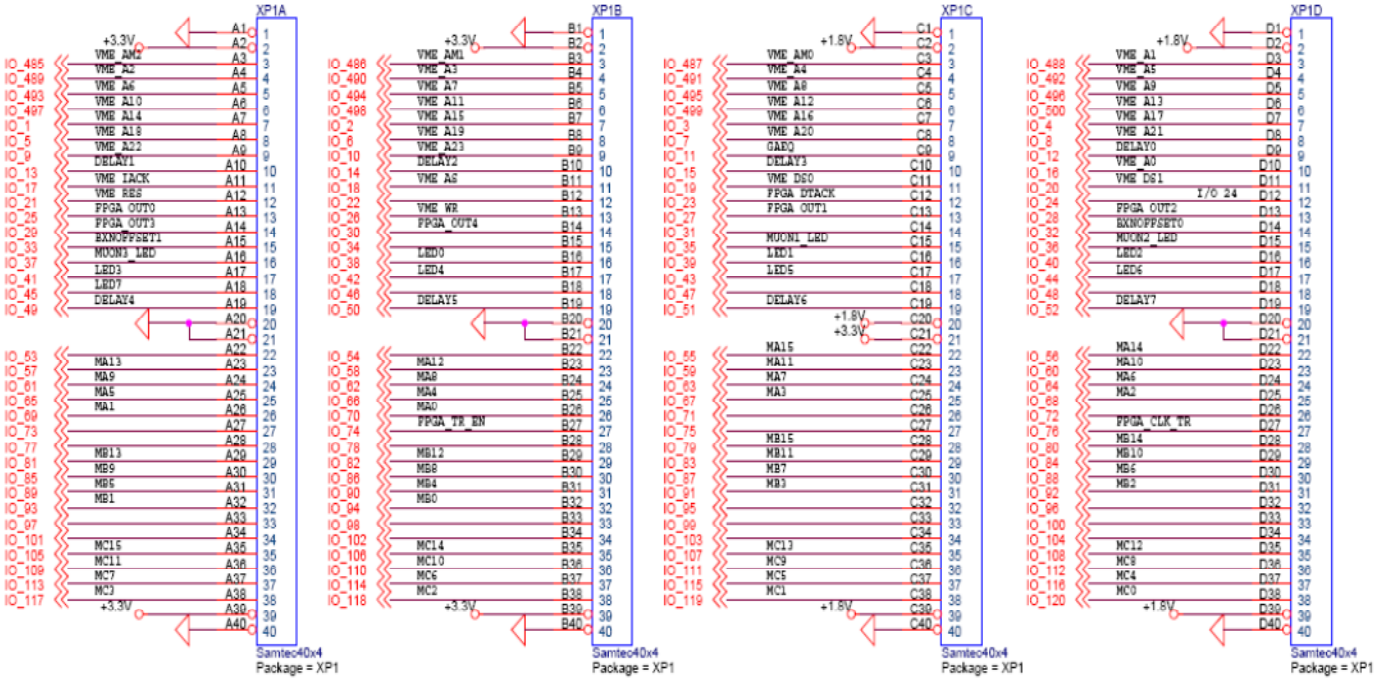
[1] http://bonner-ntserver.rice.edu/cms/projects.html#mpc
[2] http://bonner-ntserver.rice.edu/cms/MC_AST.pdf
[3] http://bonner-ntserver.rice.edu/cms/qpllManual13.pdf
[4] http://www.avagotech.com/pages/en/fiber_optics/parallel_optics/12-channel_parallel_optics/afbr-810bxxxz/
[5]. DS2401 Silicon Serial Number Specification. Available at http://pdfserv.maxim-ic.com/en/ds/DS2401.pdf

History

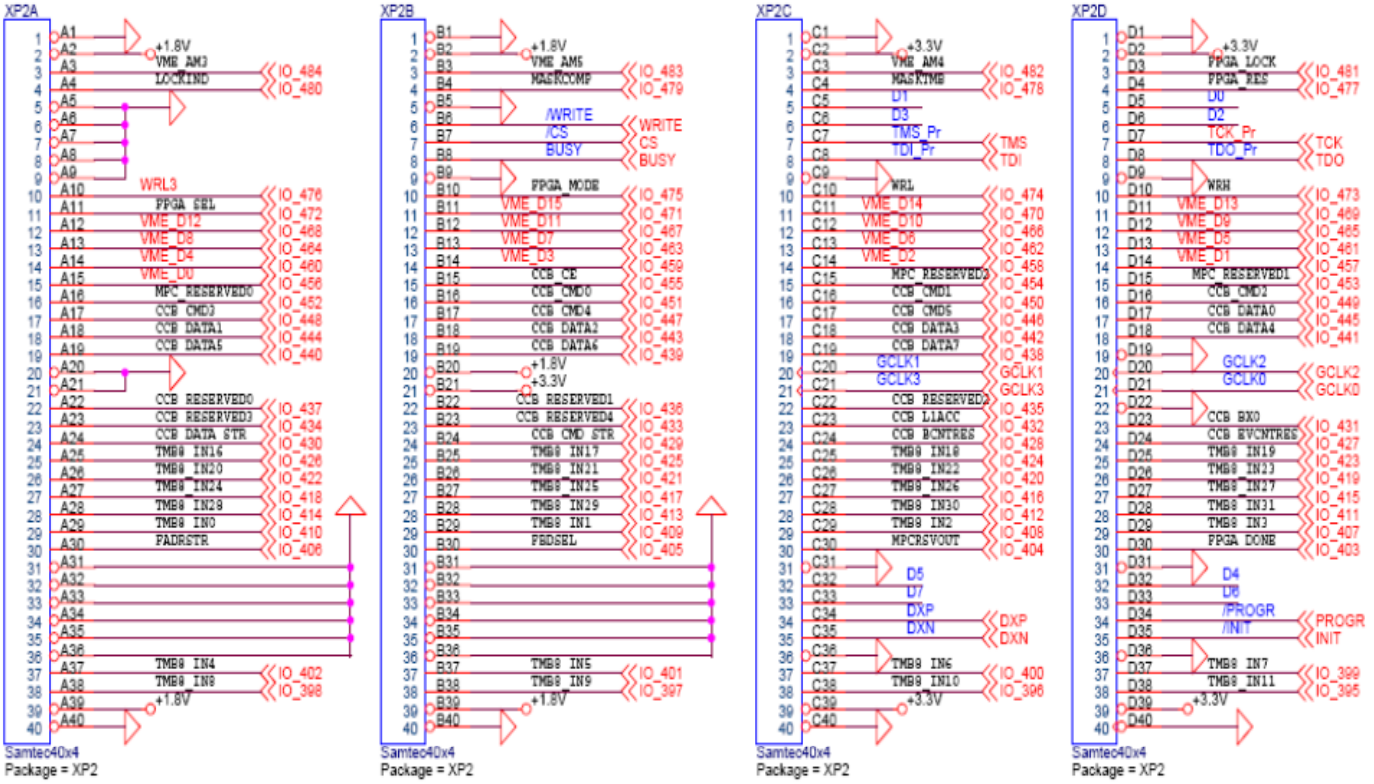
03/14/2012. Initial release.
04/09/2012. CSR6 and CSR2[1] added.
04/24/2012. PRBS error counters added. Minor changes in register addresses. CSR2[2] added.
05/15/2012. Addition to Appendix B (data format for ME2/3/4 chambers)
10/19/2012. Major changes for the revision 2 of Spartan-6 mezzanine (new connectors; new data format for optical links).
08/23/13. Major revision in VME commands. New (unified) data format for communication with the SP (Appendix B).
01/17/2004. Update of the Section 1. CSR9[7:4] have been changed; now assigned to lowest 4 bits of the QPLL_LOCKED error counter.
04/09/2014. Update of Tables 3 and 17.

Appendix A

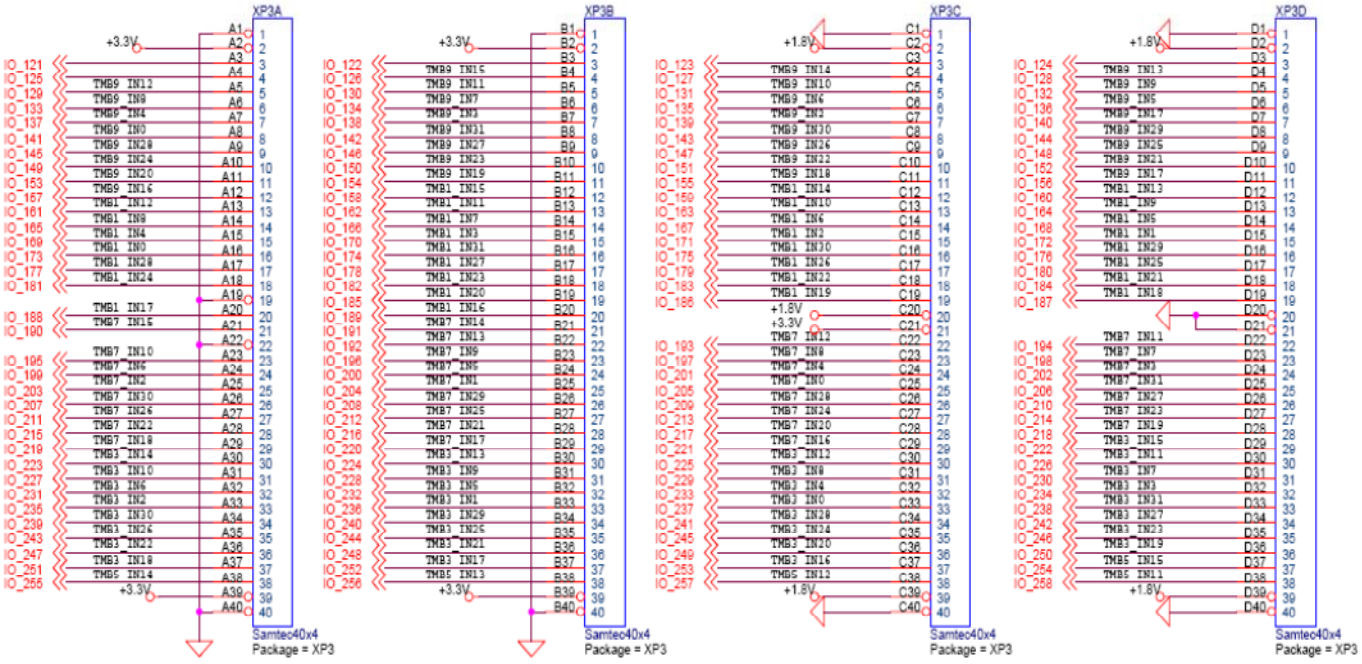
Pin assignment of XP1 mezzanine connector (left)



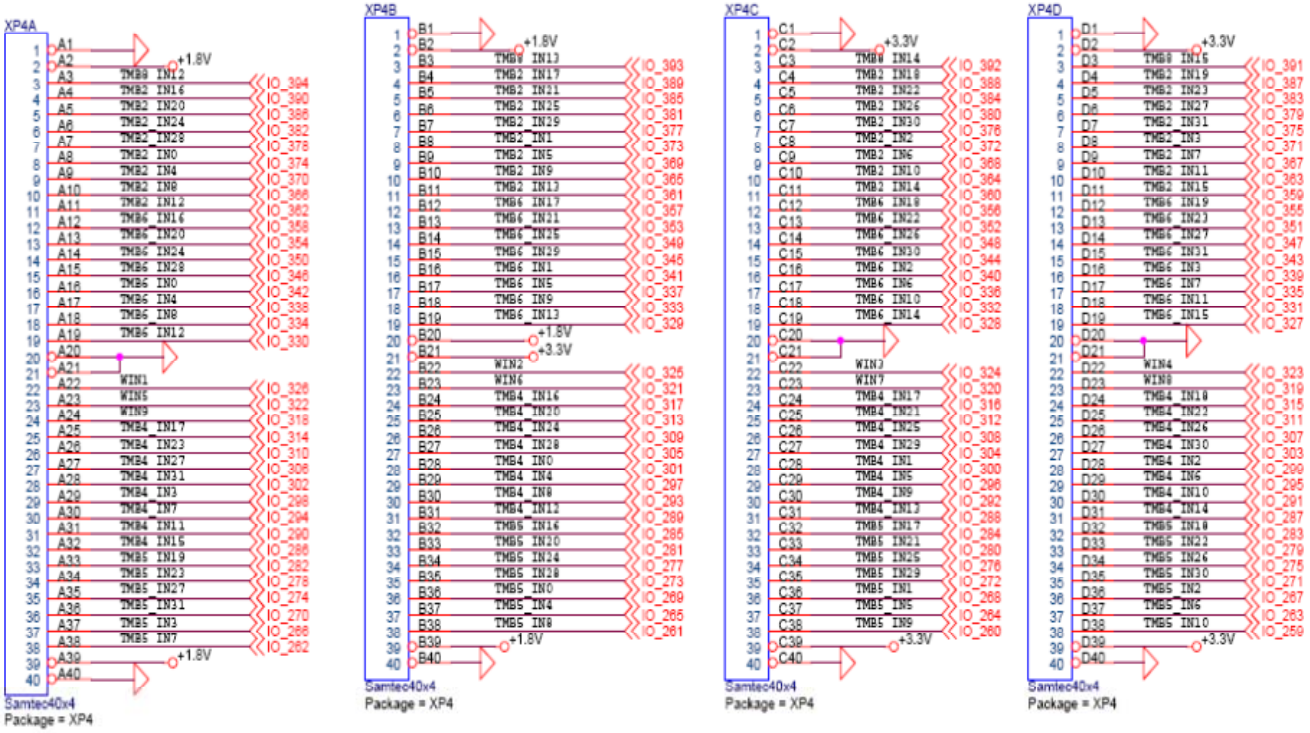
Pin assignment of XP2 mezzanine connector (top)



Pin assignment of XP3 mezzanine connector (bottom)



Pin assignment of XP4 mezzanine connector (right)



Appendix B

Unified Data Format for 8 new MPC-to-SP links running at 160MHz (all CSC chambers)

GTP1 (MGTTX0_101)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB2_LCT0_HS[0]	TMB2_LCT1_HS[0]	TMB2_LCT0_QUAL[0]	TMB2_LCT1_QUAL[0]	D(0)
TMB2_LCT0_HS[1]	TMB2_LCT1_HS[1]	TMB2_LCT0_QUAL[1]	TMB2_LCT1_QUAL[1]	D(1)
TMB2_LCT0_HS[2]	TMB2_LCT1_HS[2]	TMB2_LCT0_QUAL[2]	TMB2_LCT1_QUAL[2]	D(2)
TMB2_LCT0_HS[3]	TMB2_LCT1_HS[3]	TMB2_LCT0_QUAL[3]	TMB2_LCT1_QUAL[3]	D(3)
TMB2_LCT0_HS[4]	TMB2_LCT1_HS[4]	TMB2_LCT0_CPAT[0]	TMB2_LCT1_CPAT[0]	D(4)
TMB2_LCT0_HS[5]	TMB2_LCT1_HS[5]	TMB2_LCT0_CPAT[1]	TMB2_LCT1_CPAT[1]	D(5)
TMB2_LCT0_HS[6]	TMB2_LCT1_HS[6]	TMB2_LCT0_CPAT[2]	TMB2_LCT1_CPAT[2]	D(6)
TMB2_LCT0_HS[7]	TMB2_LCT1_HS[7]	TMB2_LCT0_CPAT[3]	TMB2_LCT1_CPAT[3]	D(7)
TMB2_LCT0_WG[0]	TMB2_LCT1_WG[0]	TMB2_LCT0_L/R]	TMB1_LCT0_WG[0]	D(8)
TMB2_LCT0_WG[1]	TMB2_LCT1_WG[1]	TMB2_LCT1_L/R	TMB1_LCT0_WG[1]	D(9)
TMB2_LCT0_WG[2]	TMB2_LCT1_WG[2]	TMB2_LCT0_VPF	TMB1_LCT0_WG[2]	D(10)
TMB2_LCT0_WG[3]	TMB2_LCT1_WG[3]	TMB2_LCT1_VPF	TMB1_LCT0_WG[3]	D(11)
TMB2_LCT0_WG[4]	TMB2_LCT1_WG[4]	TMB2_LCT0_BC0	TMB1_LCT0_WG[4]	D(12)
TMB2_LCT0_WG[5]	TMB2_LCT1_WG[5]	TMB2_LCT0_BX0	TMB1_LCT0_WG[5]	D(13)
TMB2_LCT0_WG[6]	TMB2_LCT1_WG[6]	TMB2_LCT0_SYER	TMB1_LCT0_WG[6]	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP2 (MGTTX1_101)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB3_LCT0_HS[0]	TMB3_LCT1_HS[0]	TMB3_LCT0_QUAL[0]	TMB3_LCT1_QUAL[0]	D(0)
TMB3_LCT0_HS[1]	TMB3_LCT1_HS[1]	TMB3_LCT0_QUAL[1]	TMB3_LCT1_QUAL[1]	D(1)
TMB3_LCT0_HS[2]	TMB3_LCT1_HS[2]	TMB3_LCT0_QUAL[2]	TMB3_LCT1_QUAL[2]	D(2)
TMB3_LCT0_HS[3]	TMB3_LCT1_HS[3]	TMB3_LCT0_QUAL[3]	TMB3_LCT1_QUAL[3]	D(3)
TMB3_LCT0_HS[4]	TMB3_LCT1_HS[4]	TMB3_LCT0_CPAT[0]	TMB3_LCT1_CPAT[0]	D(4)
TMB3_LCT0_HS[5]	TMB3_LCT1_HS[5]	TMB3_LCT0_CPAT[1]	TMB3_LCT1_CPAT[1]	D(5)
TMB3_LCT0_HS[6]	TMB3_LCT1_HS[6]	TMB3_LCT0_CPAT[2]	TMB3_LCT1_CPAT[2]	D(6)
TMB3_LCT0_HS[7]	TMB3_LCT1_HS[7]	TMB3_LCT0_CPAT[3]	TMB3_LCT1_CPAT[3]	D(7)
TMB3_LCT0_WG[0]	TMB3_LCT1_WG[0]	TMB3_LCT0_L/R	TMB1_LCT1_WG[0]	D(8)
TMB3_LCT0_WG[1]	TMB3_LCT1_WG[1]	TMB3_LCT1_L/R	TMB1_LCT1_WG[1]	D(9)
TMB3_LCT0_WG[2]	TMB3_LCT1_WG[2]	TMB3_LCT0_VPF	TMB1_LCT1_WG[2]	D(10)
TMB3_LCT0_WG[3]	TMB3_LCT1_WG[3]	TMB3_LCT1_VPF	TMB1_LCT1_WG[3]	D(11)
TMB3_LCT0_WG[4]	TMB3_LCT1_WG[4]	TMB3_LCT0_BC0	TMB1_LCT1_WG[4]	D(12)
TMB3_LCT0_WG[5]	TMB3_LCT1_WG[5]	TMB3_LCT0_BX0	TMB1_LCT1_WG[5]	D(13)
TMB3_LCT0_WG[6]	TMB3_LCT1_WG[6]	TMB3_LCT0_SYER	TMB1_LCT1_WG[6]	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP3 (MGTTX0_123)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB4_LCT0_HS[0]	TMB4_LCT1_HS[0]	TMB4_LCT0_QUAL[0]	TMB4_LCT1_QUAL[0]	D(0)
TMB4_LCT0_HS[1]	TMB4_LCT1_HS[1]	TMB4_LCT0_QUAL[1]	TMB4_LCT1_QUAL[1]	D(1)
TMB4_LCT0_HS[2]	TMB4_LCT1_HS[2]	TMB4_LCT0_QUAL[2]	TMB4_LCT1_QUAL[2]	D(2)
TMB4_LCT0_HS[3]	TMB4_LCT1_HS[3]	TMB4_LCT0_QUAL[3]	TMB4_LCT1_QUAL[3]	D(3)
TMB4_LCT0_HS[4]	TMB4_LCT1_HS[4]	TMB4_LCT0_CPAT[0]	TMB4_LCT1_CPAT[0]	D(4)
TMB4_LCT0_HS[5]	TMB4_LCT1_HS[5]	TMB4_LCT0_CPAT[1]	TMB4_LCT1_CPAT[1]	D(5)
TMB4_LCT0_HS[6]	TMB4_LCT1_HS[6]	TMB4_LCT0_CPAT[2]	TMB4_LCT1_CPAT[2]	D(6)
TMB4_LCT0_HS[7]	TMB4_LCT1_HS[7]	TMB4_LCT0_CPAT[3]	TMB4_LCT1_CPAT[3]	D(7)
TMB4_LCT0_WG[0]	TMB4_LCT1_WG[0]	TMB4_LCT0_L/R	TMB1_LCT0_HS[0]	D(8)
TMB4_LCT0_WG[1]	TMB4_LCT1_WG[1]	TMB4_LCT1_L/R	TMB1_LCT0_HS[1]	D(9)
TMB4_LCT0_WG[2]	TMB4_LCT1_WG[2]	TMB4_LCT0_VPF	TMB1_LCT0_HS[2]	D(10)
TMB4_LCT0_WG[3]	TMB4_LCT1_WG[3]	TMB4_LCT1_VPF	TMB1_LCT0_HS[3]	D(11)
TMB4_LCT0_WG[4]	TMB4_LCT1_WG[4]	TMB4_LCT0_BC0	TMB1_LCT0_HS[4]	D(12)
TMB4_LCT0_WG[5]	TMB4_LCT1_WG[5]	TMB4_LCT0_BX0	TMB1_LCT0_HS[5]	D(13)
TMB4_LCT0_WG[6]	TMB4_LCT1_WG[6]	TMB4_LCT0_SYER	TMB1_LCT0_HS[6]	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP4 (MGTTX1_123)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB5_LCT0_HS[0]	TMB5_LCT1_HS[0]	TMB5_LCT0_QUAL[0]	TMB5_LCT1_QUAL[0]	D(0)
TMB5_LCT0_HS[1]	TMB5_LCT1_HS[1]	TMB5_LCT0_QUAL[1]	TMB5_LCT1_QUAL[1]	D(1)
TMB5_LCT0_HS[2]	TMB5_LCT1_HS[2]	TMB5_LCT0_QUAL[2]	TMB5_LCT1_QUAL[2]	D(2)
TMB5_LCT0_HS[3]	TMB5_LCT1_HS[3]	TMB5_LCT0_QUAL[3]	TMB5_LCT1_QUAL[3]	D(3)
TMB5_LCT0_HS[4]	TMB5_LCT1_HS[4]	TMB5_LCT0_CPAT[0]	TMB5_LCT1_CPAT[0]	D(4)
TMB5_LCT0_HS[5]	TMB5_LCT1_HS[5]	TMB5_LCT0_CPAT[1]	TMB5_LCT1_CPAT[1]	D(5)
TMB5_LCT0_HS[6]	TMB5_LCT1_HS[6]	TMB5_LCT0_CPAT[2]	TMB5_LCT1_CPAT[2]	D(6)
TMB5_LCT0_HS[7]	TMB5_LCT1_HS[7]	TMB5_LCT0_CPAT[3]	TMB5_LCT1_CPAT[3]	D(7)
TMB5_LCT0_WG[0]	TMB5_LCT1_WG[0]	TMB5_LCT0_L/R	TMB1_LCT1_HS[0]	D(8)
TMB5_LCT0_WG[1]	TMB5_LCT1_WG[1]	TMB5_LCT1_L/R	TMB1_LCT1_HS[1]	D(9)
TMB5_LCT0_WG[2]	TMB5_LCT1_WG[2]	TMB5_LCT0_VPF	TMB1_LCT1_HS[2]	D(10)
TMB5_LCT0_WG[3]	TMB5_LCT1_WG[3]	TMB5_LCT1_VPF	TMB1_LCT1_HS[3]	D(11)
TMB5_LCT0_WG[4]	TMB5_LCT1_WG[4]	TMB5_LCT0_BC0	TMB1_LCT1_HS[4]	D(12)
TMB5_LCT0_WG[5]	TMB5_LCT1_WG[5]	TMB5_LCT0_BX0	TMB1_LCT1_HS[5]	D(13)
TMB5_LCT0_WG[6]	TMB5_LCT1_WG[6]	TMB5_LCT0_SYER	TMB1_LCT1_HS[6]	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP5 (MGTTX0_267)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB6_LCT0_HS[0]	TMB6_LCT1_HS[0]	TMB6_LCT0_QUAL[0]	TMB6_LCT1_QUAL[0]	D(0)
TMB6_LCT0_HS[1]	TMB6_LCT1_HS[1]	TMB6_LCT0_QUAL[1]	TMB6_LCT1_QUAL[1]	D(1)
TMB6_LCT0_HS[2]	TMB6_LCT1_HS[2]	TMB6_LCT0_QUAL[2]	TMB6_LCT1_QUAL[2]	D(2)
TMB6_LCT0_HS[3]	TMB6_LCT1_HS[3]	TMB6_LCT0_QUAL[3]	TMB6_LCT1_QUAL[3]	D(3)
TMB6_LCT0_HS[4]	TMB6_LCT1_HS[4]	TMB6_LCT0_CPAT[0]	TMB6_LCT1_CPAT[0]	D(4)
TMB6_LCT0_HS[5]	TMB6_LCT1_HS[5]	TMB6_LCT0_CPAT[1]	TMB6_LCT1_CPAT[1]	D(5)
TMB6_LCT0_HS[6]	TMB6_LCT1_HS[6]	TMB6_LCT0_CPAT[2]	TMB6_LCT1_CPAT[2]	D(6)
TMB6_LCT0_HS[7]	TMB6_LCT1_HS[7]	TMB6_LCT0_CPAT[3]	TMB6_LCT1_CPAT[3]	D(7)
TMB6_LCT0_WG[0]	TMB6_LCT1_WG[0]	TMB6_LCT0_L/R	TMB1_LCT0_QUAL[0]	D(8)
TMB6_LCT0_WG[1]	TMB6_LCT1_WG[1]	TMB6_LCT1_L/R	TMB1_LCT0_QUAL[1]	D(9)
TMB6_LCT0_WG[2]	TMB6_LCT1_WG[2]	TMB6_LCT0_VPF	TMB1_LCT0_QUAL[2]	D(10)
TMB6_LCT0_WG[3]	TMB6_LCT1_WG[3]	TMB6_LCT1_VPF	TMB1_LCT0_QUAL[3]	D(11)
TMB6_LCT0_WG[4]	TMB6_LCT1_WG[4]	TMB6_LCT0_BC0	TMB1_LCT0_L/R	D(12)
TMB6_LCT0_WG[5]	TMB6_LCT1_WG[5]	TMB6_LCT0_BX0	TMB1_LCT0_VPF	D(13)
TMB6_LCT0_WG[6]	TMB6_LCT1_WG[6]	TMB6_LCT0_SYER	TMB1_LCT0_HS[7]	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP6 (MGTTX1_267)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB7_LCT0_HS[0]	TMB7_LCT1_HS[0]	TMB7_LCT0_QUAL[0]	TMB7_LCT1_QUAL[0]	D(0)
TMB7_LCT0_HS[1]	TMB7_LCT1_HS[1]	TMB7_LCT0_QUAL[1]	TMB7_LCT1_QUAL[1]	D(1)
TMB7_LCT0_HS[2]	TMB7_LCT1_HS[2]	TMB7_LCT0_QUAL[2]	TMB7_LCT1_QUAL[2]	D(2)
TMB7_LCT0_HS[3]	TMB7_LCT1_HS[3]	TMB7_LCT0_QUAL[3]	TMB7_LCT1_QUAL[3]	D(3)
TMB7_LCT0_HS[4]	TMB7_LCT1_HS[4]	TMB7_LCT0_CPAT[0]	TMB7_LCT1_CPAT[0]	D(4)
TMB7_LCT0_HS[5]	TMB7_LCT1_HS[5]	TMB7_LCT0_CPAT[1]	TMB7_LCT1_CPAT[1]	D(5)
TMB7_LCT0_HS[6]	TMB7_LCT1_HS[6]	TMB7_LCT0_CPAT[2]	TMB7_LCT1_CPAT[2]	D(6)
TMB7_LCT0_HS[7]	TMB7_LCT1_HS[7]	TMB7_LCT0_CPAT[3]	TMB7_LCT1_CPAT[3]	D(7)
TMB7_LCT0_WG[0]	TMB7_LCT1_WG[0]	TMB7_LCT0_L/R	TMB1_LCT1_QUAL[0]	D(8)
TMB7_LCT0_WG[1]	TMB7_LCT1_WG[1]	TMB7_LCT1_L/R	TMB1_LCT1_QUAL[1]	D(9)
TMB7_LCT0_WG[2]	TMB7_LCT1_WG[2]	TMB7_LCT0_VPF	TMB1_LCT1_QUAL[2]	D(10)
TMB7_LCT0_WG[3]	TMB7_LCT1_WG[3]	TMB7_LCT1_VPF	TMB1_LCT1_QUAL[3]	D(11)
TMB7_LCT0_WG[4]	TMB7_LCT1_WG[4]	TMB7_LCT0_BC0	TMB1_LCT1_L/R	D(12)
TMB7_LCT0_WG[5]	TMB7_LCT1_WG[5]	TMB7_LCT0_BX0	TMB1_LCT1_VPF	D(13)
TMB7_LCT0_WG[6]	TMB7_LCT1_WG[6]	TMB7_LCT0_SYER	TMB1_LCT1_HS[7]	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP7 (MGTTX0_245)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB8_LCT0_HS[0]	TMB8_LCT1_HS[0]	TMB8_LCT0_QUAL[0]	TMB8_LCT1_QUAL[0]	D(0)
TMB8_LCT0_HS[1]	TMB8_LCT1_HS[1]	TMB8_LCT0_QUAL[1]	TMB8_LCT1_QUAL[1]	D(1)
TMB8_LCT0_HS[2]	TMB8_LCT1_HS[2]	TMB8_LCT0_QUAL[2]	TMB8_LCT1_QUAL[2]	D(2)
TMB8_LCT0_HS[3]	TMB8_LCT1_HS[3]	TMB8_LCT0_QUAL[3]	TMB8_LCT1_QUAL[3]	D(3)
TMB8_LCT0_HS[4]	TMB8_LCT1_HS[4]	TMB8_LCT0_CPAT[0]	TMB8_LCT1_CPAT[0]	D(4)
TMB8_LCT0_HS[5]	TMB8_LCT1_HS[5]	TMB8_LCT0_CPAT[1]	TMB8_LCT1_CPAT[1]	D(5)
TMB8_LCT0_HS[6]	TMB8_LCT1_HS[6]	TMB8_LCT0_CPAT[2]	TMB8_LCT1_CPAT[2]	D(6)
TMB8_LCT0_HS[7]	TMB8_LCT1_HS[7]	TMB8_LCT0_CPAT[3]	TMB8_LCT1_CPAT[3]	D(7)
TMB8_LCT0_WG[0]	TMB8_LCT1_WG[0]	TMB8_LCT0_L/R	TMB1_LCT0_CPAT[0]	D(8)
TMB8_LCT0_WG[1]	TMB8_LCT1_WG[1]	TMB8_LCT1_L/R	TMB1_LCT0_CPAT[1]	D(9)
TMB8_LCT0_WG[2]	TMB8_LCT1_WG[2]	TMB8_LCT0_VPF	TMB1_LCT0_CPAT[2]	D(10)
TMB8_LCT0_WG[3]	TMB8_LCT1_WG[3]	TMB8_LCT1_VPF	TMB1_LCT0_CPAT[3]	D(11)
TMB8_LCT0_WG[4]	TMB8_LCT1_WG[4]	TMB8_LCT0_BC0	TMB1_LCT0_BC0	D(12)
TMB8_LCT0_WG[5]	TMB8_LCT1_WG[5]	TMB8_LCT0_BX0	TMB1_LCT0_BX0	D(13)
TMB8_LCT0_WG[6]	TMB8_LCT1_WG[6]	TMB8_LCT0_SYER	TMB1_LCT0_SYER	D(14)
“1”	“0”	“0”	“0”	D(15)

GTP8 (MGTTX1_245)

Frame 0	Frame 1	Frame 2	Frame 3	GTP Data line
TMB9_LCT0_HS[0]	TMB9_LCT1_HS[0]	TMB9_LCT0_QUAL[0]	TMB9_LCT1_QUAL[0]	D(0)
TMB9_LCT0_HS[1]	TMB9_LCT1_HS[1]	TMB9_LCT0_QUAL[1]	TMB9_LCT1_QUAL[1]	D(1)
TMB9_LCT0_HS[2]	TMB9_LCT1_HS[2]	TMB9_LCT0_QUAL[2]	TMB9_LCT1_QUAL[2]	D(2)
TMB9_LCT0_HS[3]	TMB9_LCT1_HS[3]	TMB9_LCT0_QUAL[3]	TMB9_LCT1_QUAL[3]	D(3)
TMB9_LCT0_HS[4]	TMB9_LCT1_HS[4]	TMB9_LCT0_CPAT[0]	TMB9_LCT1_CPAT[0]	D(4)
TMB9_LCT0_HS[5]	TMB9_LCT1_HS[5]	TMB9_LCT0_CPAT[1]	TMB9_LCT1_CPAT[1]	D(5)
TMB9_LCT0_HS[6]	TMB9_LCT1_HS[6]	TMB9_LCT0_CPAT[2]	TMB9_LCT1_CPAT[2]	D(6)
TMB9_LCT0_HS[7]	TMB9_LCT1_HS[7]	TMB9_LCT0_CPAT[3]	TMB9_LCT0_CPAT[3]	D(7)
TMB9_LCT0_WG[0]	TMB9_LCT1_WG[0]	TMB9_LCT0_L/R	TMB1_LCT1_CPAT[0]	D(8)
TMB9_LCT0_WG[1]	TMB9_LCT1_WG[1]	TMB9_LCT1_L/R	TMB1_LCT1_CPAT[1]	D(9)
TMB9_LCT0_WG[2]	TMB9_LCT1_WG[2]	TMB9_LCT0_VPF	TMB1_LCT1_CPAT[2]	D(10)
TMB9_LCT0_WG[3]	TMB9_LCT1_WG[3]	TMB9_LCT1_VPF	TMB1_LCT1_CPAT[3]	D(11)
TMB9_LCT0_WG[4]	TMB9_LCT1_WG[4]	TMB9_LCT0_BC0	“0” (RESERVED)	D(12)
TMB9_LCT0_WG[5]	TMB9_LCT1_WG[5]	TMB9_LCT0_BX0	“0” (RESERVED)	D(13)
TMB9_LCT0_WG[6]	TMB9_LCT1_WG[6]	TMB9_LCT0_SYER	“0” (RESERVED)	D(14)
“1”	“0”	“0”	“0”	D(15)