Muon Port Card

Firmware version 05/30/2004

The firmware version 05/30/2004 provides two basic mode of the MPC operation:

- "sorter" mode described in the manual [1], and
- "transparent" mode, when any (out of 18) incoming LCT may be directed to any (out of 3) optical link without sorting.

Both modes apply to any source of data (either TMB's, or FIFO_A buffers). An additional CSR4 (with the address = **base + b8**) defines the mode of operation and the sources for optical link in a "transparent" mode. When CSR4[0]=0, the MPC is in a "sorter" mode. This is a default state after power cycling. When CSR4[0]=1, the MPC is in a "transparent " mode. Then the CSR4[15..1] bits define the source of data for optical links (Tables 1..3). Muon_1 and Muon_2 correspond to LCT0 and LCT1 respectively from TMB on slot 2 in the peripheral crate (or from FIFO_A1[15..0] and FIFO_A1[31..16] respectively). Muon_3 and Muon_4 correspond to LCT0 and LCT1 respectively from TMB on slot 4 in the peripheral crate (or from FIFO_A2[15..0] and FIFO_A2[31..16] respectively) and so on.

Table 1

Bits in CSR4																Source of data to optolink 1 (1st best) and FIFO_B1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	"sorter" mode
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	All sources disabled
x	x	x	x	x	x	x	x	x	x	0	0	0	0	1	1	Muon_1
x	x	x	x	x	x	x	x	x	x	0	0	0	1	0	1	Muon_2
x	x	x	x	x	x	x	x	x	x	0	0	0	1	1	1	Muon_3
x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	1	Muon_4
x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	Muon_5
x	x	x	x	x	x	x	x	x	x	0	0	1	1	0	1	Muon_6
x	x	x	x	x	x	x	x	x	x	0	0	1	1	1	1	Muon_7
x	x	x	x	x	x	x	x	x	x	0	1	0	0	0	1	Muon_8
x	x	x	x	x	x	x	x	x	x	0	1	0	0	1	1	Muon_9
x	x	x	x	x	x	x	x	x	x	0	1	0	1	0	1	Muon_10
x	x	x	x	x	x	x	x	x	x	0	1	0	1	1	1	Muon_11
x	x	x	x	x	x	x	x	x	x	0	1	1	0	0	1	Muon_12
x	x	x	x	x	x	x	x	x	x	0	1	1	0	1	1	Muon_13
x	x	x	x	x	x	x	x	x	x	0	1	1	1	0	1	Muon_14
x	x	x	x	x	x	x	x	x	x	0	1	1	1	1	1	Muon_15
x	x	x	x	x	x	x	x	x	x	1	0	0	0	0	1	Muon_16
x	x	x	x	x	x	x	x	x	x	1	0	0	0	1	1	Muon_17
x	x	x	x	x	x	x	x	x	x	1	0	0	1	0	1	Muon_18

Table 2

Bits in CSR4																Source of data to optolink 2 (2nd best) and FIFO_B2
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	"sorter" mode
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	All sources disabled
x	x	x	x	x	0	0	0	0	1	x	x	x	x	x	1	Muon_1
x	x	x	x	x	0	0	0	1	0	x	x	x	x	x	1	Muon_2
x	x	x	x	x	0	0	0	1	1	x	x	x	x	x	1	Muon_3
x	x	x	x	x	0	0	1	0	0	x	x	x	x	x	1	Muon_4
x	x	x	x	x	0	0	1	0	1	x	x	x	x	x	1	Muon_5
x	x	x	x	x	0	0	1	1	0	x	x	x	x	x	1	Muon_6
x	x	x	x	x	0	0	1	1	1	x	x	x	x	x	1	Muon_7
x	x	x	x	x	0	1	0	0	0	x	x	x	x	x	1	Muon_8
x	x	x	x	x	0	1	0	0	1	x	x	x	x	x	1	Muon_9
x	x	x	x	x	0	1	0	1	0	x	x	x	x	x	1	Muon_10
x	x	x	x	x	0	1	0	1	1	x	x	x	x	x	1	Muon_11
x	x	x	x	x	0	1	1	0	0	x	x	x	x	x	1	Muon_12
x	x	x	x	x	0	1	1	0	1	x	x	x	x	x	1	Muon_13
x	x	x	x	x	0	1	1	1	0	x	x	x	x	x	1	Muon_14
x	x	x	x	x	0	1	1	1	1	x	x	x	x	x	1	Muon_15
x	x	x	x	x	1	0	0	0	0	x	x	x	x	x	1	Muon_16
x	x	x	x	x	1	0	0	0	1	x	x	x	x	x	1	Muon_17
x	x	x	x	x	1	0	0	1	0	x	x	x	x	x	1	Muon_18

Table 3

Bits in CSR4																Source of data to optolink 3 (3rd best) and FIFO_B3
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	"sorter" mode
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	All sources disabled
0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	1	Muon_1
0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	1	Muon_2
0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	1	Muon_3
0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	1	Muon_4
0	0	1	0	1	x	x	x	x	x	x	x	x	x	x	1	Muon_5
0	0	1	1	0	x	x	x	x	x	x	x	x	x	x	1	Muon_6
0	0	1	1	1	x	x	x	x	x	x	x	x	x	x	1	Muon_7
0	1	0	0	0	x	x	x	x	x	x	x	x	x	x	1	Muon_8
0	1	0	0	1	x	x	x	x	x	x	x	x	x	x	1	Muon_9
0	1	0	1	0	x	x	x	x	x	x	x	x	x	x	1	Muon_10
0	1	0	1	1	x	x	x	x	x	x	x	x	x	x	1	Muon_11
0	1	1	0	0	x	x	x	x	x	x	x	x	x	x	1	Muon_12
0	1	1	0	1	x	x	x	x	x	x	x	x	x	x	1	Muon_13
0	1	1	1	0	x	x	x	x	x	x	x	x	x	x	1	Muon_14
0	1	1	1	1	x	x	x	x	x	x	x	x	x	x	1	Muon_15

1	0	0	0	0	x	x	x	x	x	x	x	x	x	x	1	Muon_16
1	0	0	0	1	x	x	x	x	x	x	x	x	x	x	1	Muon_17
1	0	0	1	0	x	x	x	x	x	x	x	x	x	x	1	Muon_18

In a “sorter” mode the MPC generates winner bits as described in [1]. In a “transparent” mode the MPC generated winner bits to those TMB’s, that were selected by CSR4[15..1] if “valid pattern flag” of the selected muon is “1”. The order of “winner” bits is the same in both modes: if LCT0 was selected, the “winner” bit is transmitted in the first 80Mhz frame. If LCT1 was selected, the “winner” bit is transmitted in the second 80Mhz frame.

The internal latency of the MPC processing is the same in both modes.

In a “sorter” mode the “vpf” bit from the first best selected muon acts as a “write enable” signal for all FIFO_B buffers. This assures that all three FIFO_B buffers will contain an equal number of words. But in a ”transparent” mode the “vpf” bit of every selected by CSR4[15..1] bits pattern acts as a “write enable” for its own FIFO_B buffer. So the number of words in three FIFO_B buffers may be different.

References

[1]. Muon Port Card Specification. Available at http://bonner-ntserver.rice.edu/cms/MPC2002.pdf