The MS2005 Muon Sorter Specification

Version 1.2

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Introduction

This document describes the second version of the Muon Sorter MS2005 board (built in July 2005) for the CSC EMU Trigger System at CMS. The MS2005 is located in the middle of the Track Finder (TF) crate and receives up to 36 muon tracks from 12 Sector Processors (SP) over custom 6U backplane. The MS2005 selects the four best muon candidates and transmits them in ranked order to the Global Muon Trigger (GMT) Receiver board over four copper cables. The functionality and external connections of the MS2005 are described below. Block diagram of the MS2005 board is shown on Figure 1. It comprises the backplane interface, VME interface, main processing logic based on Xilinx FPGA, located on a mezzanine card, and LVDS transmitters to GMT crate.

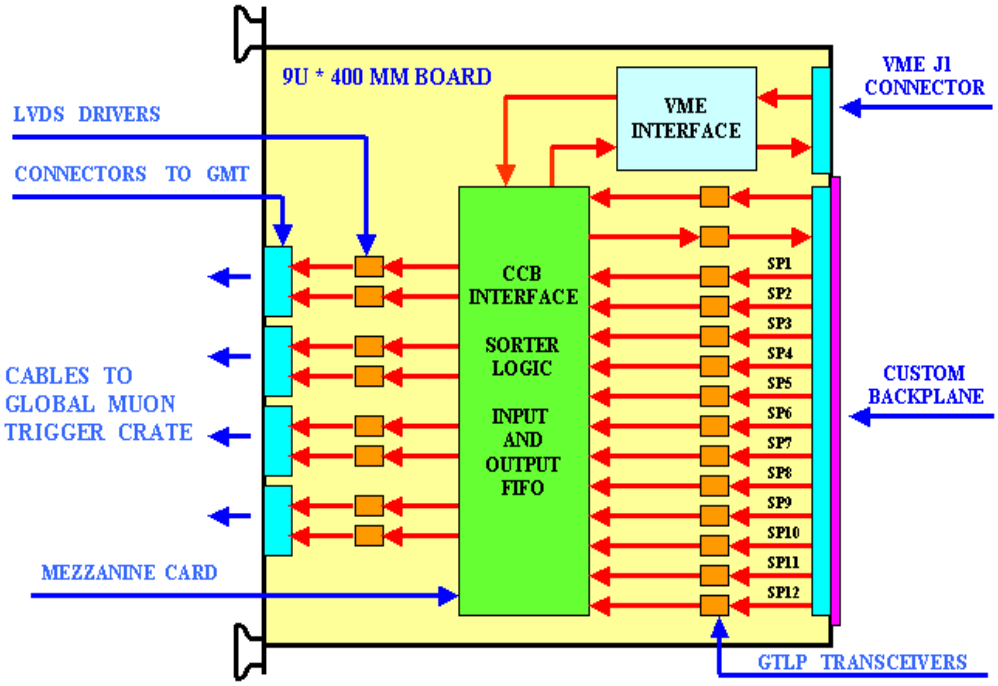

Figure 1: MS2005 Board Block Diagram

1. Interface to Clock and Control Board

The CCB distributes several common (bussed) and individual (point-to-point) signals to each module in the Track Finder crate. A full list of these signals is given in [1]. Its subset relevant to MS2005 is shown in Table 1. While the 40.08Mhz clock signal from the CCB is distributed over LVDS lines individually to each board in a crate, the other signals are transmitted using GTLP logic standard, with active level "0".

The MS2005 may generate the MS_L1A_Request signal to CCB when there is at least one valid muon after the sorting. Generation of this signal can be enabled and disabled using CSR0[7]. There are four reserved signals from the CCB to MS2005 and two reserved signals from the MS2005 to CCB.

The list of commands decoded from the ccb_cmd[5..0] lines is shown in Table 2.

Table 1: CCB-to-MS Signals

Signal	Bits	Type	Logic	Duration
Clock Bus				
Ccb_clock40	1	Point-to-point, input	LVDS	40.08Mhz
Fast Control Bus				
Ccb_clock40_enable	1	Bussed, input	GTLP	40.08Mhz reference frequency
Ccb_cmd[5..0]	6	Bussed, input	GTLP	Level
Ccb_evcntres	1	Bussed, input	GTLP	25 ns
Ccb_bcntres	1	Bussed, input	GTLP	25 ns
Ccb_cmd_strobe	1	Bussed, input	GTLP	25 ns
Ccb_bc0	1	Bussed, input	GTLP	25 ns
Ccb_l1accept	1	Bussed, input	GTLP	25 ns
Ccb_data[7..0]	8	Bussed, input	GTLP	Level
Ccb_data_strobe	1	Bussed, input	GTLP	25 ns
Ccb_ttcrx_ready	1	Bussed, input	GTLP	Level
Ccb_reserved[4..1]	4	Bussed, input	GTLP	25 ns
Reload, Trigger and Reserved Lines				
MS_hard_reset	1	Point-to-point, input	GTLP	300 ns
MS_cfg_done	1	Point-to-point, output	GTLP	Level
MS_L1A_Request	1	Point-to-point, output	GTLP	25 ns
CCB_to_MS[3..0] (reserved)	4	Point-to-point, input	GTLP	
MS_to_CCB[1..0] (reserved)	2	Point-to-point, output	GTLP	

Table 2: Commands decoded from the ccb_cmd[5..0] lines

Command	Ccb_cmd[5..0] code (hex)	Comment
BC0	1	Bunch crossing counter starts counting on the next clock tick
L1Reset	3	Load initial value into bunch crossing counter
Hard Reser	4	Reload FPGA from EPROMs
Start Trigger	6	Set "winner bit mode" for "winner" bits
Stop Trigger	7	Set "training patter mode" for "winner" bits
MS_Hard _Reset	11	Reload FPGA from EPROMs
Inject patterns from MS	31	Send test patterns from the FIFO_A to sorter
Bunch Counter Reset	32	Load initial value into bunch crossing counter

Two Digital Clock Managers (DCM, see [2]) inside the main Xilinx Virtex-2 FPGA are used. The DCM1 allows to precisely adjust the phase of the input clock in respect to data arriving from SP's. In addition to this, the phase of input clock can be adjusted using external delay chip 3D7408-025 (see CSR8). The DCM2 allows to precisely adjust the

phase of the output clock in respect to data sent to GMT. Phase adjustment range is approximately +/-100 bits, so one bit corresponds to ~100 ps. Phase adjustment can be done dynamically over VME. To increase (decrease) a phase by 1 bit, "1" ("0") should be written into the fine phase adjustment registers (Table 14). It is recommended to reset the DCM before changing the phase. After power cycling the phase is set to "0". The DCM status bits are available for read over VME from the CSR5 (Table 24).

2. Sorting Logic and Interface to Sector Processors

Each SP sends to MS2005 up to three muon tracks every 25 ns. Each pattern comprises 64 bits being sent in two frames at 80 Mhz. The frame format based on [3] is shown in Table 3.

The MS2005 sorter unit accepts 36 7-bit patterns called "Rank[6..0]" that represent the "quality" of each incoming pattern and outputs four 36-bit binary addresses of the first, second, third and fourth largest patterns. These 144 bits are used for pattern merging onto the sorter outputs. Some bits of the selected patterns are undergo further LUT conversion (see Section 3) before they are transmitted to GMT. If several selected patterns appear to have the same rank, then the pattern from the source with a largest physical address will be chosen as a 1st best, the pattern from the source with the second largest physical address will be chosen as a 2nd best and so on. Physical addresses SP_ID[3..0] from 1 to 12 are assigned to each Sector Processor (starting from the very left in the TF crate) in the MS2005 firmware. It is assumed that if there are no valid muons selected by the Sector Processor, then each SP sends a Rank[6..0]=0.

If a particular pattern from the SP has been accepted by the MS, then a "winner" bit is sent from the MS2005 back to corresponding SP, if the MS2005 is in a "winner bit mode". The total number of feedback "winner" lines is 24, or 2 lines per each SP. The "winner" bits are sent in two 80MHz frames, encoded as shown in Tables 4 and 5. The "winner" bits may be delayed within FPGA for a programmable number of bunch crossings (1..15), defined by CSR0[15..12]. Alternatively, the MS2005 may be in a "training pattern mode", then it returns a 40Mhz pattern on Wi[0] (i=1..12) line to every Sector Processor. This feature allows SP's to adjust their timing on "winner" bits. The MS2005 is set to "winner" bit mode after power up.

Table 3: SP-to-MS Data Format

First frame transmitted at 80MHz			Second frame transmitted at 80Mhz		
Bit	Signal	Muon	Bit	Signal	Muon
0	Phi_0	1	0	Rank_0	1
1	Phi_1	1	1	Rank_1	1
2	Phi_2	1	2	Rank_2	1
3	Phi_3	1	3	Rank_3	1
4	Phi_4	1	4	Rank_4	1
5	Eta_0	1	5	Rank_5	1
6	Eta_1	1	6	Rank_6	1
7	Eta_2	1	7	VC	1
8	Eta_3	1	8	C	1
9	Eta_4	1	9	HL	1
10	Phi_0	2	10	Rank_0	2
11	Phi_1	2	11	Rank_1	2

12	Phi_2	2	12	Rank_2	2
13	Phi_3	2	13	Rank_3	2
14	Phi_4	2	14	Rank_4	2
15	Eta_0	2	15	Rank_5	2
16	Eta_1	2	16	Rank_6	2
17	Eta_2	2	17	VC	2
18	Eta_3	2	18	C	2
19	Eta_4	2	19	HL	2
20	Phi_0	3	20	Rank_0	3
21	Phi_1	3	21	Rank_1	3
22	Phi_2	3	22	Rank_2	3
23	Phi_3	3	23	Rank_3	3
24	Phi_4	3	24	Rank_4	3
25	Eta_0	3	25	Rank_5	3
26	Eta_1	3	26	Rank_6	3
27	Eta_2	3	27	VC	3
28	Eta_3	3	28	C	3
29	Eta_4	3	29	HL	3
30	BC0	Common to 1-3	30	BX0	Common to 1-3
31	SE	Common to 1-3	31	SP	Common to 1-3

VC – Valid Charge (8th bit of Pt LUT output), **C** – Charge or Muon Sign
Rank – Pt LUT Output , **HL** – Halo Muon Trigger
BC0 – Bunch Crossing Zero Flag , **Eta** – Pseudorapidity
SE – Synchronization Error (Data out of sync), **Phi** – Azimuth Coordinate
BX0 – Least significant bit of the bunch crossing counter, **SP** – Spare bit

Table 4: MS-to-SP "Winner" Bit Data Format (i=1..12)

Line and frame	Function
Wi_0_Frame1	"1" if Muon_1 was selected by MS from SPi
Wi_0_Frame2	"1" if Muon_3 was selected by MS from SPi
Wi_1_Frame1	"1" if Muon_2 was selected by MS from SPi
Wi_1_Frame2	"0"

Table 5: "Winner" Bit Decoding Scheme

Selected Muons from SPi			Winner Bits			
Muon_3	Muon_2	Muon_1	Wi_1_Frame1	Wi_0_Frame1	Wi_1_Frame2	Wi_0_Frame2
-	-	-	0	0	0	0
-	-	+	0	1	0	0
-	+	-	1	0	0	0
-	+	+	1	1	0	0
+	-	-	0	0	0	1
+	-	+	0	1	0	1
+	+	-	1	0	0	1
+	+	+	1	1	0	1

The MS2005 maintains a 16-bit bunch crossing counter BXN. This counter is set to a predefined state using CSR7 upon L1Reset command from the LHC Trigger, Timing and Control (TTC) System and starts counting on the next clock tick after the BC0 command from the TTC. The BX0 bit arriving with the selected muon is compared against the least significant bit of this counter. In case of a mismatch the SyncEr bit is generated and transmitted to corresponding GMT link and FIFO_B if MASKCOMP bit of the CSR0 is "1". Another CSR0 bit, called MASKSP, when "1", enables propagation of SyncEr bits from selected muons to GMT and FIFO_B. When both MASKCOMP and MASKSP are "0", the SyncEr bits being transmitted to GMT and FIFO_B are all "0".

All the 12 data streams from SP1..SP12 boards are latched into the main FPGA on a common 80MHz clock that is derived from the master 40MHz clock provided by the CCB2004 via custom backplane. The master 40MHz clock passes through the 3D7408-025 delay chip before it reaches the FPGA. The delay value can be programmed with the CSR8[7:0] and the minimal step of adjustment is 250 ps. The delayed 40MHz clock arrives into the Digital Clock Manager DCM1 in the FPGA that doubles it. The resulting 80MHz clock must be set in the middle of the "safe window" for all 12 SP sources. Fine clock adjustments within the 12.5 ns clock period can be done using either CSR8, or DCM1. The first method (CSR8) is preferred. It was measured that for 12 SP05 boards providing valid patterns simultaneously, the "safe window" corresponds to **CSR8=78..101(dec)**, so the recommended setting is **CSR8=89(dec)=59hex**. Then it is not necessary to program the DCM1 since its delay is set to "0" automatically on power cycling. For more details, including programming of the DCM, see the User's Guide [4].

All signals from the SP's (32*12=384 lines) to the MS2005 as well as 24 "winner" lines from the MS2005 to SP's are transmitted over backplane using "negative" (active "0") GTLP logic. They are terminated (56 Ohm to +1.5V) on the receiver ends. Pin assignment of the backplane connectors on MS slot based on [5] is given in Tables 6..10.

Table 6: Pin assignment of the X23 [4] backplane connector

X23	Z	A	B	C	D	E	F
1	GND	CLK_MS	CLK-MS	Ccb_ready	Ccb_rsv1	Ms_HR	GND
2	GND	Cll_enable	Ccb_rsv4	GND	Ccb_rsv2	Ccb_rsv3	GND
3	GND	Ccb_cmd0	Ccb_cmd1	GND	Ccb_cmd2	Ccb_cmd3	GND
4	GND	Ccb_cmd4	Ccb_cmd5	GND	Ccb_ecres	Ccb_bcres	GND
5	GND	Ccb_cmdstr	Ccb_bx0	GND	Ccb_l1a	Ccb_datstr	GND
6	GND	Ccb_data0	Ccb_data1	GND	Ccb_data2	Ccb_data3	GND
7	GND	Ccb_data4	Ccb_data5	GND	Ccb_data6	Ccb_data7	GND
8	GND	Ccb_to_ms0	Ccb_to_ms1	GND	Ccb_to_ms2	Ccb_to_ms3	GND
9	GND	SP1_2	SP1_3	GND	SP1_0	SP1_1	GND
10	GND	SP1_6	SP1_7	GND	SP1_4	SP1_5	GND
11	GND	SP1_10	SP1_11	GND	SP1_8	SP1_9	GND
12	GND	SP1_31	SP1_14	GND	SP1_12	SP1_13	GND
13	GND	SP1_15	SP1_18	GND	SP1_20	SP1_16	GND
14	GND	SP1_19	SP1_23	GND	SP1_17	SP1_21	GND
15	GND	SP1_24	SP1_25	GND	SP1_22	SP1_30	GND
16	GND	SP1_28	SP1_29	GND	SP1_26	SP1_27	GND
17	GND	SP12_2	SP12_3	GND	SP12_0	SP12_1	GND
18	GND	SP12_6	SP12_7	GND	SP12_4	SP12_5	GND
19	GND	SP12_10	SP12_11	GND	SP12_8	SP12_9	GND
20	GND	SP12_14	SP12_15	GND	SP12_13	SP12_31	GND
21	GND	SP12_12	SP12_19	GND	SP12_16	SP12_17	GND
22	GND	SP12_20	SP12_24	GND	SP12_18	SP12_22	GND
23	GND	SP12_25	SP12_21	GND	SP12_23	SP12_26	GND
24	GND	SP12_29	SP12_30	GND	SP12_27	SP12_28	GND
25	GND	SP3_2	SP3_3	GND	SP3_0	SP3_1	GND

Table 7: Pin assignment of the X24 [4] backplane connector

X24	Z	A	B	C	D	E	F
1	GND	SP3_6	SP3_7	GND	SP3_4	SP3_5	GND
2	GND	SP3_10	SP3_11	GND	SP3_8	SP3_9	GND
3	GND	SP3_31	SP3_14	+1.5V	SP3_12	SP3_13	GND
4	GND	SP3_15	SP3_18	GND	SP3_20	SP3_16	GND
5	GND	SP3_19	SP3_23	GND	SP3_17	SP3_21	GND
6	GND	SP3_24	SP3_25	+1.5V	SP3_22	SP3_30	GND
7	GND	SP3_28	SP3_29	GND	SP3_26	SP3_27	GND
8	GND	SP10_2	SP10_3	GND	SP10_0	SP10_1	GND
9	GND	SP10_6	SP10_7	+1.5V	SP10_4	SP10_5	GND
10	GND	SP10_10	SP10_11	GND	SP10_8	SP10_9	GND
11	GND	SP10_14	SP10_15	GND	SP10_13	SP10_31	GND
12	GND	SP10_12	SP10_19	+1.5V	SP10_16	SP10_17	GND
13	GND	SP10_20	SP10_24	GND	SP10_18	SP10_22	GND
14	GND	SP10_25	SP10_21	GND	SP10_23	SP10_26	GND
15	GND	SP10_29	SP10_30	+1.5V	SP10_27	SP10_28	GND
16	GND	SP5_2	SP5_3	GND	SP5_0	SP5_1	GND
17	GND	SP5_6	SP5_7	GND	SP5_4	SP5_5	GND
18	GND	SP5_10	SP5_11	+1.5V	SP5_8	SP5_9	GND
19	GND	SP5_31	SP5_14	GND	SP5_12	SP5_13	GND
20	GND	SP5_15	SP5_18	GND	SP5_20	SP5_16	GND
21	GND	SP5_19	SP5_23	+1.5V	SP5_17	SP5_21	GND
22	GND	SP5_24	SP5_25	GND	SP5_22	SP5_30	GND
23	GND	SP5_28	SP5_29	GND	SP5_26	SP5_27	GND
24	GND	SP8_2	SP8_3	+1.5V	SP8_0	SP8_1	GND
25	GND	SP8_6	SP8_7	GND	SP8_4	SP8_5	GND

Table 8: Pin assignment of the X25 [4] backplane connector

X25	Z	A	B	C	D	E	F
1	GND	SP8_10	SP8_11	GND	SP8_8	SP8_9	GND
2	GND	SP8_14	SP8_15	GND	SP8_13	SP8_31	GND
3	GND	SP8_12	SP8_19	+1.5V	SP8_16	SP8_17	GND
4	GND	SP8_20	SP8_24	GND	SP8_18	SP8_22	GND
5	GND	SP8_25	SP8_21	GND	SP8_23	SP8_26	GND
6	GND	SP8_29	SP8_30	+1.5V	SP8_27	SP8_28	GND
7	GND	SP6_2	SP6_3	GND	SP6_0	SP6_1	GND
8	GND	SP6_6	SP6_7	GND	SP6_4	SP6_5	GND
9	GND	SP6_10	SP6_11	+1.5V	SP6_8	SP6_9	GND
10	GND	SP6_31	SP6_14	GND	SP6_12	SP6_13	GND
11	GND	SP6_15	SP6_18	GND	SP6_20	SP6_16	GND
12	GND	SP6_19	SP6_23	+1.5V	SP6_17	SP6_21	GND
13	GND	SP6_24	SP6_25	GND	SP6_22	SP6_30	GND
14	GND	SP6_28	SP6_29	GND	SP6_26	SP6_27	GND
15	GND	SP7_2	SP7_3	+1.5V	SP7_0	SP7_1	GND
16	GND	SP7_6	SP7_7	GND	SP7_4	SP7_5	GND
17	GND	SP7_10	SP7_11	GND	SP7_8	SP7_9	GND
18	GND	SP7_14	SP7_15	+1.5V	SP7_13	SP7_31	GND
19	GND	SP7_12	SP7_19	GND	SP7_16	SP7_17	GND
20	GND	SP7_20	SP7_24	GND	SP7_18	SP7_22	GND
21	GND	SP7_25	SP7_21	+1.5V	SP7_23	SP7_26	GND
22	GND	SP7_29	SP7_30	GND	SP7_27	SP7_28	GND
23	GND	SP4_2	SP4_3	GND	SP4_0	SP4_1	GND
24	GND	SP4_6	SP4_7	+1.5V	SP4_4	SP4_5	GND
25	GND	SP4_10	SP4_11	GND	SP4_8	SP4_9	GND

Table 9: Pin assignment of the X26 [4] backplane connector

X26	Z	A	B	C	D	E	F
1	GND	SP4_31	SP4_14	GND	SP4_12	SP4_13	GND
2	GND	SP4_15	SP4_18	GND	SP4_20	SP4_16	GND
3	GND	SP4_19	SP4_23	+1.5V	SP4_17	SP4_21	GND
4	GND	SP4_24	SP4_25	GND	SP4_22	SP4_30	GND
5	GND	SP4_28	SP4_29	GND	SP4_26	SP4_27	GND
6	GND	SP9_2	SP9_3	+1.5V	SP9_0	SP9_1	GND
7	GND	SP9_6	SP9_7	GND	SP9_4	SP9_5	GND
8	GND	SP9_10	SP9_11	GND	SP9_8	SP9_9	GND
9	GND	SP9_14	SP9_15	+1.5V	SP9_13	SP9_31	GND
10	GND	SP9_12	SP9_19	GND	SP9_16	SP9_17	GND
11	GND	SP9_20	SP9_24	GND	SP9_18	SP9_22	GND
12	GND	SP9_25	SP9_21	+1.5V	SP9_23	SP9_26	GND
13	GND	SP9_29	SP9_30	GND	SP9_27	SP9_28	GND
14	GND	SP2_2	SP2_3	GND	SP2_0	SP2_1	GND
15	GND	SP2_6	SP2_7	+1.5V	SP2_4	SP2_5	GND
16	GND	SP2_10	SP2_11	GND	SP2_8	SP2_9	GND
17	GND	SP2_31	SP2_14	GND	SP2_12	SP2_13	GND
18	GND	SP2_15	SP2_18	+1.5V	SP2_20	SP2_16	GND
19	GND	SP2_19	SP2_23	GND	SP2_17	SP2_21	GND
20	GND	SP2_24	SP2_25	GND	SP2_22	SP2_30	GND
21	GND	SP2_28	SP2_29	+1.5V	SP2_26	SP2_27	GND
22	GND	SP11_2	SP11_3	GND	SP11_0	SP11_1	GND
23	GND	SP11_6	SP11_7	GND	SP11_4	SP11_5	GND
24	GND	SP11_10	SP11_11	+1.5V	SP11_8	SP11_9	GND
25	GND	SP11_14	SP11_15	GND	SP11_13	SP11_31	GND

Table 10: Pin assignment of the X64 [4] backplane connector

X64	Z	A	B	C	D	E	F
1	GND	SP11_12	SP11_19	GND	SP11_16	SP11_17	GND
2	GND	SP11_20	SP11_24	GND	SP11_18	SP11_22	GND
3	GND	SP11_25	SP11_21	GND	SP11_23	SP11_26	GND
4	GND	SP11_29	SP11_30	GND	SP11_27	SP11_28	GND
5	GND	Ms_to_ccb0	Ms_to_ccb1	GND	Ms_l1a_req	Ms_cfg_done	GND
6	GND	W6_0	W6_1	GND	W7_0	W7_1	GND
7	GND	W5_0	W5_1	GND	W8_0	W8_1	GND
8	GND	W4_0	W4_1	GND	W9_0	W9_1	GND
9	GND	W3_0	W3_1	GND	W10_0	W10_1	GND
10	GND	W2_0	W2_1	GND	W11_0	W11_1	GND
11	GND	W1_0	W1_1	GND	W12_0	W12_1	GND

3. Interface to the Global Muon Trigger Receiver and Output Lookup Table RAM

The interface to the GMT receiver module is based on specification [6]. The MS2005-to-GMT data format is shown in Table 11. All signals representing one muon pattern are transmitted over twisted pair cable using 68-pin SCSI-3 connectors. Four such connectors are placed on the front panel of the MS2005. All four selected muons are transmitted at 40 MHz in ranked order, with the connector 1 assigned to Muon_1 (1^{st} best), connector 2 assigned to Muon_2 (2^{nd} best) and so on. The TI SN75LVDS387 transmitters are used. Pin assignment of the connector is given in Table 12.

There is one 68-pin SCSI-3 connector and two TI SN75LVDT386 LVDS receivers on MS2005 board. One out of four GMT cables can be plugged into this connector and data saved into FIFO_D buffer (see section 5 for more details). This feature allows to test the GMT connection even if the GMT receiver module is not available.

Table 11: MS-to-GMT Data Format (per one muon pattern)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Eta0	**Quality[2..0]**			**Pt[4..0]**					**Phi[7..0]**							
33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
G	**P**	**Clk**	**G**	**SE**	**Bc0**	**Bx2**	**Bx1**	**Bx0**	**VC**	**C**	**HL**	**Eta[5..1]**				

HL – Halo Muon (0 = "positive" endcap)
VC – Valid Charge
Bx[2..0] – three least significant bits of bunch crossing counter
BC0 - Bunch Crossing Zero Flag
SE – Synchronization Error, S – sign (=charge) (1 – negative, 0 – positive)
Clock – 40Mhz synchronizing clock, G – Ground
P – Parity = XNOR[29..0]
Notes: 1) Pt[4..0] and Quality[2..0] are sent inverted, all other bits are not inverted.
2) For empty candidates (if Pt=0), all bits from 16 to 24 are set to "0", Phi[7..0]="1", Pt[4..0]="1" (after inversion), Quality[2..0]="1" (after inversion)

Table 12: MS-to-GMT 68-wire Cable Interface

Bit	Pin	Signal	Pin	Signal
0	1	Phi_0+	35	Phi_0-
1	2	Phi_1+	36	Phi_1-
2	3	Phi_2+	37	Phi_2-
3	4	Phi_3+	38	Phi_3-
4	5	Phi_4+	39	Phi_4-
5	6	Phi_5+	40	Phi_5-
6	7	Phi_6+	41	Phi_6-
7	8	Phi_7+	42	Phi_7-
8	9	Pt_0+	43	Pt_0-
9	10	Pt_1+	44	Pt_1-
10	11	Pt_2+	45	Pt_2-
11	12	Pt_3+	46	Pt_3-
12	13	Pt_4+	47	Pt_4-
13	14	Quality_0+	48	Quality_0-
14	15	Quality_1+	49	Quality_1-
15	16	Quality_2+	50	Quality_2-
16	17	Eta_0+	51	Eta_0-
17	18	Eta_1+	52	Eta_1-
18	19	Eta_2+	53	Eta_2-
19	20	Eta_3+	54	Eta_3-
20	21	Eta_4+	55	Eta_4-
21	22	Eta_5+	56	Eta_5-
22	23	HL+	57	HL-
23	24	C+	58	C-
24	25	VC+	59	VC-
25	26	BX0+	60	BX0-
26	27	BX1+	61	BX1-
27	28	BX2+	62	BX2-

28	29	BC0+	63	BC0-
29	30	SyncEr+	64	SyncEr-
30	31	Parity+	65	Parity-
31	32	40Mhz Clock+	66	40Mhz Clock-
32	33	GND	67	GND
33	34	GND	68	GND

The BC0 signal transmitted to GMT, is a logical OR of 12 BC0 inputs from all SP's; it is propagated through the MS2005 independently from the results of sorting.

Block diagram of the output data conversion scheme for one muon is shown on Fig 2. Each LUT is implemented inside the main FPGA and available for read and write over VME.

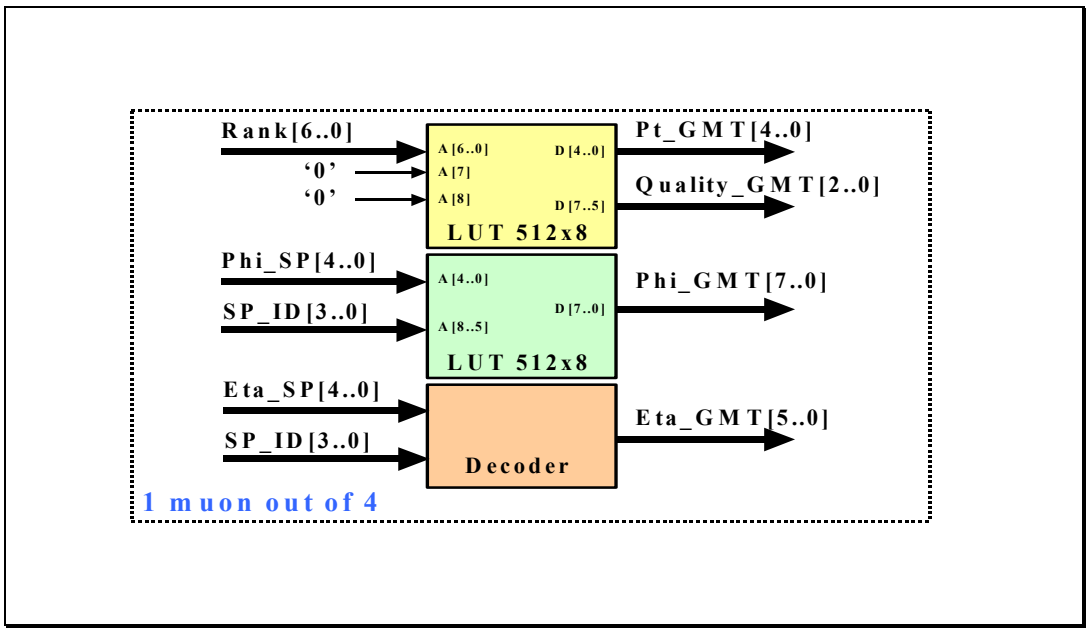

Figure 2: Block Diagram of the Output Data Conversion Scheme

More details about access to LUT are shown in Table 13. Access to all LUT RAM's is available from the VME over lines D0-D7 (Phi LUT) and D8-D15 (Rank LUT). All addresses are listed in Table 14. The SP_ID[3..0] represent the order of SP's in the TF crate, counting from the left: SP_ID=1 for SP1, SP_ID=2 for SP2 and so on.

Table 13: Access to LUT RAMs from VME

Rank LUT, 512*8 bit		**Phi LUT, 512*8 bit**	
Address	Data	Address	Data
A0 = Rank[0]	D0 = Pt[0] (VME D8 line)	A0 = Phi_SP[0]	D0 = Phi_GMT[0] (VME D0 line)
A1 = Rank[1]	D1 = Pt[1] (VME D9 line)	A1 = Phi_SP[1]	D1 = Phi_GMT[1] (VME D1 line)
A2 = Rank[2]	D2 = Pt[2] (VME D10 line)	A2 = Phi_SP[2]	D2 = Phi_GMT[2] (VME D2 line)
A3 = Rank[3]	D3 = Pt[3] (VME D11 line)	A3 = Phi_SP[3]	D3 = Phi_GMT[3] (VME D3 line)
A4 = Rank[4]	D4 = Pt[4] (VME D12 line)	A4 = Phi_SP[4]	D4 = Phi_GMT[4] (VME D4 line)
A5 = Rank[5]	D5 = Quality[0] (VME D13 line)	A5 = SP_ID[0]	D4 = Phi_GMT[5] (VME D5 line)
A6 = Rank[6]	D6 = Quality[1] (VME D14 line)	A6 = SP_ID[1]	D6 = Phi_GMT[6] (VME D6 line)
A7 = 0	D7 = Quality[2] (VME D15 line)	A7 = SP_ID[2]	D7 = Phi_GMT[7] (VME D7 line)
A8 = 0		A8 = SP_ID[3]	

3.1. Rank and Phi Look-Up Tables and Eta Decoder

The 7-bit Rank[6..0] from Sector Processors is already separated into Pt[4..0] and Quality[1..0] fields [7]. The upper two address bits are "0". So each Rank LUT outputs the data equal to the value on address bus. At this moment it is proposed that the Quality[2]=0.

We assume that SP1-SP6 belong to a "positive" endcap of the CSC system, and SP7-SP12 belong to a "negative" endcap. Then, based on [5], the Eta decoder performs the following decoding:

- for SP1-SP6: Eta_GMT[4..0] = Eta_SP[4..0], Eta_GMT[5] = 0;
- for SP7-SP12: Eta_GMT[4..0] = Eta_SP[4..0], Eta_GMT[5] = 1.

Sector 1 of the CSC system starts at phi=15 degrees, which is equal to bin 6 (with the binning in 2.5 degree intervals). Each sector covers 60 degrees, so the LUT would add 6 to Phi value for sector 1 and 7, 6+24 to Phi value for sector 2 and 8 and so on. The Phi LUT content can be summarized as:

- for SP1 and SP7: Phi_GMT[7..0] = Phi_SP[4..0] + 6
- for SP2 and SP8: Phi_GMT[7..0] = Phi_SP[4..0] + 30
- for SP3 and SP9: Phi_GMT[7..0] = Phi_SP[4..0] + 54
- for SP4 and SP10: Phi_GMT[7..0] = Phi_SP[4..0] + 78
- for SP5 and SP11: Phi_GMT[7..0] = Phi_SP[4..0] + 102
- for SP6 and SP12: Phi_GMT[7..0] = Phi_SP[4..0] + 126

4. VME Interface

The MS2005 decodes the A24 addresses when the code on address lines A[23..19] is equal to 5-bit geographical address of its slot in the TF crate. This mode requires using of J1 part of the VME64x backplane. In case of using the TF custom backplane, the MS slot is 14, and the base geographical address is 700000(hex). The MS recognizes AM codes 39(hex) and 3D(hex). Decoded addresses and VME commands are listed in Table 14. The MS2005 does not respond to byte-addressing modes, so all valid addresses must be even numbers.

Table 14: Decoded VME Addresses

Address (hex)	Access	Function
XCR3128XL PLD		
700000…70000E	Read/Write	SCANPSC100F JTAG Controller
700010	Write*	Reset SCANPSC100F controller
700012	Read/Write	CSR4 (see Table 23)
700014	Read	CSR3 (see Table 22)
700016	Write*	Generate 500 ns "Hard_Reset" pulse to the FPGA
700018	Write*	Generate "Soft_Reset" pulse to FPGA (reset all FIFO buffers, set "training pattern mode", reset RAM Address Counter (see Section 6) to "0")

XC2V4000-5FF1152C FPGA		
700100	Read/Write	FIFO_A1[15..0]. Corresponds to SP1
700102	Read/Write	FIFO_A1[31..16]. Corresponds to SP1
700104	Read/Write	FIFO_A2[15..0]. Corresponds to SP2
700106	Read/Write	FIFO_A2[31..16]. Corresponds to SP2
700108	Read/Write	FIFO_A3[15..0]. Corresponds to SP3
70010A	Read/Write	FIFO_A3[31..16]. Corresponds to SP3
70010C	Read/Write	FIFO_A4[15..0]. Corresponds to SP4
70010E	Read/Write	FIFO_A4[31..16]. Corresponds to SP4
700110	Read/Write	FIFO_A5[15..0]. Corresponds to SP5
700112	Read/Write	FIFO_A5[31..16]. Corresponds to SP5
700114	Read/Write	FIFO_A6[15..0]. Corresponds to SP6
700116	Read/Write	FIFO_A6[31..16]. Corresponds to SP6
700118	Read/Write	FIFO_A7[15..0]. Corresponds to SP7
70011A	Read/Write	FIFO_A7[31..16]. Corresponds to SP7
70011C	Read/Write	FIFO_A8[15..0]. Corresponds to SP8
70011E	Read/Write	FIFO_A8[31..16]. Corresponds to SP8
700120	Read/Write	FIFO_A9[15..0]. Corresponds to SP9
700122	Read/Write	FIFO_A9[31..16]. Corresponds to SP9
700124	Read/Write	FIFO_A10[15..0]. Corresponds to SP10
700126	Read/Write	FIFO_A10[31..16]. Corresponds to SP10
700128	Read/Write	FIFO_A11[15..0]. Corresponds to SP11
70012A	Read/Write	FIFO_A11[31..16]. Corresponds to SP11
70012C	Read/Write	FIFO_A12[15..0]. Corresponds to SP12
70012E	Read/Write	FIFO_A12[31..16]. Corresponds to SP12
700130	Read/Write	FIFO_B1[15..0]. 1st best muon transmitted to GMT
700132	Read/Write	FIFO_B1[31..16]. 1st best muon transmitted to GMT
700134	Read/Write	FIFO_B2[15..0]. 2nd best muon transmitted to GMT
700136	Read/Write	FIFO_B2[31..16]. 2nd best muon transmitted to GMT
700138	Read/Write	FIFO_B3[15..0]. 3rd best muon transmitted to GMT
70013A	Read/Write	FIFO_B3[31..16]. 3rd best muon transmitted to GMT
70013C	Read/Write	FIFO_B4[15..0]. 4th best muon transmitted to GMT
70013E	Read/Write	FIFO_B4[31..16]. 4th best muon transmitted to GMT
700140	Read/Write	FIFO_C1[15..0]. 1st best muon from the sorter output
700142	Read/Write	FIFO_C1[31..16]. 1st best muon from the sorter output
700144	Read/Write	FIFO_C2[15..0]. 2nd best muon from the sorter output
700146	Read/Write	FIFO_C2[31..16]. 2nd best muon from the sorter output
700148	Read/Write	FIFO_C3[15..0]. 3rd best muon from the sorter output
70014A	Read/Write	FIFO_C3[31..16]. 3rd best muon from the sorter output
70014C	Read/Write	FIFO_C4[15..0]. 4th best muon from the sorter output
70014E	Read/Write	FIFO_C4[31..16]. 4th best muon from the sorter output
700150	Read/Write	FIFO_D[15..0]. Input FIFO (GMT connection)
700152	Read/Write	FIFO_D[31..16]. Input FIFO (GMT connection)
700154		
700156		
700158	Read/Write	CSR0 (general purpose). See Table 19.
70015A	Read	CSR1 (FIFO full/empty status). See Table 20.
70015C	Read	CSR2 (date of the firmware version) See Table 21)
70015E	Write*	Transmit 255 words (510 frames) of data from all FIFO_A

		buffers in "Test" mode
700160	Write**	Set up fine phase adjustment for DCM1 (main clock).
700162	Write**	Set up fine phase adjustment for DCM2 (output clock to GMT).
700164	Write*	Reset PSDONE status bits from DCM1 and DCM2
700166	Write/Read	CSR7 (BXN offset)
700168	Read	CSR5 (DCM status register) See Table 24)
70016A	Write*	Set "winner bit mode"
70016C	Write*	Set "training pattern mode"
70016E	Read/Write	CSR8 (programmable delay chip 3D7408-0.25)
700170	Read/Write	CSR9 (Enable/Disable SP inputs)
700172	Write*	Reset DCM1
700174	Write*	Reset DCM2
700176		
700178	Read/Write	Access to RAM address counter (common for all RAM[4..1])
70017A	Read/Write	CSR6 (see Table 25)
70017C	Read/Write	Access to RAM buffer, selected by CSR6
70017E	Write	Send 512 bits of data from RAM[4..1] to GMT receiver at 40MHz, starting from address 0, if CSR0[10]=1.
700400-7007FE	Read/Write	Rank and Phi Look-Up Tables, Muon_1 (see Table 13)
700800-700BFE	Read/Write	Rank and Phi Look-Up Tables, Muon_2 (see Table 13)
700C00-700FFE	Read/Write	Rank and Phi Look-Up Tables, Muon_3 (see Table 13)
701000-7013FE	Read/Write	Rank and Phi Look-Up Tables, Muon_4 (see Table 13)

*** Write any data.**

**** Write "1" to increase phase shift by 1 bit. Write "0" to decrease phase shift by 1 bit.**

5. FIFO Buffers

Four groups of FIFO Buffers (FIFO_A, FIFO_B, FIFO_C and FIFO_D) are implemented in the main FPGA in order to test the MS2005 internal functionality and its communications with the SP and GMT. All buffers are 511-word deep and available from VME for read and write (Table 14). Since three muon patterns are packed into FIFO_A in two frames, each FIFO_A effectively comprises 255 patterns. Its format is shown in Table 15. FIFO_A1 corresponds to SP1, FIFO_A2 corresponds to SP2 and so on. In a "Test" mode the test patterns representing 36 muons can be send out simultaneously from all FIFO_A buffers at 80Mhz upon specific VME command (note the last word to be loaded into every FIFO_A buffer must be "0" for proper operation). They pass through the sorter that selects the four best patterns and transmits them to GMT, FIFO_B, and FIFO_C.

FIFO_B format is shown in Table 16. In a "Trigger" mode the selected patterns from the SP's act as a data sources. The outputs from the sorter (before LUT conversion) can be stored inside the FIFO_C. Its data format is shown in Table 17. Both FIFO_B and FIFO_C operate at 40Mhz (as well as the outputs to GMT). FIFO_D format is shown in Table 18. An external cable can connect one of the front panel connectors to an on-board connector P12. Thus an output data representing one selected muon can be stored in FIFO_D instead of sending to GMT. Data is loaded into FIFO_D only if at least one out of seven Pt[4..0]+Quality[1..0] bits is non-zero.

Table 15: FIFO_A Data Format

FIFO_A Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Phi_Muon_2[4..0]					Eta_Muon_1[4..0]					Phi_Muon_1[4..0]				
FIFO_A Frame 1															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SE	Bc0	Eta_Muon_3[4..0]				Phi_Muon_3[4..0]						Eta_Muon_2[4..0]			
FIFO_A Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rank_Muon_2[6..0]						HL	C	VC	Rank_Muon_1[6..0]						
FIFO_A Frame 2															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SP	Bx0	HL	C	VC	Rank_Muon_3[6..0]							HL	C	VC	

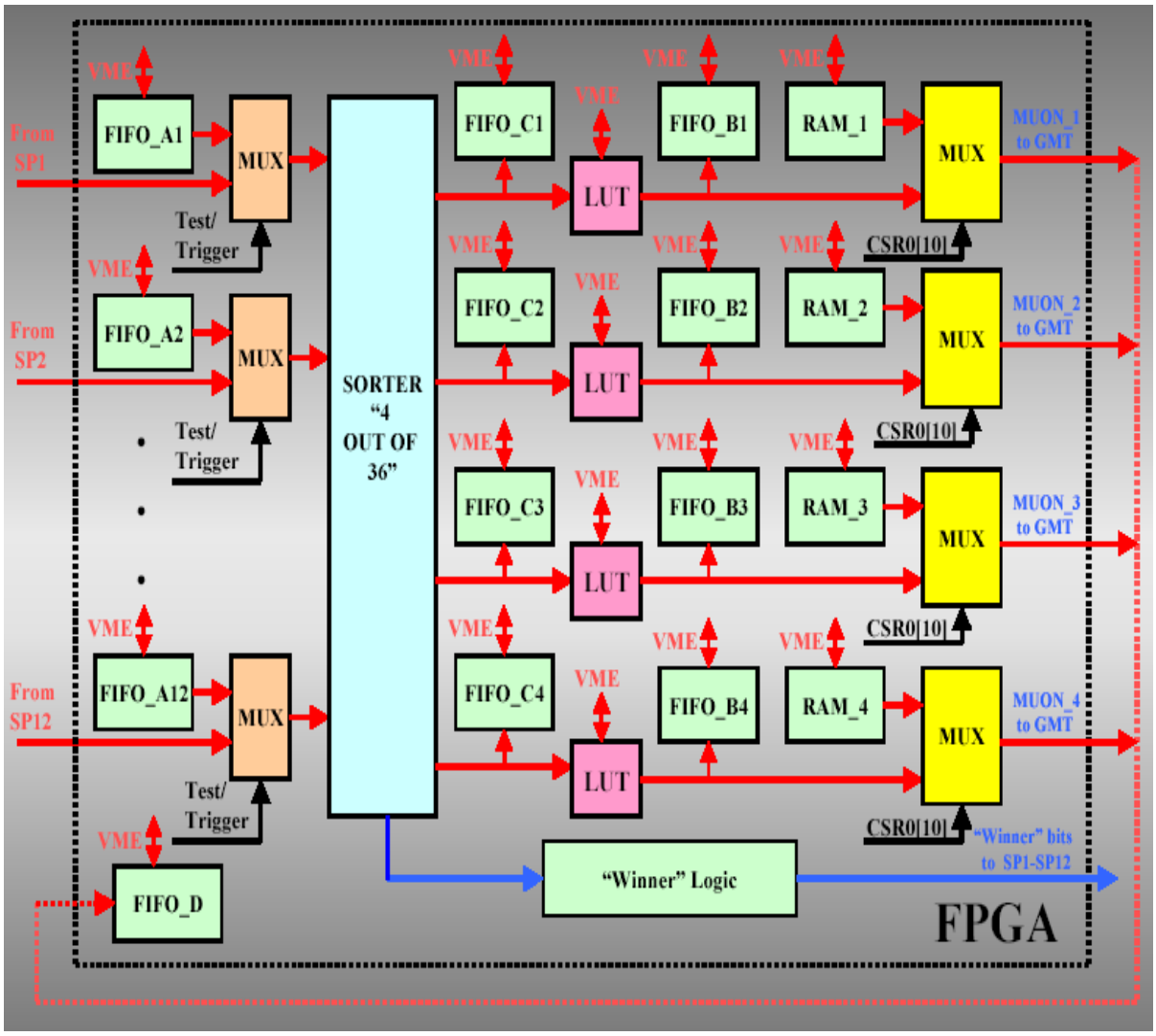

Figure 3: Block Diagram of FIFO Buffers

Table 16: FIFO_B Data Format

FIFO_B															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Quality[2..0]			**Pt[4..0]**					**Phi[7..0]**							
FIFO_B															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
"0"	**P***	**SE**	**Bc0**	**Bx2**	**Bx1**	**Bx0**	**VC**	**C**	**HL**	**Eta[5..0]**					

Note1. BX[2..0] and SE bits are entering the FIFO_B after masking (see CSR0[6..5]). See also notes 1) and 2) to Table 10.
Note 2. (*) Parity (P) is calculated for bits [29..0]. P="1" if the number of "1" is even.

Table 17: FIFO_C Data Format

FIFO_C															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Eta0	**Phi[4..0]**					**HL**	**C**	**VC**	**Rank[6..0]**						
FIFO_C															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
"0"	**"0"**	**"0"**	**"0"**	**ID3**	**ID2**	**ID1**	**ID0**	**SE**	**Bc0**	**SP**	**Bx0**	**Eta[4..1]**			

ID[3..0] bits correspond to physical slot (1 to 12, counting from the very left (slot 6) Sector Processor) of the particular SP in the TF crate.

Table 18: FIFO_D Data Format

FIFO_D															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Quality[2..0]			**Pt[4..0]**					**Phi[7..0]**							
FIFO_D															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
"0"	**P**	**SE**	**Bc0**	**Bx2**	**Bx1**	**Bx0**	**VC**	**C**	**HL**	**Eta[5..0]**					

See notes 1) and 2) in Table 16.

One important feature of all FIFO_B and FIFO_C buffers is that the data from FIFO_A ("Test" mode) or SP's ("Trigger" mode) can be saved in FIFO_B or FIFO_C only if there is at least one valid muon pattern. This allows acquiring into FIFO_B and FIFO_C the data, representing only valid patterns. The non-zero 7-bit rank indicator from the **first best selected muon after sorting** acts as "write enable" signal for all FIFO_C buffers. The non-zero 7-bit Pt[4..0]+Quality[1..0] value of the **first best selected muon after LUT** conversion acts as "write enable" signal for all FIFO_B buffers. This means that if there is just one valid pattern coming after sorting from FIFO_A or SP, it will be stored in FIFO_C1 and "0" will be written into other FIFO_C buffers. The same is true for FIFO_B buffers. This assures that all four FIFO_B and all four FIFO_C buffers will contain an equal number of words inside. As for VME access, any data can be loaded and read back out of any FIFO buffer independently.

The FULL and EMPTY flags (common to all FIFO_A[12..1], FIFO_B[4..1], FIFO_C[4..1] and FIFO_D buffers) are available for read from CSR1. Upon Soft_Reset command all EMPTY flags are set to "1" and all FULL flags are set to "0".

6. Output RAM Buffers

In order to simplify the MS-to-GMT testing procedures, four output RAM buffers RAM[4..1], 512x32 bits each (Figure 3) have been implemented. The data in these buffers represents the muon patterns that the MS2005 can directly send to GMT at 40Mhz on external signal (RAM1 represents the 1st best muon, RAM2 represents the 2nd best muon and so on). Sorter logic and RAM buffers are multiplexed on the outputs of the MS2005 with the CSR0[10] as a multiplexer control input. There is a common 9-bit address counter for all RAM buffers, accessible from the VME. Every RAM buffer is available for write and read from VME according to CSR6[7..0]. So, in order to access any specific address in a RAM the following procedures should be done:

1. Load CSR6[7..0] to select a RAM buffer.
2. Load address counter (0..1FF).
3. Write/read 16-bit data into/from selected RAM buffer.

If CSR0[10]=1, then upon write to address 70015Eh or on arriving of the Ccb_bcntres pulse from the CCB (over dedicated backplane line, see Table 1) all the 512 words from all RAM buffers will be sent out of MS2005 to GMT starting from address 0. The 12.8 us pulse generated upon this commands will also be used to load the data into FIFO_D, if the cable is connected. Bits [31..30] of every RAM buffer are actually not being sent to GMT. Bits [29..0] correspond to data format shown in Table 11. RAM content is sent to GMT without any change.

7. Control and Status Registers (CSR)

Table 19: CSR0 (inside the FPGA, general purpose register)

Bit and access	Function
0 (R/W)	FPGA Mode (Trigger mode if "0", Test mode (FIFO_A is a source of data) if "1")
1(R/W)	
2 (R/W)	
3 (R/W)	
4 (R/W)	
5 (R/W)	MASKSP (Masks SE bits from all selected patterns). Enabled if "1" and disabled if "0"
6 (R/W)	MASKCOMP (Masks all outputs of BXN comparators). Enabled if "1" and disabled if "0"
7 (R/W)	MASKER (Masks transmission of BXN[0] bit from selected muons to GMT). Enabled if "1" and disabled if "0". Bits BXN[2..1]=0.
8 (R/W)	MASKBXN (Masks transmission of BXN[2..0] bits from internal bunch crossing counter to GMT). Enabled if "1"and disabled if "0"
9 (R/W)	Enable MS_L1A_Request generation to CCB. Enabled if "1" and disabled if "0".
10 (R/W)	Source of data for the GMT (sorter logic if "0" and RAM[4..1] if "1")
11 (R/W)	-
12 (R/W)	Delay of all "winner" bits to SP, LSB
13 (R/W)	Delay of all "winner" bits to SP
14 (R/W)	Delay of all "winner" bits to SP
15 (R/W)	Delay of all "winner" bits to SP, MSB

Note: All bits in CSR0 are set to "0" after power cycling

Table 20: CSR1 (inside the FPGA, FIFO status outputs)

Bit and access	Function
0 (R)	FIFO_A FULL. Active "1" if at least one out of 12 FIFO_A buffers is full. Set to "0" after "Soft_Reset"
1(R)	FIFO_A EMPTY. Active "1" if ALL 12 FIFO_A buffers are empty. Set to "1" after "Soft_Reset"
2 (R)	FIFO_B FULL. Active "1" if at least one out of four FIFO_B buffers is full. Set to "0" after "Soft_Reset"
3 (R)	FIFO_B EMPTY. Active "1" if ALL four FIFO_B buffers are empty. Set to "1" after "Soft_Reset"
4 (R)	FIFO_C FULL. Active "1" if at least one out of four FIFO_C buffers is full. Set to "0" after "Soft_Reset"
5 (R)	FIFO_C EMPTY. Active "1" if ALL four FIFO_C buffers are empty. Set to "1" after Soft_Reset"
6 (R)	FIFO_D FULL. Active "1" if FIFO_D is full. Set to "0" after "Soft_Reset"
7 (R)	FIFO_D EMPTY. Active "1" if FIFO_D is empty. Set to "1" after "Soft_Reset"
8 (R)	"0"
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

Table 21: CSR2 (inside the main FPGA, date of the current firmware version)

Bit and access	Function
0 (R)	Day, LSB
1(R)	Day
2 (R)	Day
3 (R)	Day
4 (R)	Day, MSB
5 (R)	Month, LSB
6 (R)	Month
7 (R)	Month
8 (R)	Month, MSB
9 (R)	Year, LSB (*)
10 (R)	Year (*)
11 (R)	Year, MSB (*)
12..15 (R)	"0"

(*) The code at CSR2<11..9> should be added to 2000 to get an actual year. For example, CSR2=1252(dec) corresponds to July 4, 2002.

Table 22: CSR3 (inside control CPLD)

Bit and access	Function
0 (R)	FPGA Configuration Done and DLL locked (Active "1")
1(R)	-
2 (R)	-
3 (R)	-
4 (R)	-

5 (R)	-
6 (R)	-
7 (R)	-
8 (R)	-
9 (R)	-
10 (R)	-
11 (R)	-
12 (R)	-
13 (R)	-
14 (R)	-
15 (R)	-

Table 23: CSR4 (inside control CPLD)

Bit and access	Function
0 (R/W)	Enable (if "1") or Disable (if "0") SCANPSC100F controller. Set to "0" after power up.
1(R/W)	Enable (if "1") or Disable (if "0") "Hard_Reset" and "MS_Hard_Reset" pulses from the CCB. Set to "0" after power up
2 (R/W)	-
3 (R/W)	-
4 (R/W)	-
5 (R/W)	-
6 (R/W)	-
7 (R/W)	-
8 (R/W)	-
9 (R/W)	-
10 (R/W)	-
11 (R/W)	-
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

Note: All bits in CSR4 are set to "0" after power cycling

Table 24: CSR5 (inside the FPGA, DCM status bits)

Bit and access	Function
0 (R)	PSDONE status from DCM1
1(R)	PSDONE status from DCM2
2 (R)	STATUS[0] from DCM1
3 (R)	STATUS[1] from DCM1
4 (R)	STATUS[2] from DCM1
5 (R)	STATUS[0] from DCM2
6 (R)	STATUS[1] from DCM2
7 (R)	STATUS[2] from DCM2
8 (R)	"0"
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

Table 25: CSR6 (inside the FPGA, RAM control)

Bit and access	Function
0 (R/W)	Enable R/W from/to RAM1 (Muon_1[15..0]) if "1", disable if "0"
1(R/W)	Enable R/W from/to RAM1 (Muon_1[31..16]) if "1", disable if "0"
2 (R/W)	Enable R/W from/to RAM2 (Muon_2[15..0]) if "1", disable if "0"
3 (R/W)	Enable R/W from/to RAM2 (Muon_2[31..16]) if "1", disable if "0"
4 (R/W)	Enable R/W from/to RAM3 (Muon_3[15..0]) if "1", disable if "0"
5 (R/W)	Enable R/W from/to RAM3 (Muon_3[31..16]) if "1", disable if "0"
6 (R/W)	Enable R/W from/to RAM4 (Muon_4[15..0]) if "1", disable if "0"
7 (R/W)	Enable R/W from/to RAM4 (Muon_4[31..16]) if "1", disable if "0"
8 (R/W)	-
9 (R/W)	-
10 (R/W)	-
11 (R/W)	-
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

Note: All bits in CSR6 are set to "0" after power cycling

Table 26: CSR7 (inside the FPGA, BXN offset)

Bit and access	Function
0 (R/W)	BXN offset, LSB
1(R/W)	BXN offset
2 (R/W)	BXN offset
3 (R/W)	BXN offset
4 (R/W)	BXN offset
5 (R/W)	BXN offset
6 (R/W)	BXN offset
7 (R/W)	BXN offset
8 (R/W)	BXN offset
9 (R/W)	BXN offset
10 (R/W)	BXN offset
11 (R/W)	BXN offset
12 (R/W)	BXN offset
13 (R/W)	BXN offset
14 (R/W)	BXN offset
15 (R/W)	BXN offset, MSB

Table 27: CSR8 (inside the FPGA)

Bit and access	Function
0 (R/W)	Delay of the 40Mhz clock from the CCB (LSB) (*)
1(R/W)	Delay of the 40Mhz clock from the CCB (*)
2 (R/W)	Delay of the 40Mhz clock from the CCB (*)
3 (R/W)	Delay of the 40Mhz clock from the CCB (*)
4 (R/W)	Delay of the 40Mhz clock from the CCB (*)
5 (R/W)	Delay of the 40Mhz clock from the CCB (*)
6 (R/W)	Delay of the 40Mhz clock from the CCB (*)
7 (R/W)	Delay of the 40Mhz clock from the CCB (MSB) (*)

8 (R/W)	-
9 (R/W)	-
10 (R/W)	-
11 (R/W)	-
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

(*) – 1 step corresponds to 0.25 ns for the 3D7408-0.25 delay line
Note: All bits in CSR8 are set to "0" after power cycling

Table 28: CSR9 (inside the FPGA)

Bit and access	Function
0 (R/W)	Enable (if "0") or Disable (if "1") input data from SP1
1(R/W)	Enable (if "0") or Disable (if "1") input data from SP2
2 (R/W)	Enable (if "0") or Disable (if "1") input data from SP3
3 (R/W)	Enable (if "0") or Disable (if "1") input data from SP4
4 (R/W)	Enable (if "0") or Disable (if "1") input data from SP5
5 (R/W)	Enable (if "0") or Disable (if "1") input data from SP6
6 (R/W)	Enable (if "0") or Disable (if "1") input data from SP7
7 (R/W)	Enable (if "0") or Disable (if "1") input data from SP8
8 (R/W)	Enable (if "0") or Disable (if "1") input data from SP9
9 (R/W)	Enable (if "0") or Disable (if "1") input data from SP10
10 (R/W)	Enable (if "0") or Disable (if "1") input data from SP11
11 (R/W)	Enable (if "0") or Disable (if "1") input data from SP12
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

Note: All bits in CSR0 are set to "0" after power cycling

8. Mezzanine Board and JTAG Access to FPGA, EPROM and PLD

A mezzanine card designed for the SP board is used. It comprises one Xilinx XC2V4000-5FF1152C FPGA and four XC18V04 EPROMs, all accessible over Xilinx Parallel Cable IV using 14-pin connector P10. Pin assignment is shown in Table 29. In addition to that a fast JTAG access to FPGA and EPROMs from the VME bus is possible using 8-bit Fairchild SCANPSC100F [8] controller. There is a Xilinx CoolRunner XCR3128XL CPLD [9] that acts as a VME interface for this JTAG controller. The CPLD itself can be programmed over Xilinx Parallel Cable IV (separate 14-pin connector P11). CSR4[0] should be set to "1" in order to enable operation of the SCANPSC100F controller.

The content of the FPGA can be reloaded from four EPROM's upon VME-generated Hard_Reset unconditionally or on 500 ns "Hard_Reset" and "MS_Hard_Reset" pulses from the CCB if CSR4[1]=1. A default state after power up CSR4[1]=0, or both "Hard_Reset" commands from the CCB are disabled.

The main 40.08 Mhz clock for the mezzanine card is provided from the MS2005 board. It can be either CCB clock obtained from the backplane (when S1-1 is "on" and S1-2 is

"off") or internal 40.08Mhz clock from an on-board oscillator (when S1-2 is "on" and S1-1 is "off"). Further one of these sources may be delayed in the 3D7408-0.25 delay chip before sending to mezzanine FPGA (if S1-3 is "on" and S1-4 is "off") or sent to mezzanine FPGA directly (if S1-3 is "off" and S1-4 is "on").

Table 29: Xilinx Parallel Cable IV, connectors P10 and P11

Pin	Signal
1	GND
2	+3.3V
3	GND
4	TMS
5	GND
6	TCK
7	GND
8	TDO (input in respect to target FPGA or CPLD)
9	GND
10	TDI (output in respect to target FPGA or CPLD)
11	GND
12	Not used
13	GND
14	Not used

9. Switches and Fuses

DIP switch S1 is needed to select the source of the master clock. If S1-1 is "on", the source is the 40.08 clock from the CCB. If S1-2 is "on", the source is on-board quartz oscillator (80.16 Mhz divided by 2). Only one switch S1-1 or S1-2 should be set "on". The standard option is when S1-1 is "on". The source clock selected by S1-1 or S1-2 can further delayed in 3D7408-0.25 delay chip or sent to mezzanine FPGA directly. If S1-3 is "on" and S1-4 is "off", the clock is sent through the delay chip. If S1-3 is "off" and S1-4 is "on", the clock is sent directly. Only one switch (S1-3 or S1-4) should be set "on". The default option is when S1-4 is set "on".

Fuse F5 monitors +5V from the VME J1 backplane. Fuse F3 provides +1.5V for the mezzanine card from on-board voltage regulator U52. Both are required at any time.

Fuse F4 monitors +3.3V power from J1 VME64x backplane while fuse F7 monitors +3.3V from on-board voltage regulator U54. Only one (either F7 or F4) should be installed at a time. The default option is when F4 is installed.

Fuses F1 and F2 monitor a reference voltage for the GTLP receivers (variable +0.88V…+1.0V) and GTLP terminators (+1.5V). Fuse F1 monitors +1.5V powers from the custom TF backplane while F2 monitors +1.5V from on-board voltage regulator U53. Only one should be installed at a time. The default option is when F1 is installed. Rotary potentiometer R104 allows to adjust a reference voltage for all GTLP receivers. It is recommended to set it to minimum (+0.88V).

10. Front Panel

There are the following LED's on the front panel:

- Four 68-pin connectors for communication with GMT receiver;
- Four red LEDs "MUON[1..4] (D1-D4 respectively, with one-shots) indicate a valid muon patters that was selected and passed to GMT;
- Green LED "DONE" (D13) indicates that FPGA configuration and initialization done properly and the DLL is locked;
- Yellow LED "TEST" (D6) indicates the MS2005 is in "Test" mode (CSR0[0]=1);
- Yellow LED "JTAG" (D7) indicates JTAG access from VME over SCANPSC100F;
- Yellow LED "DACK" (D5, with one-shot) indicates an access to MS over VME;
- Green LED "+5.0" (D14) indicate an active on-board power +5.0V from VME backplane
- Green LED "+3.0" (D16) indicate an active on-board power +3.3V either from VME backplane (if fuse F4 is installed) or from on-board U54 voltage regulator (if fuse F7 is installed)
- Green LED "+1.5G" (D20) indicate an active on-board power +1.5V for all GTLP backplane terminators (obtained from custom backplane if fuse F1 is installed or from on-board voltage regulator U53 if fuse F2 is installed);
- Green LED "+1.5F" (D18) indicate an active on-board +1.5V power for the FPGA core, obtained from on-board voltage regulator U52;
- Red LED "FAEM" (FIFO_A Empty) (D10) indicates that all 12 FIFO_A buffers are empty;
- Red LED "FBEM" (FIFO_B Empty) (D11) indicates that all 4 FIFO_B buffers are empty;
- Red LED "FAFL" (FIFO_A Full) (D8) indicated that at least one out of 12 FIFO_A buffers is full;
- Red LED "FBFL" (FIFO_B Full) (D9) indicates that at least one out of 4 FIFO_B buffers is full;
- Green "CLK40" LED (D12). Indicates that the 40Mhz clock is provided for the main FPGA when flashing at ~5Hz;
- Two reserved (D15 and D17) red LED's.

11. Initialization and Self Test Procedures

The initialization and testing procedures are described in [4].

References

[1] http://bonner-ntserver.rice.edu/cms/projects.html#ccb
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[5] http://www.phys.ufl.edu/~madorsky/TrackFinder/ms.dxf

[6] Specification of the Interface between the Regional Muon Triggers and the Global Muon Trigger. Version 1.00, June 8, 2004. Available at: http://wwwhephy.oeaw.ac.at/p3w/cms/trigger/globalMuonTrigger/notes/Reg_to_GMT_note_1.00_submitted.pdf
[7] http://www.phys.ufl.edu/~acosta/cms/LU-SP02_MS_Data_Format.pdf
[8] http://www.fairchildsemi.com/ds/SC/SCANPSC100F.pdf
[9] http://direct.xilinx.com/bvdocs/publications/ds016.pdf

History

08/19/2005. Initial Release.
09/28/2005. “Reset DCM1” command (Table 14) was added.
12/08/2005. Addition to Section 3 (Transparent BC0).
03/01/2007. Changed to Version 1.2. Additions to Section 2. Changes in Section 11.