The Virtex-5 Mezzanine for the MS2005 Muon Sorter Baseboard

Draft Specification Version 1.0

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April 10, 2015

Introduction

This document describes the new mezzanine card designed for the Muon Sorter MS2005 baseboard [1]. Its block diagram is shown in Fig.1. The mezzanine comprises not only the Xilinx XC5VLX110T-FF1136C FPGA, but also the 12 channel Avago AFBR-810B optical transmitter and 12-channel Avago AFBR-820B optical receiver. A picture of the baseboard with the new mezzanine installed is shown in Fig.2. Top and bottom view of the mezzanine are shown in Fig.3.

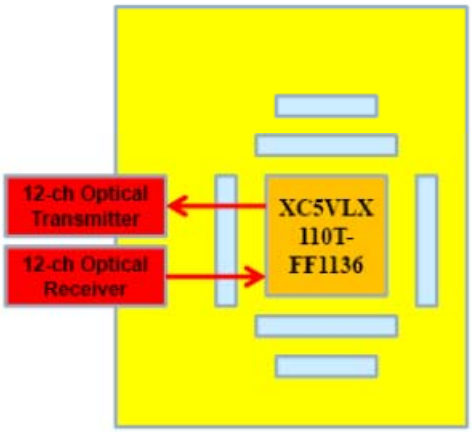

Figure 1: Block Diagram of the mezzanine

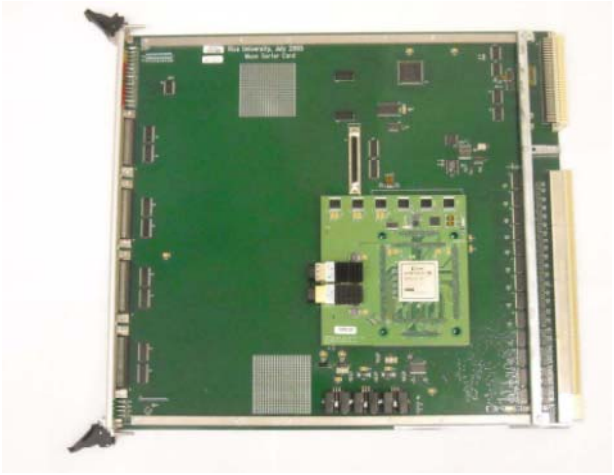

Figure 2: Baseboard with the new mezzanine

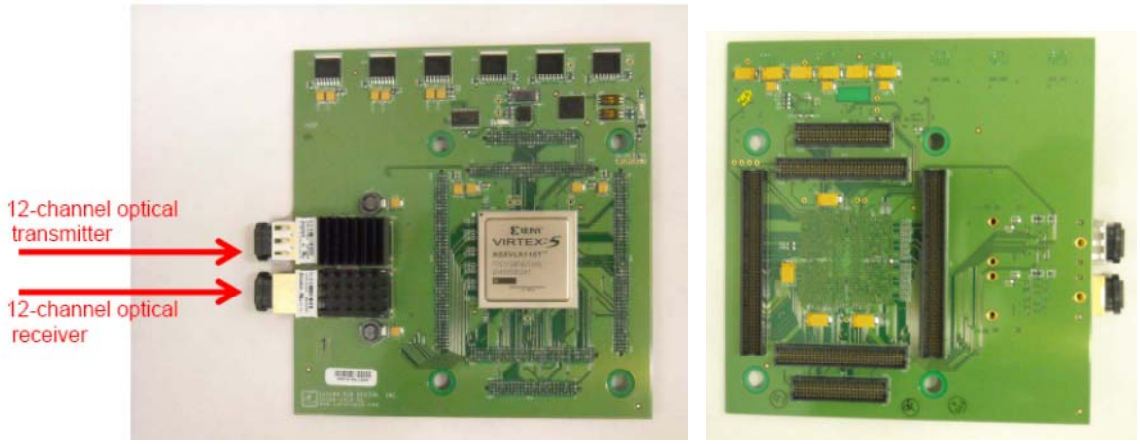

Figure 3: Top (left) and bottom (right) views of the Virtex-5 mezzanine board

1. FPGA and EPROM

Xilinx XC5VLX110T-2FFG1136C FPGA with the Xilinx XCF32PFCG48C PROM reside on this mezzanine board. They are accessible via the JTAG bus either from Xilinx connector on the base MS2005 baseboard or from the VME using SCANPSC100F JTAG Controller, also residing on the baseboard. Switch SW2 on the mezzanine board specifies the FPGA configuration mode (Table 1).

Table 1

SW2-1	SW2-2	FPGA configuration mode	M[2:0]	Data Bus width	CCLK direction
on	**on**	**Master SelectMAP (default)**	**100**	**8**	**Output**
off	**on**	**JTAG**	**101**	**1**	**Input (TCK)**
on	**off**	**Slave SelectMAP**	**110**	**8**	**Input**
off	**off**	**Slave Serial**	**111**	**1**	**Input**

The FPGA in a JTAG chain can be bypassed using switch SW1 (Table 2).

Table 2

SW1-1	SW1-2	FPGA chain
off	**off**	**Do not use**
on	**off**	**PROM**
off	**on**	**FPGA (1st device in chain) + PROM (2nd device in chain) (default option)**
on	**on**	**Do not use**

All the communications between the FPGA and the base MS2005 board are implemented via the six Samtec MOLC type connectors (2 125-pin MOLC-125-61-L-Q-LC, 2 135-pin MOLC-135-61-L-Q-LC and 2 150-pin MOLC-150-61-L-Q-LC).

The main 40.08Mhz clock arrives from the baseboard and acts as an input to the QPLL [2] device. The QPLL produces low-jitter 40.08MHz, 80.16Mhz, and 160.32MHz clocks in LVDS levels. The 160.32Mhz clock is provided directly to the MGTREFCLK inputs of 12 out of 16 GTP blocks available in the FPGA. The other 4 blocks are not used. The 40.08MHz clock from the QPLL is used in the FPGA. The 80.16Mhz output of the QPLL is not used anywhere in the design.

There are 4 GTP block currently instantiated in the design. Data transmission rate is set to 3.2Gbps.

2. External Interfaces

The Virtex-5 firmware supports all the interfaces of the MS2005 baseboard, similarly to the original Virtex-2 mezzanine [1]. They include:

- Clock and Control Board interface as described in [1]
- Interface to 12 Sector Processors as described in [1]
- Interface to Global Muon Trigger as described in [1]
- VME Slave interface as described in [1] with minor modifications (Section 3)

3. Sorting Logic

The sorting unit has been ported from the Virtex-2 design [1] to Virtex-5 without modifications.

4. VME Interface

The MS2005 decodes the A24 addresses when the code on address lines A[23..19] is equal to 5-bit geographical address of its slot in the CSC Track Finder crate. This mode requires using of J1 part of the VME64x backplane. In case of using the TF custom backplane, the MS slot is 14, and the base geographical address is 700000(hex). The MS recognizes AM codes 39(hex) and 3D(hex). Decoded addresses and VME commands are listed in Table 3. The MS2005 does not respond to byte-addressing modes, so all valid addresses must be even numbers. The functionality added in the Virtex-5 design is shown in red.

Table 3: Decoded VME Addresses

Address (hex)	Access	Function
XCR3128XL PLD		
700000…70000E	Read/Write	SCANPSC100F JTAG Controller
700010	Write*	Reset SCANPSC100F controller
700012	Read/Write	CSR4
700014	Read	CSR3
700016	Write*	Generate 500 ns “Hard_Reset” pulse to the FPGA
700018	Write*	Generate “Soft_Reset” pulse to FPGA (reset all FIFO buffers, set “training pattern mode”, reset RAM Address Counter to “0”)
XC2V4000-5FF1152C FPGA		
700100 (0)	Read/Write	FIFO_A1[15..0]. Corresponds to SP1
700102 (1)	Read/Write	FIFO_A1[31..16]. Corresponds to SP1
700104 (2)	Read/Write	FIFO_A2[15..0]. Corresponds to SP2
700106 (3)	Read/Write	FIFO_A2[31..16]. Corresponds to SP2
700108 (4)	Read/Write	FIFO_A3[15..0]. Corresponds to SP3
70010A (5)	Read/Write	FIFO_A3[31..16]. Corresponds to SP3
70010C (6)	Read/Write	FIFO_A4[15..0]. Corresponds to SP4
70010E (7)	Read/Write	FIFO_A4[31..16]. Corresponds to SP4
700110 (8)	Read/Write	FIFO_A5[15..0]. Corresponds to SP5
700112 (9)	Read/Write	FIFO_A5[31..16]. Corresponds to SP5
700114 (10)	Read/Write	FIFO_A6[15..0]. Corresponds to SP6
700116 (11)	Read/Write	FIFO_A6[31..16]. Corresponds to SP6
700118 (12)	Read/Write	FIFO_A7[15..0]. Corresponds to SP7
70011A (13)	Read/Write	FIFO_A7[31..16]. Corresponds to SP7
70011C (14)	Read/Write	FIFO_A8[15..0]. Corresponds to SP8
70011E (15)	Read/Write	FIFO_A8[31..16]. Corresponds to SP8
700120 (16)	Read/Write	FIFO_A9[15..0]. Corresponds to SP9
700122 (17)	Read/Write	FIFO_A9[31..16]. Corresponds to SP9
700124 (18)	Read/Write	FIFO_A10[15..0]. Corresponds to SP10
700126 (19)	Read/Write	FIFO_A10[31..16]. Corresponds to SP10
700128 (20)	Read/Write	FIFO_A11[15..0]. Corresponds to SP11
70012A (21)	Read/Write	FIFO_A11[31..16]. Corresponds to SP11

70012C (22)	Read/Write	FIFO_A12[15..0]. Corresponds to SP12
70012E (23)	Read/Write	FIFO_A12[31..16]. Corresponds to SP12
700130 (24)	Read/Write	FIFO_B1[15..0]. 1st best muon transmitted to GMT
700132 (25)	Read/Write	FIFO_B1[31..16]. 1st best muon transmitted to GMT
700134 (26)	Read/Write	FIFO_B2[15..0]. 2nd best muon transmitted to GMT
700136 (27)	Read/Write	FIFO_B2[31..16]. 2nd best muon transmitted to GMT
700138 (28)	Read/Write	FIFO_B3[15..0]. 3rd best muon transmitted to GMT
70013A (29)	Read/Write	FIFO_B3[31..16]. 3rd best muon transmitted to GMT
70013C (30)	Read/Write	FIFO_B4[15..0]. 4th best muon transmitted to GMT
70013E (31)	Read/Write	FIFO_B4[31..16]. 4th best muon transmitted to GMT
700140 (32)	Read/Write	FIFO_C1[15..0]. 1st best muon from the sorter output
700142 (33)	Read/Write	FIFO_C1[31..16]. 1st best muon from the sorter output
700144 (34)	Read/Write	FIFO_C2[15..0]. 2nd best muon from the sorter output
700146 (35)	Read/Write	FIFO_C2[31..16]. 2nd best muon from the sorter output
700148 (36)	Read/Write	FIFO_C3[15..0]. 3rd best muon from the sorter output
70014A (37)	Read/Write	FIFO_C3[31..16]. 3rd best muon from the sorter output
70014C (38)	Read/Write	FIFO_C4[15..0]. 4th best muon from the sorter output
70014E (39)	Read/Write	FIFO_C4[31..16]. 4th best muon from the sorter output
700150 (40)	Write	GTPRESET_IN, all GTP blocks
700152 (41)	Write	PRBSCNTRESET[0-1]_IN, all GTP blocks
700154 (42)	Read	CSR10 (GTP status register)
700156 (43)	Read	CSR11 (Status of GTP links)
700158 (44)	Read/Write	CSR0 (general purpose)
70015A (45)	Read	CSR1 (FIFO full/empty status)
70015C (46)	Read	CSR2 (date of the firmware version)
70015C (46)	Write	CSR11 (test register)
70015E (47)	Write*	Transmit 255 words (510 frames) of data from all FIFO_A buffers in “Test” mode
70015E (47)	Read	FIFO_E[15..0] from GTP1
700160 (48)	Write**	Set up fine phase adjustment for DCM1 (main clock).
700160 (48)	Read	FIFO_F[15..0] from GTP2
700162 (49)	Write**	Set up fine phase adjustment for DCM2 (output clock to GMT).
700162 (49)	Read	FIFO_G[15..0] from GTP3
700164 (50)	Write*	Reset PSDONE status bits from DCM1 and DCM2
700164 (50)	Read	FIFO_H[15..0] from GTP4
700166 (51)	Write/Read	CSR7 (BXN offset)
700168 (52)	Read	CSR5 (DCM status register)
70016A (53)	Write*	Set “winner bit mode”
70016C (54)	Write*	Set “training pattern mode”
70016E (55)	Read/Write	CSR8 (programmable delay chip 3D7408-0.25 on the baseboard)
700170 (56)	Read/Write	CSR9 (Enable/Disable SP inputs)
700172 (57)	Write*	Reset DCM1 (internal clocks)
700174 (58)	Write*	Reset DCM2 (external 40Mhz clock to GMT)
	Read	The value of the counter of words that have been sent from output RAM to GMT
700176 (59)	Write*	Resets “Send data from output RAM on the first BCReset or first BC0 only” mode
700178 (60)	Read/Write	Access to RAM address counter (common for all RAM[4..1])

70017A (61)	Read/Write	CSR6
70017C (62)	Read/Write	Access to RAM buffer, selected by CSR6
70017E (63)	Write*	Send patters from RAM[4..1] to GMT receiver at 40MHz, starting from address 0, if CSR0[10]=1.
700180 (64)	Read	Rate Counter_1[15:0], muon 1
700182 (65)	Read	Rate Counter_1[31:16], muon 1
700184 (66)	Read	Rate Counter_2[15:0], muon 2
700186 (67)	Read	Rate Counter_2[31:16], muon 2
700188 (68)	Read	Rate Counter_3[15:0], muon 3
70018A (69)	Read	Rate Counter_3[31:16], muon 3
70018C (70)	Read	Rate Counter_4[15:0], muon 4
70018E (71)	Read	Rate Counter_4[31:16], muon 4
700190 (72)	Write*	Reset all Rate Counters
700400-7007FE	Read/Write	Rank and Phi Look-Up Tables, Muon_1
700800-700BFE	Read/Write	Rank and Phi Look-Up Tables, Muon_2
700C00-700FFE	Read/Write	Rank and Phi Look-Up Tables, Muon_3
701000-7013FE	Read/Write	Rank and Phi Look-Up Tables, Muon_4

*** Write any data.**

**** Write "1" to increase phase shift by 1 bit. Write "0" to decrease phase shift by 1 bit.**

5. FIFO Buffers

Several groups of FIFO Buffers are implemented in the Virex-5 FPGA in order to test the MS2005 internal functionality and its communications with the SP and GMT. All buffers are 511-word deep and available from VME for read and write (Table 3).

FIFO_A, FIFO_B, and FIFO_C are implemented the same way as in the original design [1]. FIFO_A1 (along with the test register CSR11) can also be a source of input data to all GTP transmitters. CSR9[15] is used to select one of these sources to the GTPs.

FIFO_D has been removed from the design.

In the present implementation there are 4 GTP blocks instantiated. The data from GTP receivers can be stored in the new FIFO_E, FIFO_F, FIFO_G and FIFO_H buffers (Table 3).

6. Output RAM Buffers

Output RAM buffers are implemented identically to the initial design [1].

7. Control and Status Registers (CSR)

Table 4: CSR0 (inside the FPGA, general purpose register)

Bit and access	Function
0 (R/W)	FPGA Mode (Trigger mode if "0", Test mode (FIFO_A is a source of data) if "1")
1 (R/W)	-
2 (R/W)	-
3 (R/W)	-
4 (R/W)	-
5 (R/W)	MASKSP (Masks SE bits from all selected patterns). Enabled if "1" and disabled if "0"
6 (R/W)	MASKCOMP (Masks all outputs of the BXN comparators). Enabled if "1" and disabled if "0"
7 (R/W)	MASKER (Masks transmission of BXN[0] bit from selected muons to GMT). Enabled if "1" and disabled if "0". Bits BXN[2..1]=0.
8 (R/W)	MASKBXN (Masks transmission of BXN[2..0] bits from internal bunch crossing counter to GMT). Enabled if "1"and disabled if "0"
9 (R/W)	Enable MS_L1A_Request generation to CCB. Enabled if "1" and disabled if "0".
10 (R/W)	Source of data for the GMT (sorter logic if "0" and RAM[4..1] if "1")
11 (R/W)	-
12 (R/W)	Delay of all "winner" bits to SP, LSB
13 (R/W)	Delay of all "winner" bits to SP
14 (R/W)	Delay of all "winner" bits to SP
15 (R/W)	Delay of all "winner" bits to SP, MSB

Note: All bits in CSR0 are set to "0" after power cycling

Table 5: CSR1 (inside the FPGA, FIFO status outputs)

Bit and access	Function
0 (R)	FIFO_A FULL. Active "1" if at least one out of 12 FIFO_A buffers is full. Set to "0" after "Soft_Reset"
1 (R)	FIFO_A EMPTY. Active "1" if ALL 12 FIFO_A buffers are empty. Set to "1" after "Soft_Reset"
2 (R)	FIFO_B FULL. Active "1" if at least one out of four FIFO_B buffers is full. Set to "0" after "Soft_Reset"
3 (R)	FIFO_B EMPTY. Active "1" if ALL four FIFO_B buffers are empty. Set to "1" after "Soft_Reset"
4 (R)	FIFO_C FULL. Active "1" if at least one out of four FIFO_C buffers is full. Set to "0" after "Soft_Reset"
5 (R)	FIFO_C EMPTY. Active "1" if ALL four FIFO_C buffers are empty. Set to "1" after Soft_Reset"
6 (R)	"0"
7 (R)	"0"
8 (R)	"0"
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

Table 6: CSR2 (inside the main FPGA, date of the current firmware version)

Bit and access	Function
0 (R)	Day, LSB
1 (R)	Day
2 (R)	Day
3 (R)	Day
4 (R)	Day, MSB
5 (R)	Month, LSB
6 (R)	Month
7 (R)	Month
8 (R)	Month, MSB
9 (R)	Year, LSB (*)
10 (R)	Year (*)
11 (R)	Year (*)
12 (R)	Year, MSB (*)
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

(*) The code at CSR2<12..9> should be added to 2000 to get an actual year. For example, CSR2=1252(dec) corresponds to July 4, 2002.

Table 7: CSR3 (inside the control CPLD)

Bit and access	Function
0 (R)	FPGA Configuration Done and DLL locked (Active "1")
1 (R)	-
2 (R)	-
3 (R)	-
4 (R)	-
5 (R)	-
6 (R)	-
7 (R)	-
8 (R)	-
9 (R)	-
10 (R)	-
11 (R)	-
12 (R)	-
13 (R)	-
14 (R)	-
15 (R)	-

Table 8: CSR4 (inside the control CPLD)

Bit and access	Function
0 (R/W)	Enable (if "1") or Disable (if "0") SCANPSC100F controller. Set to "0" after power up.
1 (R/W)	Enable (if "1") or Disable (if "0") "Hard_Reset" and "MS_Hard_Reset" pulses from the CCB. Set to "0" after power up
2 (R/W)	-
3 (R/W)	-
4 (R/W)	-
5 (R/W)	-
6 (R/W)	-
7 (R/W)	-
8 (R/W)	-
9 (R/W)	-

10 (R/W)	-
11 (R/W)	-
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

Note: All bits in CSR4 are set to "0" after power cycling

Table 9: CSR5 (inside the FPGA, DCM status bits)

Bit and access	Function
0 (R)	PSDONE status from DCM1
1 (R)	PSDONE status from DCM2
2 (R)	STATUS[0] from DCM1
3 (R)	STATUS[1] from DCM1
4 (R)	STATUS[2] from DCM1
5 (R)	STATUS[0] from DCM2
6 (R)	STATUS[1] from DCM2
7 (R)	STATUS[2] from DCM2
8 (R)	CONTROL5 input from the CPLD
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

Table 10: CSR6 (inside the FPGA, RAM control)

Bit and access	Function
0 (R/W)	Enable R/W from/to RAM1 (Muon_1[15..0]) if "1", disable if "0"
1 (R/W)	Enable R/W from/to RAM1 (Muon_1[31..16]) if "1", disable if "0"
2 (R/W)	Enable R/W from/to RAM2 (Muon_2[15..0]) if "1", disable if "0"
3 (R/W)	Enable R/W from/to RAM2 (Muon_2[31..16]) if "1", disable if "0"
4 (R/W)	Enable R/W from/to RAM3 (Muon_3[15..0]) if "1", disable if "0"
5 (R/W)	Enable R/W from/to RAM3 (Muon_3[31..16]) if "1", disable if "0"
6 (R/W)	Enable R/W from/to RAM4 (Muon_4[15..0]) if "1", disable if "0"
7 (R/W)	Enable R/W from/to RAM4 (Muon_4[31..16]) if "1", disable if "0"
8 (R/W)	Enable to send data from output RAM on BCReset command from CCB2004 if "1" and disable if "0"
9 (R/W)	Enable to send data from output RAM on the first arriving BCReset command only if "1"; Enable to send data from output RAM on every BCReset command if "0"
10 (R/W)	Enable to send data from output RAM on the BC0 command if "1" and disable if "0"
11 (R/W)	Enable to send data from output RAM on the first arriving BC0 command only if "1"; Enable to send data from output RAM on every BC0 command if "0"
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	Enable data loading into FIFO_D from external cable according to bits CSR6[11:8]. The source is the sorting unit.

Note: All bits in CSR6 are set to "0" after power cycling

Table 11: CSR7 (inside the FPGA, BXN offset)

Bit and access	Function
0 (R/W)	BXN offset, LSB
1 (R/W)	BXN offset
2 (R/W)	BXN offset
3 (R/W)	BXN offset
4 (R/W)	BXN offset
5 (R/W)	BXN offset
6 (R/W)	BXN offset
7 (R/W)	BXN offset
8 (R/W)	BXN offset
9 (R/W)	BXN offset
10 (R/W)	BXN offset
11 (R/W)	BXN offset
12 (R/W)	BXN offset
13 (R/W)	BXN offset
14 (R/W)	BXN offset
15 (R/W)	BXN offset, MSB

Note: All bits in CSR7 are set to "0" after power cycling

Table 12: CSR8 (inside the FPGA)

Bit and access	Function
0 (R/W)	Delay of the 40Mhz clock from the CCB (LSB) (*)
1 (R/W)	Delay of the 40Mhz clock from the CCB (*)
2 (R/W)	Delay of the 40Mhz clock from the CCB (*)
3 (R/W)	Delay of the 40Mhz clock from the CCB (*)
4 (R/W)	Delay of the 40Mhz clock from the CCB (*)
5 (R/W)	Delay of the 40Mhz clock from the CCB (*)
6 (R/W)	Delay of the 40Mhz clock from the CCB (*)
7 (R/W)	Delay of the 40Mhz clock from the CCB (MSB) (*)
8 (R/W)	-
9 (R/W)	-
10 (R/W)	-
11 (R/W)	-
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

(*) – 1 step corresponds to 0.25 ns for the 3D7408-0.25 delay line
Note: All bits in CSR8 are set to "0" after power cycling

Table 13: CSR9 (inside the FPGA)

Bit and access	Function
0 (R/W)	Enable (if "0") or Disable (if "1") input data from SP1
1 (R/W)	Enable (if "0") or Disable (if "1") input data from SP2
2 (R/W)	Enable (if "0") or Disable (if "1") input data from SP3
3 (R/W)	Enable (if "0") or Disable (if "1") input data from SP4
4 (R/W)	Enable (if "0") or Disable (if "1") input data from SP5
5 (R/W)	Enable (if "0") or Disable (if "1") input data from SP6
6 (R/W)	Enable (if "0") or Disable (if "1") input data from SP7
7 (R/W)	Enable (if "0") or Disable (if "1") input data from SP8
8 (R/W)	Enable (if "0") or Disable (if "1") input data from SP9
9 (R/W)	Enable (if "0") or Disable (if "1") input data from SP10

10 (R/W)	Enable (if “0”) or Disable (if “1”) input data from SP11
11 (R/W)	Enable (if “0”) or Disable (if “1”) input data from SP12
12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	Multiplex data to the inputs of GTP receivers. If “0” the source is FIFO_D. If “1” the source is a test register CSR11.

Note: All bits in CSR9 are set to “0” after power cycling

Table 14: CSR10 (inside the FPGA)

Bit and access	Function
0 (R/W)	RXENMCOMMAALIGN[0-1]_IN, all GTP blocks
1 (R/W)	RXENPCOMMAALIGN[0-1]_IN, all GTP blocks
2 (R/W)	-
3 (R/W)	-
4 (R/W)	-
5 (R/W)	-
6 (R/W)	-
7 (R/W)	TXCHARISK[0-1]_IN[0], all GTP blocks
8 (R/W)	TXCHARISK[0-1]_IN[1], all GTP blocks
9 (R/W)	LOOPBACK[0-1][0], all GTP blocks
10 (R/W)	LOOPBACK[0-1][1], all GTP blocks
11 (R/W)	LOOPBACK[0-1][2], all GTP blocks
12 (R/W)	RXENPRBSTST[0-1]_IN[0], all GTP blocks
13 (R/W)	RXENPRBSTST[0-1]_IN[1], all GTP blocks
14 (R/W)	-
15 (R/W)	-

Note: All bits in CSR9 are set to “0” after power cycling

Table 15: CSR11 (inside the FPGA)

Bit and access	Function
0 (R/W)	“0”
1 (R/W)	“0”
2 (R/W)	“0”
3 (R/W)	“0”
4 (R/W)	“0”
5 (R/W)	“0”
6 (R/W)	“0”
7 (R/W)	“0”
8 (R/W)	RESETDONE[1] from GTP1
9 (R/W)	RESETDONE[2] from GTP2
10 (R/W)	RESETDONE[3] from GTP3
11 (R/W)	RESETDONE[4] from GTP4
12 (R/W)	“0”
13 (R/W)	“0”
14 (R/W)	“0”
15 (R/W)	“0”

9. Power distribution and voltage regulators

The sources of power for the mezzanine components are listed in the Table 16 below.

Table 16

Voltage	Source	Load(s)
+3.3V	Baseboard through 8 pins of XP2 and XP3	FPGA: VCCO; CMOS logic, XCF32P PROM, voltage regulators, optical parts
+1.5V	Baseboard through 8 pins of XP2 and XP3	Not used
+2.5V	Micrel MIC69502 voltage regulator (U7)	QPLL, optical parts
+2.5VAUX	Micrel MIC69502 voltage regulator (U9)	FPGA: VCCAUX
+1.2VGTP	Micrel MIC69502 voltage regulator (U8)	FPGA:MGTAVTTX, MGTAVTTRX, MGTAVTTRXC, MGTAVCCPLL
+1.8V	Micrel MIC69502 voltage regulator (U12)	XCF32P PROM
+1.0AVCC	Micrel MIC69502 voltage regulator (U10)	FPGA: MGTAVCC
+1.0VINT	Micrel MIC69502 voltage regulator (U11)	FPGA: VCCINT

10. LED's

- Green LED D1 is "on" when the QPLL is locked
- Green LED D2 is "on" when the FPGA "DONE" output is "high" (successful configuration from the PROM)

11. Test Points

TP1: +2.5V power
TP2: 40.08Mhz clock from the baseboard (input to QPLL)
TP3: TMS (JTAG)
TP4: TCK (JTAG)
TP5: TDO (JTAG)
TP6: TDI (JTAG)
TP7: pin H13 of the FPGA
TP8: pin E14 of the FPGA
TP9: pin A33 of the FPGA
TP10: BUSY (PROM)
TP11: GND
TP12: GND

References

[1] MS2005 Specification http://padley.rice.edu/cms/MS2005_090709.pdf
[2] QPLL Manual. http://padley.rice.edu/cms/qpllManual13.pdf

History

04/10/2015. Initial release