MUON TESTER BOARD FOR THE CSC MUON PORT CARD AND MUON SORTER

MT'2004 Specification

Rice University

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Abstract

This document describes the functionality of the MT'2004 board intended for testing of the custom backplane interfaces of the Muon Port Card (MPC) [1] and Muon Sorter (MS) [2] boards.

Introduction

The MPC board residing in the middle of the EMU peripheral crate will be getting data from up to nine Trigger Motherboards (TMB) [3] over custom peripheral backplane. The MS board residing in the middle of the Track Finder (TF) crate will be getting data from up to 12 Sector Processors (SP) [4]. Both custom backplanes utilize the 32-bit data transmission at 80Mhz from the TMB to the MPC and from the SP to the MS using GTLP logic levels. Full test of the MPC and MS would require 9 TMB's and 12 SP's boards installed. In some cases (especially during production testing of the MPC and MS) it would be more convenient to use a simple TMB or SP emulator that can provide the same data stream and timing. The proposed Muon Tester (MT'2004) board may be housed in any (peripheral or TF) crate and produce a data patterns from internal memory that represent either TMB or SP output format. The MT'2004 is fully programmable from VME. The proposed MT board can also be used for testing of the Clock and Control Board (CCB) [5].

Block diagram of the MT'2004 is shown on Figure 1. It comprises the VME drivers and receivers, CCB receivers, GTLP transmitters to MPC and MS and the FPGA that performs all the control functions.

1. CCB Interface

The MT'2004 receives the main 40.08Mhz clock, ccb_cmd[5..0], ccb_cmd_strobe and some other optional signals from the CCB. The clock comes over LVDS lines, all other signals – over GTLP lines. Pin assignment of the 55-pin connector to CCB is shown in Table 1. The location of the CCB connector on both TMB and SP cards in respect to VME connector is the same, so the MT'2004 is compatible with both crates. An internal 40.08Mhz clock from on-board oscillator can be used for board debugging when the

CCB is unavailable. During normal operation the MT should always getting a clock from the CCB. The list of commands decoded from the ccb_cmd[5..0] bus is shown in Table 2.

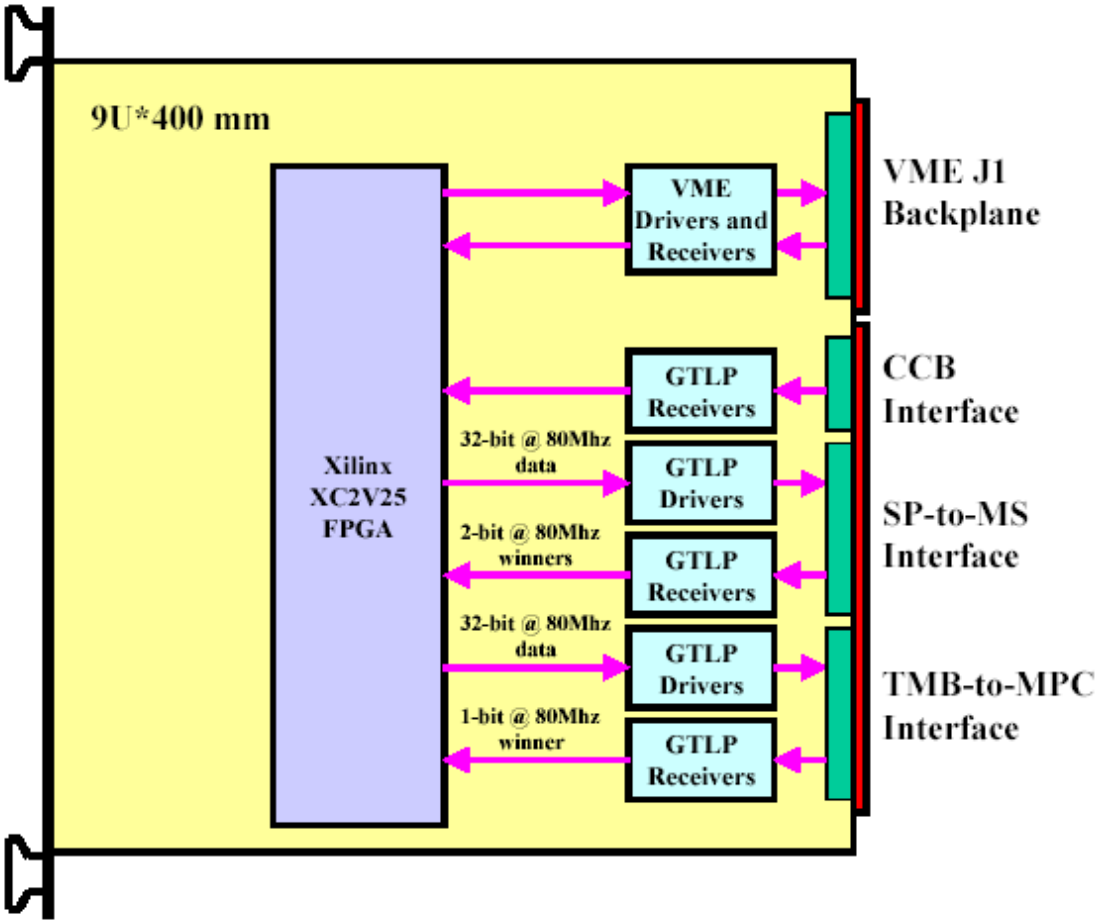

Figure 1. Block Diagram of the MT'2004

Table 1: CCB Connector, peripheral and TF crates

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Ccb_clock+	B1	Ccb_clock-	C1	GND	D1	Conf_done	E1	
A2	Ccb_clken	B2	Ccb_reserv4	C2	GND	D2		E2	
A3	Ccb_cmd0	B3	Ccb_cmd1	C3	GND	D3	Ccb_cmd2	E3	Ccb_cmd3
A4	Ccb_cmd4	B4	Ccb_cmd5	C4	GND	D4	Ccb_evcntres	E4	Ccb_bcntres
A5	Ccb_cmd_str	B5	Ccb_bc0	C5	GND	D5	Ccb_l1a	E5	
A6		B6		C6	GND	D6		E6	
A7		B7		C7	GND	D7		E7	
A8	Ccb_ready	B8	Ccb_reserv1	C8	GND	D8	Ccb_reserv2	E8	Ccb_reserv3
A9		B9		C9	GND	D9		E9	
A10		B10		C10	GND	D10		E10	
A11		B11		C11	GND	D11		E11	

Table 2: Decoded CCB Commands

Command	Code (hex)	Description
Inject patterns from TMBs	24	Inject test patterns from FIFO_A to MPC
Inject patterns from SP	2F	Inject test patterns from FIFO_B to MS

2. TMB Interface

Data that represents patterns from the TMB can be loaded into FIFO_A that is 32-bit wide and 511 word deep. Then the data from FIFO_A can be sent out of MT'2004 at 80Mhz on CCB (Table 2) or VME (Table 8) command. Two Fairchild GTLP16612MEA LVTTL-to-GTLP transmitters (same as on TMB board) are used for the backplane connection. Pin assignment of the TMB connector and data format are given in Tables 3 and 4 respectively.

The "winner" bit from the MPC can be accepted into FIFO_C that is 1-bit wide and 511 word deep. The "winner" arrives at 80Mhz as well and can be latched into the FPGA with an adjustable (in respect to the main clock from CCB) input clock. Clock adjustments can be done dynamically over VME, see Table 8 and [6].

Table 3: TMB Connector, peripheral crate

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Tmb_data0	B1	Tmb_data1	C1	GND	D1	Tmb_data2	E1	Tmb_data3
A2	Tmb_data4	B2	Tmb_data5	C2	GND	D2	Tmb_data6	E2	Tmb_data7
A3	Tmb_data8	B3	Tmb_data9	C3	GND	D3	Tmb_data10	E3	Tmb_data11
A4	Tmb_data12	B4	Tmb_data13	C4	GND	D4	Tmb_data14	E4	Tmb_data15
A5	Tmb_data16	B5	Tmb_data17	C5	GND	D5	Tmb_data18	E5	Tmb_data19
A6	Tmb_data20	B6	Tmb_data21	C6	GND	D6	Tmb_data22	E6	Tmb_data23
A7	Tmb_data24	B7	Tmb_data25	C7	GND	D7	Tmb_data26	E7	Tmb_data27
A8	Tmb_data28	B8	Tmb_data29	C8	GND	D8	Tmb_data30	E8	Tmb_data31
A9	Tmb_winner	B9		C9	GND	D9		E9	
A10		B10		C10	GND	D10		E10	
A11		B11		C11	GND	D11		E11	

Table 4: TMB-to-MPC data Format

First frame transmitted at 80MHz			Second frame transmitted at 80Mhz		
Bit	Signal	LCT	Bit	Signal	LCT
0	Wire Group_0	0	0	½-strip_0	0
1	Wire Group_1	0	1	½-strip_1	0
2	Wire Group_2	0	2	½-strip_2	0
3	Wire Group_3	0	3	½-strip_3	0
4	Wire Group_4	0	4	½-strip_4	0
5	Wire Group_5	0	5	½-strip_5	0
6	Wire Group_6	0	6	½-strip_6	0
7	CLCT Pattern_ID0	0	7	½-strip_7	0
8	CLCT Pattern_ID1	0	8	L/R Bend Angle	0
9	CLCT Pattern_ID2	0	9	SYNC_ER	0
10	CLCT Pattern_ID3	0	10	BXN[0]	0
11	Quality_0 (used for sorting)	0	11	BC0	0
12	Quality_1 (used for sorting)	0	12	CSC_ID0	0
13	Quality_2 (used for sorting)	0	13	CSC_ID1	0
14	Quality_3 (used for sorting)	0	14	CSC_ID2	0
15	Valid Pattern Flag	0	15	CSC_ID3	0
16	Wire Group_0	1	16	½-strip_0	1
17	Wire Group_1	1	17	½-strip_1	1
18	Wire Group_2	1	18	½-strip_2	1

19	Wire Group_3	1	19	½-strip_3	1
20	Wire Group_4	1	20	½-strip_4	1
21	Wire Group_5	1	21	½-strip_5	1
22	Wire Group_6	1	22	½-strip_6	1
23	CLCT Pattern_ID0	1	23	½-strip_7	1
24	CLCT Pattern_ID1	1	24	L/R_Bend Angle	1
25	CLCT Pattern_ID2	1	25	SYNC_ER	1
26	CLCT Pattern_ID3	1	26	BXN[0]	1
27	Quality_0 (used for sorting)	1	27	BC0	1
28	Quality_1 (used for sorting)	1	28	CSC_ID0	1
29	Quality_2 (used for sorting)	1	29	CSC_ID1	1
30	Quality_3 (used for sorting)	1	30	CSC_ID2	1
31	Valid Pattern Flag	1	31	CSC_ID3	1

3. Sector Processor Interface

Data that represents patterns from the SP can be loaded into FIFO_B that is 32-bit wide and 511 word deep. Then the data from FIFO_B can be sent out of MT'2004 at 80Mhz on CCB (Table 2) or VME (Table 8) command. Two TI SN74GTLPH16912 LVTTL-to-GTLP transmitters (same as on SP board) are used for the backplane connection. Pin assignment of the SP connector and data format are given in Tables 5 and 6 respectively.

Two "winner" bits from the MS can be accepted into FIFO_D that is 2-bit wide and 511 word deep. The "winners" arrives also at 80Mhz and can be latched into the FPGA with an adjustable (in respect to the main clock from CCB) input clock. Clock adjustments can be done dynamically over VME, see Table 8 and [6]. The "winner" bit data format is given in Table 7.

Table 5: SP Connector, TF crate

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1		B1		C1	GND	D1		E1	
A2		B2		C2	GND	D2		E2	
A3		B3		C3	GND	D3		E3	
A4	Sp_win0	B4	Sp_win1	C4	GND	D4		E4	
A5	Sp_data0	B5	Sp_data1	C5	GND	D5	Sp_data2	E5	Sp_data3
A6	Sp_data4	B6	Sp_data5	C6	GND	D6	Sp_data6	E6	Sp_data7
A7	Sp_data8	B7	Sp_data9	C7	GND	D7	Sp_data10	E7	Sp_data11
A8	Sp_data12	B8	Sp_data13	C8	Sp_data31	D8	Sp_data14	E8	Sp_data15
A9	Sp_data16	B9	Sp_data17	C9	Sp_data18	D9	Sp_data19	E9	Sp_data20
A10	Sp_data21	B10	Sp_data22	C10	Sp_data23	D10	Sp_data24	E10	Sp_data25
A11	Sp_data26	B11	Sp_data27	C11	Sp_data28	D11	Sp_data29	E11	Sp_data30

Table 6: SP-to-MS Data Format

First frame transmitted at 80MHz			Second frame transmitted at 80Mhz		
Bit	Signal	Muon	Bit	Signal	Muon
0	Phi_0	1	0	Rank_0	1
1	Phi_1	1	1	Rank_1	1
2	Phi_2	1	2	Rank_2	1
3	Phi_3	1	3	Rank_3	1
4	Phi_4	1	4	Rank_4	1

5	Eta_0	1	5	Rank_5	1
6	Eta_1	1	6	Rank_6	1
7	Eta_2	1	7	VC	1
8	Eta_3	1	8	C	1
9	Eta_4	1	9	HL	1
10	Phi_0	2	10	Rank_0	2
11	Phi_1	2	11	Rank_1	2
12	Phi_2	2	12	Rank_2	2
13	Phi_3	2	13	Rank_3	2
14	Phi_4	2	14	Rank_4	2
15	Eta_0	2	15	Rank_5	2
16	Eta_1	2	16	Rank_6	2
17	Eta_2	2	17	VC	2
18	Eta_3	2	18	C	2
19	Eta_4	2	19	HL	2
20	Phi_0	3	20	Rank_0	3
21	Phi_1	3	21	Rank_1	3
22	Phi_2	3	22	Rank_2	3
23	Phi_3	3	23	Rank_3	3
24	Phi_4	3	24	Rank_4	3
25	Eta_0	3	25	Rank_5	3
26	Eta_1	3	26	Rank_6	3
27	Eta_2	3	27	VC	3
28	Eta_3	3	28	C	3
29	Eta_4	3	29	HL	3
30	BC0 *	Common to 1-3	30	BX0 *	Common to 1-3
31	SE *	Common to 1-3	31	SP *	Common to 1-3

- BC0 – Bunch Crossing Zero Flag
- BX0 – Least significant bit of the buncg crossing counter
- SE – Synchronization Error (Data out of sync)
- SP – Spare bit

Table 7: MS-to-SP "Winner" Bit Format

Line and frame	Function
Sp_win0_Frame1	"1" if Muon_1 was selected by MS from SP
Sp_win0_Frame2	"1" if Muon_3 was selected by MS from SP
Sp_win1_Frame1	"1" if Muon_2 was selected by MS from SP
Sp_win1_Frame2	"0"

4. VME Interface and Control and Status Registers (CSR)

The MT'2004 can be accessed in the VME crate using geographical addressing that utilizes the address pins GA<4-0> available on the VME64x backplane. In this mode the CCB'2004 recognizes its address space when the code on address lines A<23-19> is equal to the 5-bit geographical code of its slot. The board recognizes an AM codes 39(hex), 3A(hex), 3D(hex), 3E(hex) and supports A24D16 slave operations. The MT'2004 does not respond to byte-addressing modes, so all valid addresses must be even numbers. For example, if the board is located on slot 6, its base address is 300000(hex). The list of decoded VME commands is given in Table 8.

Table 8: VME Commands

Address	Access	Command
Base+00	R/W	CSR0, general purpose
Base+02	R	CSR1, CCB interface status
Base+04	R	CSR2, FIFO status
Base+06	R	CSR3, Date of firmware revision
Base+08	R/W	FIFO_A, TMB_data[15..0]
Base+0a	R/W	FIFO_A, TMB_data[31..16]
Base+0c	R/W	FIFO_B, SP_data[15..0]
Base+0e	R/W	FIFO_B, SP_data[31..16]
Base+10	R	FIFO_C, TMB_winner over VME_data[0]. The rest VME_data[15..1] = "0"
Base+12	R	FIFO_D, SP_winner[1..0] over VME_data[1..0]. The rest VME_data[15..2] = "0"
Base+14	R	Read L1A counter over VME_data[15..0]
Base+16	W	Start transmission from FIFO_A
Base+18	W	Start transmission from FIFO_B
Base+1a	W	Write fine phase clock shift into DCM to adjust an input clock for "winner" bits
Base+1c	W	Reset all FIFO buffers and L1A counter
Base+1e	W	Write fine phase clock shift into DCM to adjust a clock for output data to MPC/SP

4.1. CSR0

Bit	Access	Function
0	R/W	
1	R/W	
2	R/W	
3	R/W	
4	R/W	
5	R/W	
6	R/W	
7	R/W	
8	R/W	
9	R/W	
10	R/W	
11	R/W	
12	R/W	
13	R/W	
14	R/W	
15	R/W	

4.2. CSR1

Bit	Access	Function
0	R	Ccb_bcreset
1	R	Ccb_evcntres
2	R	Ccb_cmd0
3	R	Ccb_cmd1
4	R	Ccb_cmd2
5	R	Ccb_cmd3
6	R	Ccb_cmd4
7	R	Ccb_cmd5
8	R	Ccb_l1a
9	R	Ccb_bc0
10	R	Ccb_ready
11	R	Ccb_clken

12	R	Ccb_res1
13	R	Ccb_res2
14	R	Ccb_res3
15	R	Ccb_res4

4.3. CSR2

Bit	Access	Function
0	R	FIFO_A is full (active « 1 »)
1	R	FIFO_B is full (active « 1 »)
2	R	FIFO_C is full (active « 1 »)
3	R	FIFO_D is full (active « 1 »)
4	R	FIFO_A is empty (active « 1 »). Also « 1 » after power up and RESETFIFO command
5	R	FIFO_B is empty (active « 1 »). Also « 1 » after power up and RESETFIFO command
6	R	FIFO_C is empty (active « 1 »). Also « 1 » after power up and RESETFIFO command
7	R	FIFO_D is empty (active « 1 »). Also « 1 » after power up and RESETFIFO command
8	R	« 0 »
9	R	« 0 »
10	R	« 0 »
11	R	« 0 »
12	R	« 0 »
13	R	« 0 »
14	R	« 0 »
15	R	« 0 »

4.4. CSR3

Bit	Access	Function
0	R	Day, LSB
1	R	Day
2	R	Day
3	R	Day
4	R	Day, MSB
5	R	Month, LSB
6	R	Month
7	R	Month
8	R	Month, MSB
9	R	Year, LSB *
10	R	Year *
11	R	Year, MSB *
12	R	« 0 »
13	R	« 0 »
14	R	« 0 »
15	R	« 0 »

* CSR3[11..9] should be added to 2000 to get an actual year

5. JTAG Access to FPGA and EPROM

The Xilinx XC2V25-4FG456 FPGA requires one XC18V02 EPROM. Both FPGA and EPROM can be programmed over Xilinx Parallel Cable IV. A 14-bit header is placed near the FPGA on MT'2004 board.

6. On-board switches and fuses

Switch S1 is needed to configure/program the FPGA and EPROM over JTAG.

S1-1 is not used.
S1-2 and S1-3 define the configuration mode of the FPGA (see Table 9 below). Master SelectMAP mode should be chosen by default.

Table 9

S1-2	S1-3	Mode
off	off	Slave Serial
on	off	Boundary Scan
off	on	Master SelectMAP
on	on	Not used

S1-4, 5, 6 allow to change the order of EPROM and FPGA in a JTAG chain (Table 10).

Table 10

S1-4	S1-5	S1-6	JTAG chain
on	off	on	XC18V02VQ44C EPROM + XC2V250-FG456 FPGA
on	on	off	XC18V02VQ44C EPROM
All others			Not effective

S1-7 controls the HSWAP_EN pin of the FPGA. If "on", it activates the internal pull-up for user i/o in the device prior to configuration. By default, HSWAP_EN is tired "1" with internal pull-up resistor.

S1-8 (when "on") allows to reconfigure the FPGA from EPROM on "Hard_reset" commands.

Switch S2 allows to chose the clock source for the FPGA. The source is a backplane clock from CCB when S2-1 is "on" and on-board oscillator when S2-2 is "on". Only one switch (either S2-1 or S2-2) should be "on".

S3 should be used only for debugging purposes. It allows to select the geographical addresses GA[4..0] when VME64x backplane is not available.

Switches S5 and S6 allows to select the operational mode of output GTLP transmitters to SP (S5) and TMB (S6). The mode is transparent when S5-2 (or S6-2) is "on" and clocked (with 80Mhz clock produced by DCM in the FPGA) when S5-1 (or S6-1) is "on".

When S4-1 is "on", the on-board oscillator turns off. S4-2 is not used.

Fuse F3 must be installed at any time, it provides +5V power from VME backplane. Fuse F2 provides +3.3V power from the VME64x backplane, while F4 provides +3.3V from on-board voltage regulator U23. Only one (by default, F2) should be installed. Fuse F1 is

needed to provide +1.5V for the FPGA core and GTLP termination (winner bits). It should be installed at any time.

7. Front Panel

There are 18 LEDs on the front panel:

- +3.3V (D17) , +5V (D16), +1.5V (D18) active on-board powers (green)
- "DONE" (D1) FPGA configuration from EPROM done successfully (green)
- "LOCK" (D2) FPGA DLL's have been locked (green)
- "DACK" (D3) indicates VME access to MT (green, with one-shot)
- "FULA" (D4) TMB data FIFO is full (read)
- "FULB" (D5) SP data FIFO is full (read)
- "FULC" (D6) TMB "winner" FIFO is full (read)
- "FULD" (D7) SP "winner" FIFO is full (read)
- "EMPA" (D8) TMB data FIFO is empty (red)
- "EMPB" (D9) SP data FIFO is empty (red)
- "EMPC" (D10) TMB "winner" FIFO is empty (red)
- "EMPD" (D11) SP "winner" FIFO is empty (red)
- "ST_TMB" (D12) indicates start of data transmission from FIFO_A (red, with one-shot)
- "ST_SP" (D13) indicates start of data transmission from FIFO_B (red, with one-shot)
- "CLKC" (D14) indicates that the main CCB clock is OK (red). Provided by the counter inside FPGA with a frequency of ~10Hz
- "CLKV" (D15) indicates that the 16Mhz VME clock is OK (red). Provided by the counter inside FPGA with a frequency of ~10Hz

References

[1]. Muon Port Card Specification. Available at
http://bonner-ntserver.rice.edu/cms/MPC2002.pdf
[2]. Muon Sorter Specification. Available at http://bonner-ntserver.rice.edu/cms/MS2003.pdf
[3]. Trigger Motherboard Specification. Available at
http://www-collider.physics.ucla.edu/cms/trigger/tmb2003/tmb2003_spec_v1p01.pdf
[4]. Sector Processor documentation. Available at
http://www.phys.ufl.edu/~uvarov/tf_crate/interfaces.htm
[5]. Clock and Control Board documentation. Available at
http://bonner-ntserver.rice.edu/cms/projects.html#ccb
[6]. Xilinx Virtex-2 documentation is available at
http://direct.xilinx.com/bvdocs/publications/ds031-2.pdf

History

01/30/2004: Initial release
03/17/2004: Changes in Table 8.