# The CCB Mezzanine Board for GEM Electronics

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The Clock and Control Board (CCB) mezzanine described below is intended for the clock and control distribution from the Cathode Strip Chamber CCB to the Optohybrid Boards (OH) residing on a GEM chambers at CMS.

The mezzanine is located near the front panel of the CCB (Figures 1 and 2). It supports copper links up to six OH boards using standard Type A HDMI connectors and cables (Fig.3). OH1 connector in on the top and OH6 is on the bottom of the front panel.

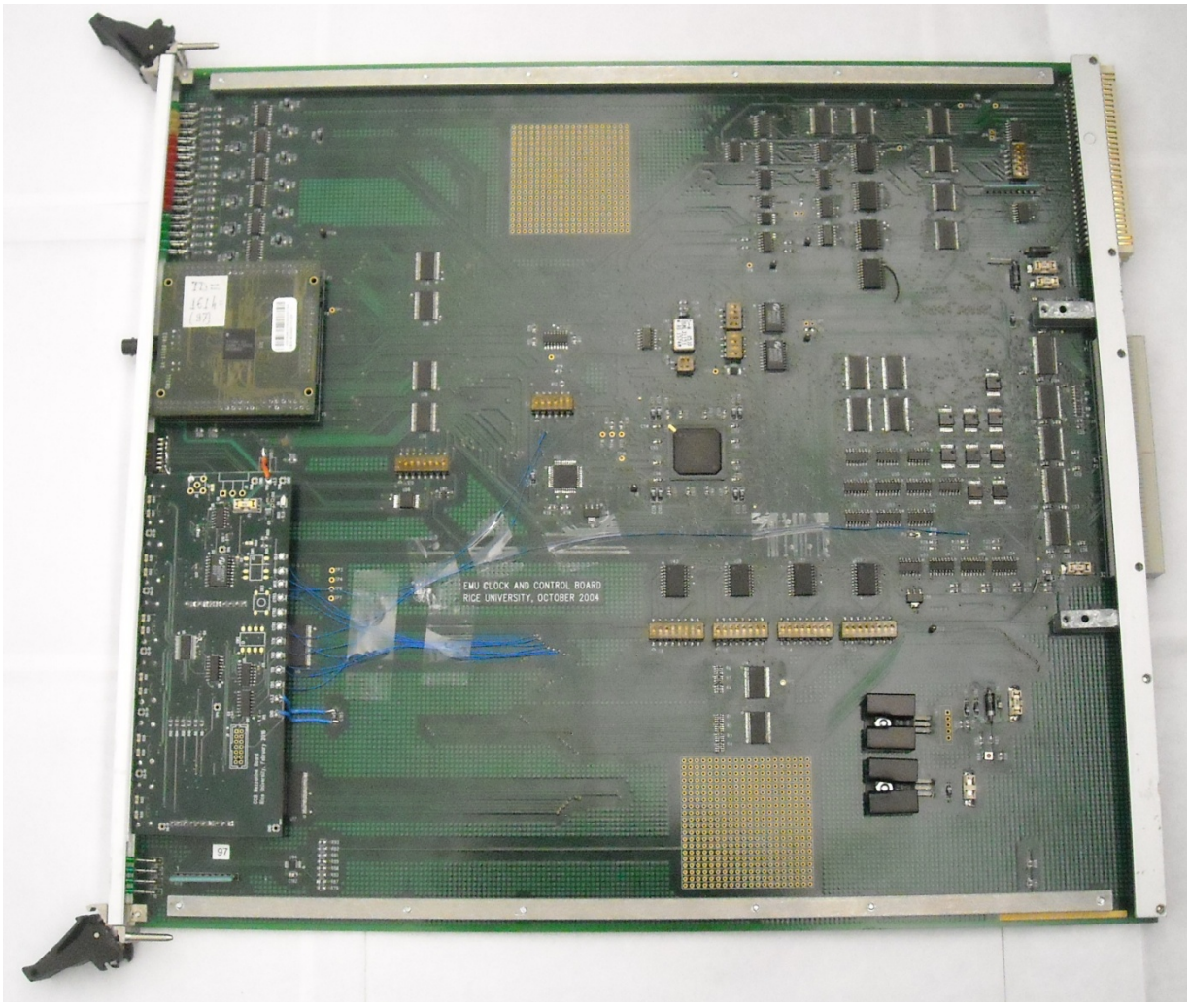


Figure 1: CCB baseboard with the mezzanine installed

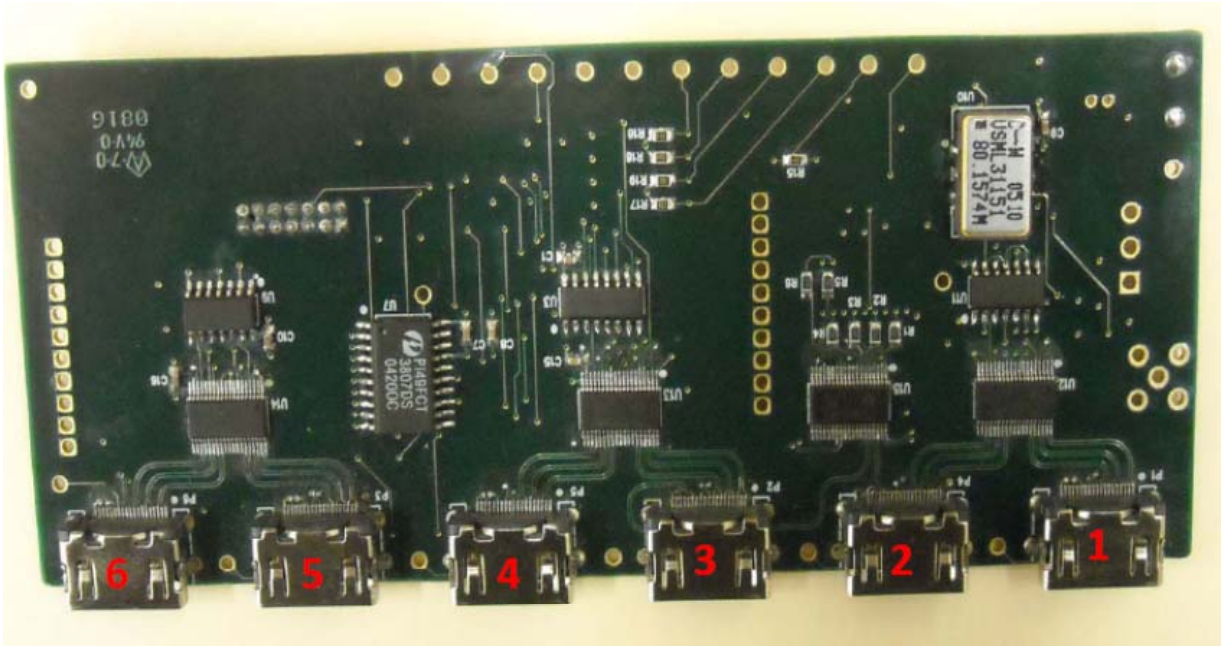


Figure 2: Mezzanine board with 6 HDMI connectors (bottom view)

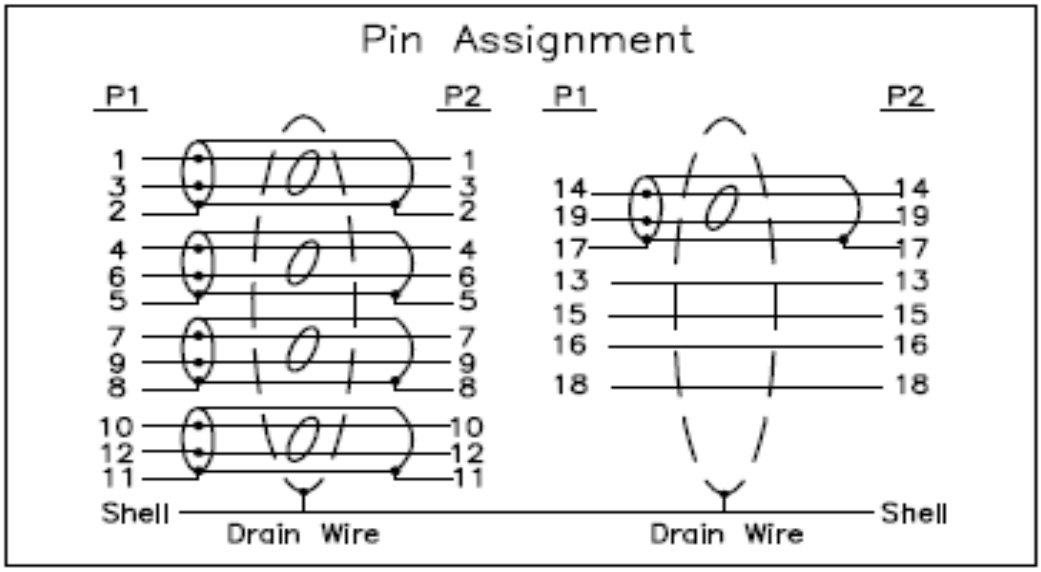


Figure 3: HDMI Type A connector

The mezzanine is connected to the CCB baseboard with 10 wires. The 3.3V power and GND are also provided from the baseboard. The mezzanine supports JTAG access to Xilinx programmable devices located on the OH (four JTAG signals TMS, TDI, TDO, TCK), provides the 40.079MHz master clock, Hard Reset (HR) signal to reload the FPGA from its PROM, and one control signal (MUX) to select the JTAG path on the OH board. The four JTAG signals and a clock are delivered to/from OH board in LVDS levels; the other two signals in 3.3V LVTTL levels. Pin assignment of the HDMI connector is shown in Table 1.

**Table 1**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | TMS+ | 6 | TDI- | 11 | Common | 16 | HR |
| 2 | Common | 7 | TCK+ | 12 | TDO- | 17 | Common |
| 3 | TMS- | 8 | Common | 13 | Not used | 18 | Not used |
| 4 | TDI+ | 9 | TCK- | 14 | Clock+ | 19 | Clock- |
| 5 | Common | 10 | TDO+ | 15 | MUX | | |

"Common" pins 2,5,8,11,17 can be connected to GND with a 0 Ohm resistor (individually for each HDMI connector; not installed by default). The four cage pins of each HDMI connector can be connected to GND with another 0 Ohm resistor as well (not installed by default).

The mezzanine can also be used in a standalone mode, with the 3.3V power provided from an external source (use connector J3). The clock source in this mode could be either an on-board oscillator (40.079MHz output) or an external LVTTL source (SMA connector). Access to JTAG signals in this mode is possible through the standard Xilinx 14-pin cable. Depending on HDMI cable length, the frequency of TCK clock should be decreased to 1.5…3MHz or even lower. The choice of the clock and a JTAG path are defined by switch SW1 (Table 2). Switch SW2 (Table 3) allows to chose a JTAG path for one of six OH1..OH6 boards. The clock is delivered to all OH boards unconditionally from the selected source. Switch SW2 should be installed and used only in a "standalone" mode. A comparison of the mezzanine and standalone modes is shown in Table 4.

**Table 2**

| | |
|---|---|
| SW1-1 "on", SW1-2 "off", SW1-3 "off" | Clock from the SMA connector |
| SW1-1 "off", SW1-2 "on", SW1-3 "off" | 40.079MHz clock from the CCB baseboard |
| SW1-1 "off", SW1-2 "off", SW1-3 "on" | 40.079MHz clock from the on-board oscillator |
| SW1-4 "off" | JTAG path from the CCB baseboard (CSRB8) |
| SW1-4 "on" | JTAG path from Xilinx connector (use SW2 to select the OH board) |

**Table 3**

| | |
|---|---|
| SW2-1 "on" | MUX="1" (use in standalone mode only) |
| SW2-1 "off" | MUX="0" (use in standalone mode only) |
| SW2-2 "off", SW2-3 "off", SW2-4 "off" | All OH1..OH6 are selected (JTAG "write" only) |
| SW2-2 "off", SW2-3 "off", SW2-4 "on" | OH6 is selected, HDMI connector P6 |
| SW2-2 "off", SW2-3 "on", SW2-4 "off" | OH5 is selected, HDMI connector P3 |
| SW2-2 "off", SW2-3 "on", SW2-4 "on" | OH4 is selected, HDMI connector P5 |
| SW2-2 "on", SW2-3 "off", SW2-4 "off" | OH3 is selected, HDMI connector P2 |
| SW2-2 "on", SW2-3 "off", SW2-4 "on" | OH2 is selected, HDMI connector P4 |
| SW2-2 "on", SW2-3 "on", SW2-4 "off" | OH1 is selected, HDMI connector P1 |
| SW2-2 "on", SW2-3 "on", SW2-4 "on" | None of OH1..OH6 is selected |

**Table 4**

| | CCB Mezzanine | Standalone |
|---|---|---|
| LHC clock | From the CCB baseboard (TTC or on-board oscillator), use DIP switch SW1 | On-board 40.079MHz clock (1), SMA connector (2); use DIP switch SW1 |
| JTAG | From the CCB baseboard (CSRB8) | Xilinx 14-pin connector (J1)<br>Molex 87831-1420 |
| Hard Reset | From the CCB baseboard | Push Button |
| Selection of OH1..OH6 | From the CCB register CSRB8 | DIP switch SW2-2,3,4 |
| MUX signal to select a GBT or CCB path on OH | From the CCB register CSRB8 | DIP switch SW2-1 |
| +3.3V Power and GND | From the CCB baseboard | 3-pin connector Molex 26-60-5030 (J3) |

In the "mezzanine" mode all the JTAG signals, MUX, and CTR[3:1] controls are provided from the CSRB8 (address 68002Eh, Table 5).

**Table 5**

| Bit | Access | Function |
|---|---|---|
| 0 | R/W | TDI signal to the OH board selected by bits[10:8] |
| 1 | R/W | TMS signal to the OH board selected by bits[10:8] |
| 2 | R/W | TCK signal to the OH board selected by bits[10:8] |
| 3 | R | TDO signal from the OH board selected by bits[10:8] |
| 4 | R/W | - |
| 5 | R/W | - |
| 6 | R/W | - |
| 7 | R/W | - |
| 8 | R/W | Control bits to select the OH board:<br>000 – None, 001 – OH1 (top HDMI connector); 010 – OH2, 011 – OH3,<br>100 – OH4, 101 – OH5, 110 – OH6 (bottom HDMI connector),<br>111 – all OH boards (for write only, doesn't apply to TDO) |
| 9 | R/W | |
| 10 | R/W | |
| 11 | R/W | MUX signal to OH board selected by bits[10:8] |
| 12 | R/W | Generate 500 ns Hard Reset pulse to all connected OH boards (write "1" once); independent from bit[13] |
| 13 | R/W | If "1" allows propagation of Hard Resets from the TTC*;<br>if "0" propagation of Hard Resets is disabled |
| 14 | R/W | - |
| 15 | R/W | - |

*Also CSRB1[0] should be "0".

The SMA connector can also be used to provide an output clock (either from on-board oscillator or from the CCB baseboard). It is recommended to turn SW1-1 “off” and add an external wire from the TP5 (U2-19) to the SMA signal pin.

## History

04/29/2016. Table 3. SW2-1 “on” and “off” reverted.