

## Optical DMB Test Firmware

### ODMB Version 2

10 May, 2013

#### 1. Addresses

| Address      | Access | Function  |
|--------------|--------|---|
| Base + FFFCh | R/W    | Discrete logic register: Bit[0]: TMS (Write)/TDO (Read), Bit[1]: TDI (Write); Bits[15:2]: not used  |
| Base + 0     | R/W    | GTX Control Register, all links. Bit[0]: RXENMCOMMAALIGN_IN; Bit[1]: RXENPCOMMAALIGN_IN; Bits[6:2]: not used, Bits[8:7]: TXCHARISK_IN[1:0]; Bits[11:9]: LOOPBACK_IN[2:0]; Bits[15:12]: not used |
| Base + 2     | R/W    | GTX PRBS Control Register, all links, Bits[3:1]: RXENPRBSTST_IN[2:0]  |
| Base + 4     | R      | Bit[0] – LVMB_SDOOUT; Bits[7:1]=0; Bits[15:8]=R_LVMB_PON[7:0]   |
| Base + 6     | R      | STATUSA(15:0) Bytes Aligned status from 12 GTX links on lines [11:0]; bits[15:12]=0   |
| Base + 8     | R      | STATUSB(15:0) Comma Detect status from 12 GTX links on lines [11:0]; bits[15:12]=0  |
| Base + a     | R      | STATUSC(15:0) PLLKDET status from 12 GTX links on lines [11:0]; bits[15:12]=0   |
| Base + c     | R      | STATUSD(15:0) RESETDONE status from 12 GTX links on lines [11:0]; bits[15:12]=0   |
| Base + e     | R      | Firmware Date (bits[4:0] – day; bits[8:5] – month; bits[12:9] – year, bits[15:13]=0)  |
| Base + 10    | W      | Reset internal buffers and FIFOs (dataless)   |
| Base + 12    | W      | Send data from FIFO_A to GTXs (dataless)  |
| Base + 14    | W      | Reset COMMADET latches for all GTX links (dataless)   |
| Base + 16    | W      | Reset PRBS error counters, all GTX links (dataless)   |
| Base + 18    | W      | GTXTXRESET_IN, GTXRXRESET_IN; Reset all GTXs (dataless)   |
| Base + 1a    | W      | PLLTXRESET_IN, PLLRXRESET_IN; Reset PLL TX/RX, all GTX links (dataless)   |
| Base + 1c    | W      | TX/RX DLYALIGNRESET, all GTX links (dataless)   |
| Base + 1e    | R/W    |   |
| Base + 20    | R      | PRBS error counter, GTX link 1  |
| Base + 22    | R      | PRBS error counter, GTX link 2  |
| Base + 24    | R      | PRBS error counter, GTX link 3  |
| Base + 26    | R      | PRBS error counter, GTX link 4  |
| Base + 28    | R      | PRBS error counter, GTX link 5  |
| Base + 2a    | R      | PRBS error counter, GTX link 6  |
| Base + 2c    | R      | PRBS error counter, GTX link 7  |
| Base + 2e    | R      | PRBS error counter, GTX link 8  |
| Base + 30    | R      | PRBS error counter, GTX link 9  |
| Base + 32    | R      | PRBS error counter, GTX link 10   |
| Base + 34    | R      | PRBS error counter, GTX link 11   |
| Base + 36    | R      | PRBS error counter, GTX link 12   |
| Base + 38    | R      | CMDREG[15:0] register from CCB. CLK=CMDSTR. Bit[0]=BCNTRES, bit[1]=EVCNTRES, Bits[7:2]=CMD[5:0], bits[15:8]=0   |
| Base + 3a    | R      | L1A counter, 16 bits  |
| Base + 3c    | R      | BC0 counter, 16 bits  |
| Base + 3e    | R      | DATREG[15:0] register from CCB. CLK=DATSTR. Bits[7:0]=DAT[7:0], bits[15:8]=0  |
| Base + 40    | W      | Reset SMON core (dataless)  |

|           |     |   |
|-----------|-----|---|
| Base + 42 |     |   |
| Base + 44 |     |   |
| Base + 46 |     |   |
| Base + 48 |     |   |
| Base + 4a |     |   |
| Base + 4c |     |   |
| Base + 4e |     |   |
| Base + 50 | W   | FIFO_A13 (output to transmitter OT1, 80MHz)   |
| Base + 52 | W   | FIFO_A14 (output to transmitter OT2, 125MHz)  |
| Base + 54 | R   | FIFO_B13 (input from receiver OT1, 80MHz)   |
| Base + 56 | R   | FIFO_B14 (input from receiver OT2, 125MHz)  |
| Base + 58 | R   | Read-only signals from DCFEBs through the PPIB board:<br>bits[6:0] – DONE[7:1], bits[7]=0, bits[14:8] – TDO[7:1], bit[15]=0   |
| Base + 5a | R/W | JTAG related signals to DCFEBs through the PPIB board:<br>bits[6:0] – TCK[7:1], bit[7] – TMS, bit[8] – TDI. <b>Bit[14] in register (Base+5c) should be “1” to allow propagation of TDI and TMS signals to PPIB.</b>   |
| Base + 5c | R/W | Timing, Trigger and Control signals to DCFEBs through the PPIB board:<br>bits[6:0] – L1A_MATCH[7:1], bit[7] – L1A, bit[8] – RESYNC, bit[9] – BC0, bit[10] – REPRGEN, bit[11] – EXTPLS, bit[12] – INJPLS, bit[13] – not used, bit[14] – V6_JTAG_SEL. <b>Bit[14] should be “1” to allow propagation of TDI and TMS signals from the register (base+5a) or 25 ns pulses (below) to PPIB. Bit[15]: if “0” the signals to PPIB are provided as described above from the registers (base+5a) and (base+5c). If “1” the signals above are 25 ns pulses (write only).</b> |
| Base + 5e |     |   |
| Base + 60 | R/W | FIFO_B1 (from RX[15:0] GTX link 1)  |
| Base + 62 | R/W | FIFO_B2 (from RX[15:0] GTX link 2)  |
| Base + 64 | R/W | FIFO_B3 (from RX[15:0] GTX link 3)  |
| Base + 66 | R/W | FIFO_B4 (from RX[15:0] GTX link 4)  |
| Base + 68 | R/W | FIFO_B5 (from RX[15:0] GTX link 5)  |
| Base + 6a | R/W | FIFO_B6 (from RX[15:0] GTX link 6)  |
| Base + 6c | R/W | FIFO_B7 (from RX[15:0] GTX link 7)  |
| Base + 6e | R/W | FIFO_B8 (from RX[15:0] GTX link 8)  |
| Base + 70 | R/W | FIFO_B9 (from RX[15:0] GTX link 9)  |
| Base + 72 | R/W | FIFO_B10 (from RX[15:0] GTX link 10)  |
| Base + 74 | R/W | FIFO_B11 (from RX[15:0] GTX link 11)  |
| Base + 76 | R/W | FIFO_B12 (from RX[15:0] GTX link 12)  |
| Base + 78 | W   | ODMB_Hard_Reset pulse to PPIB (800 ns)  |
| Base + 7a | R/W | Bit[0]=LVMB_SCLK; Bit[1]=LVMB_SDI; Bit[2]=LVMB_PONLOAD; Bit[3]=LVMB_PONOE, Bits[15:4] – N/D   |
| Base + 7c | R/W | Bits[6:0]=LVMB_CSB[6:0]; Bit[7] – N/D; Bits[15:8]=LVMB_PON[7:0]   |
| Base + 7e | R   | Status register, Bit[0]=QPLLLOCKED; Bit[1]=QPLLERROR; Bit[2]=MMCM locked; Bits[12:3]=0; Bit[13]=RX2SD; Bits[14]=0; Bit[15]=FPGA_DONE  |
|           | W   | Reset QPLL (dataless)   |

## 2. GTX links

| Bank       | Link     | Pin | ODMB assignment      |
|------------|----------|-----|----------------------|
| <b>112</b> | MGTCLK0P | AK6 | GL1_CLK_P (125MHz)   |
|            | MGTCLK0N | AK5 | GL1_CLK_N (125 MHz)  |
|            | MGTCLK1P | AH6 | -                    |
|            | MGTCLK1N | AH5 | -                    |
|            | MGTRXP0  | AP5 | GL1_RX_P             |
|            | MGTRXN0  | AP6 | GL1_RXN              |
|            | MGTTXP0  | AP1 | GL1_TXP              |
|            | MGTTXN0  | AP2 | GL1_TXN              |
|            | MGTRXP1  | AM5 | -                    |
|            | MGTRXN1  | AM6 | -                    |
|            | MGTTXP1  | AN3 | -                    |
|            | MGTTXN1  | AN4 | -                    |
|            | MGTRXP2  | AL3 | -                    |
|            | MGTRXN2  | AL4 | -                    |
|            | MGTTXP2  | AM2 | -                    |
|            | MGTTXN2  | AM2 | -                    |
|            | MGTRXP3  | AJ3 | -                    |
|            | MGTRXN3  | AJ4 | -                    |
| MGTTXP3    | AK1      | -   |                      |
| MGTTXN3    | AK2      | -   |                      |
| <b>113</b> | MGTCLK0P | AD6 | GLO_CLK_P (80.00MHz) |
|            | MGTCLK0N | AD5 | GLO_CLK_N (80.00MHz) |
|            | MGTCLK1P | AB6 | -                    |
|            | MGTCLK1N | AB5 | -                    |
|            | MGTRXP0  | AG3 | GLO_RXP              |
|            | MGTRXN0  | AG4 | GLO_RXN              |
|            | MGTTXP0  | AH1 | GLO_TXP              |
|            | MGTTXN0  | AH2 | GLO_TXN              |
|            | MGTRXP1  | AF5 | -                    |
|            | MGTRXN1  | AF6 | -                    |
|            | MGTTXP1  | AF1 | -                    |
|            | MGTTXN1  | AF2 | -                    |
|            | MGTRXP2  | AE3 | -                    |
|            | MGTRXN2  | AE4 | -                    |
|            | MGTTXP2  | AD1 | -                    |
|            | MGTTXN2  | AD2 | -                    |
|            | MGTRXP3  | AC3 | -                    |
|            | MGTRXN3  | AC4 | -                    |
| MGTTXP3    | AB1      | -   |                      |
| MGTTXN3    | AB2      | -   |                      |
| <b>114</b> | MGTCLK0P | V6  | -                    |
|            | MGTCLK0N | V5  | -                    |
|            | MGTCLK1P | T6  | -                    |





















|            |         |          |               |
|------------|---------|----------|---------------|
|            | MGCLK1N | T5       | -             |
|            | MGTRXP0 | AA3      | ORX2_05P      |
|            | MGTRXN0 | AA4      | ORX2_05N      |
|            | MGTTXP0 | Y1       | -             |
|            | MGTTXN0 | Y2       | -             |
|            | MGTRXP1 | W3       | ORX2_01P      |
|            | MGTRXN1 | W4       | ORX2_P1N      |
|            | MGTTXP1 | V1       | -             |
|            | MGTTXN1 | V2       | -             |
|            | MGTRXP2 | U3       | ORX2_04P      |
|            | MGTRXN2 | U4       | ORX2_04N      |
|            | MGTTXP2 | T1       | -             |
|            | MGTTXN2 | T2       | -             |
|            | MGTRXP3 | R3       | ORX2_02P      |
|            | MGTRXN3 | R4       | ORX2_02N      |
|            | MGTTXP3 | P1       | -             |
|            | MGTTXN3 | P2       | -             |
| <b>115</b> | MGTKL0P | P6       | QPLL_160MHZ_P |
|            | MGTKL0N | P5       | QPLL_160MHZ_N |
|            | MGTKL1P | M6       | -             |
|            | MGTKL1N | M5       | -             |
|            | MGTRXP0 | N3       | ORX2_03P      |
|            | MGTRXN0 | N4       | ORX2_03N      |
|            | MGTTXP0 | M1       | -             |
|            | MGTTXN0 | M2       | -             |
|            | MGTRXP1 | L3       | ORX2_11P      |
|            | MGTRXN1 | L4       | ORX2_11N      |
|            | MGTTXP1 | K1       | -             |
|            | MGTTXN1 | K2       | -             |
|            | MGTRXP2 | K5       | ORX2_10P      |
|            | MGTRXN2 | K6       | ORX2_10N      |
|            | MGTTXP2 | H1       | -             |
|            | MGTTXN2 | H2       | -             |
|            | MGTRXP3 | J3       | ORX2_12P      |
|            | MGTRXN3 | J4       | ORX2_12N      |
|            | MGTTXP3 | F1       | -             |
|            | MGTTXN3 | F2       | -             |
| <b>116</b> | MGTKL0P | H6       | -             |
|            | MGTKL0N | H5       | -             |
|            | MGTKL1P | F6       |               |
|            | MGTKL1N | F5       |               |
|            | MGTRXP0 | G3       | ORX2_07P      |
|            | MGTRXN0 | G4       | ORX2_07N      |
|            | MGTTXP0 | D1       | -             |
|            | MGTTXN0 | D2       | -             |
| MGTRXP1    | E3      | ORX2_08P |               |













|  |         |    |          |
|--|---------|----|----------|
|  | MGTRXN1 | E4 | ORX2_08N |
|  | MGTTXP1 | C3 | -        |
|  | MGTTXN1 | C4 | -        |
|  | MGTRXP2 | D5 | ORX2_09P |
|  | MGTRXN2 | D6 | ORX2_09N |
|  | MGTTXP2 | B1 | -        |
|  | MGTTXN2 | B2 | -        |
|  | MGTRXP3 | B5 | ORX2_06P |
|  | MGTRXN3 | B6 | ORX2_06N |
|  | MGTTXP3 | A3 | -        |
|  | MGTTXN3 | A4 | -        |

### 3. SYS\_MON Channels

| Pin | Name in the schematic symbol | Name in the Xilinx spec | Signal         |
|-----|------------------------------|-------------------------|----------------|
| G11 | L12P_SM5P_35                 | L2P_SM0P_35             | LV_P3V3_SM_P   |
| F11 | L12N_SM5N_35                 | L2N_SM0N_35             | LV_P3V3_SM_N   |
| A13 | L7P_SM4P_35                  | L3P_SM1P_35             | P5V_SM_P       |
| A14 | L7N_SM4N_35                  | L3N_SM1N_35             | P5N_SM_N       |
| F14 | L3P_SM1P_35                  | L5P_SM2P_35             | THERM2_P       |
| E14 | L3N_SM1N_35                  | L5N_SM2N_35             | THERM2_N       |
| H10 | L5P_SM2P_35                  | L6P_SM3P_35             | P3V3_PPIB_SM_P |
| G10 | L5N_SM2N_35                  | L6N_SM3N_35             | P3V3_PPIB_SM_N |
| B12 | L13P_SM6P_35                 | L7P_SM4P_35             | P2V5_SM_P      |
| B13 | L13N_SM6N_35                 | L7N_SM4N_35             | P2V5_SM_N      |
| H12 | L2P_SM0P_35                  | L12P_SM5P_35            | THERM1_P       |
| J12 | L2N_SM0N_35                  | L12N_SM5N_35            | THERM1_N       |
| A11 | L14P_SM7P_35                 | L13P_SM6P_35            | P1V0_SM_P      |
| B11 | L14N_SM7N_35                 | L13N_SM6N_35            | P1V0_SM_N      |
| E13 | L6P_SM3P_35                  | L15P_SM7P_35            | P5V_LVMB_SM_P  |
| F13 | L6N_SM3N_35                  | L15N_SM7N_35            | P5V_LVMB_SM_N  |

#### 4. LEDs

|                               |  |  |                                  |
|-------------------------------|--|--|----------------------------------|
| SD from OT1 transceiver       |   |   | SD from OT2 transceiver          |
| ENDTACK_B                     |   |   | ENJTAG_B                         |
| Data Transmission from FIFO_A |   |   | 40MHz Master CLOCK               |
| Geographical Address decoded  |   |   | VME DTACK from FPGA              |
| QPLL locked                   |   |   | VME DTACK from discrete logic    |
| MMCM locked                   |   |   | TXCLKOUT from GTX                |
| SD from SNAP12 receiver       |   |   | 160MHz clock from clock driver 1 |
| Not Used                      |   |   | 160MHz clock from clock driver 2 |
| FPGA_DONE                     |   |   | FPGA_INIT_B                      |
| QPLL error                    |  |  | QPLL locked                      |

|   |   |   |
|---|---|---|
|  |  |  |
| 5.0V_LVMB   | 1.0V  | 1.2V  |
|  |  |  |
| 1.8V  | 2.5V  | 3.3V  |
|  |  |  |
| 3.3V_VCCT   | 3.3V_VCCR   | 3.3V_ORX  |
|  |  |  |
| 5.0V_VME  | 3.3V_VME  | 3.3V_PPIB   |

## 5. Test Points

TP46: 160Mhz clock from GTX clock driver 0 (GTX\_115)

TP44: 160Mhz clock from GTX clock driver 1 (GTX\_116)

TP42: 160Mhz clock from GTX clock driver 2 (GTX\_114)

TP33: TDO1 from PPIB

TP35: TDO2 from PPIB

TP37: TDO3 from PPIB

TP39: TDO4 from PPIB

TP41: TDO5 from PPIB

TP43: TDO6 from PPIB

TP45: TDO7 from PPIB

## 6. Front Panel Push Buttons

**Top:** Hard Reset to the FPGA (reload from XCF128X)

**Middle:** The PPIB interface signals are generated as described in Section 1 (addresses base+5a and base+5c). This is a default option after power cycling (**effective for odmb\_051015 firmware version only**).

**Bottom:** Continuous generation of all PPIB signals (25 ns pulses) every 3.2 microseconds (**effective for odmb\_051013 firmware version only**).