Dear GBTx users,

Please read the following important note concerning the reliability of the high-speed data scrambling for the GBTx data input.

As you might know, it was recently discovered that the scrambling of the high-speed data sent to the GBTx can get stuck at a constant value depending on the provided user data. This usually happens when sending specific static or periodic patterns to the GBTx. In these situations, the GBTx may periodically report that certain bits have been corrected by FEC, or the GBTX CDR may experience lock loss when utilized in conjunction with the VTRx transceiver. There are several effective ways to mitigate this problem:

- Avoid sending constant patterns and repetitive constant patterns whenever feasible. For example, avoid repeatedly sending a data word A for one clock cycle and then a data word B for N-1 clock cycles.
- Frequently toggle all unused bits, such as disabled ePorts, to introduce variability in the data stream. It is crucial that these actions impact at least one bit of the data in each of the four scramblers to ensure comprehensive mitigation.
- The most beneficial way to toggle bit(s) is on a random way every clock cycle.
- Another effective way is to have one bit per scrambler carrying a >3 MHz clock. Even if this implies sending a repetitive pattern, if the frequency is high enough it can prevent the scrambler from reaching deadlock.
- The scrambler 4 has the IC and EC bits inside it. These can be toggled by sending HDLC commands to perform readings on the GBTx or GBT-SCA registers. Doing this repeatedly can already significantly reduce the chances of deadlock for this scrambler. A solution would still need to be found for the three other scramblers.

There are other types of mitigations that can reduce the problem frequency but might not totally eliminate it. These are:

- Lowering the bandwidth of the duty cycle correction loop for receivers different than the VTRx (GBTIA).
- Decreasing the GBTX CDR bandwidth through the CDR PLL filter resistor register (34[3:2]). However, in systems with relatively high levels of power supply noise, lower PLL bandwidths are likely to result in higher jitter.

You can find a detailed report in our new webpage GBT project application notes (https://gbtproject.web.cern.ch/ replaceshttps://espace.cern.ch/GBT-Project/whichwill be deprecated soon).

In case of doubt, do not hesitate to contact gbtx-support@cern.ch.

Best regards,
GBTx support team.