GE2/1 Optohybrid Board

Draft Specification ver.2.0

Rice University

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Introduction

The GE2/1 Optohybrid Version 2 (OH2) board provides readout and trigger interfaces to the GE2/1 on-chamber electronics. This is the second revision of the OH board designed in late 2019. A comprehensive description of the GE2/1 GEM design and electronics can be found in the Technical Design Report [1]. The most up-to-date information about the OH board is available in [2]. A block diagram of the OH board and its top and bottom views are shown in Figs.1-3 respectively.

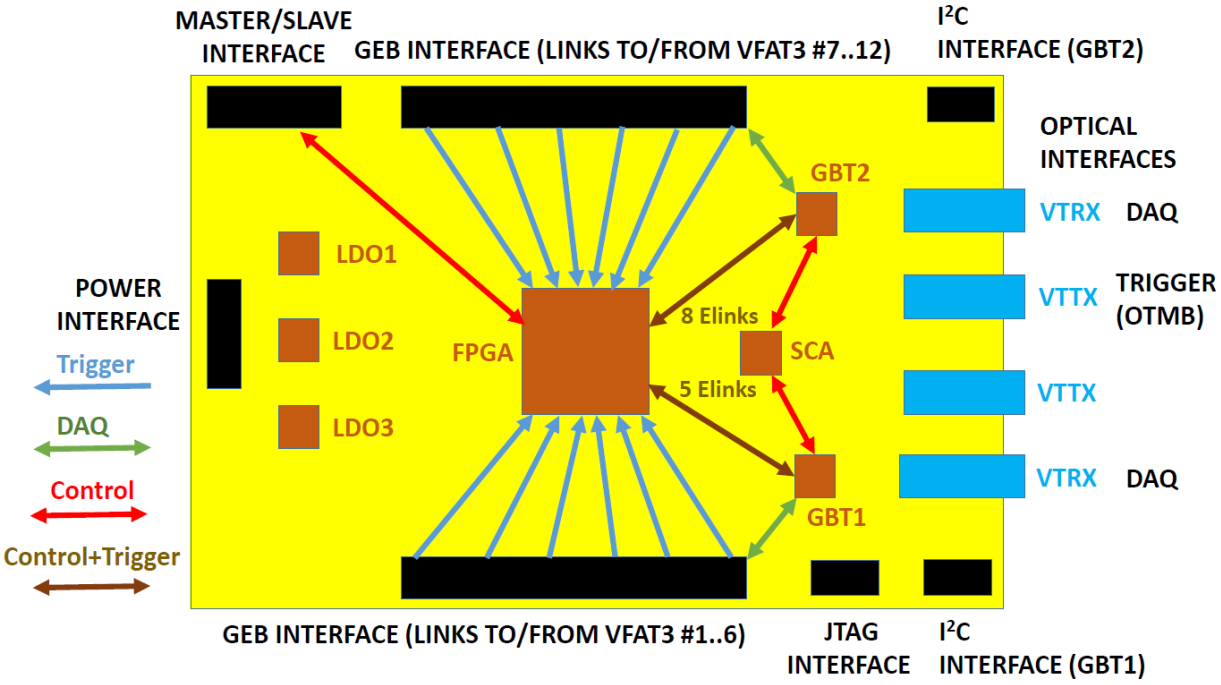


Figure 1: Block diagram of the Optohybrid board

The main tasks of the OH board are to synchronize the data sent by the VFAT3 ASICs [3], zero-suppress the trigger data in the FPGA, encode the data and send them via optical links to the backend processor farm. There is also a dedicated trigger link to the CSC Trigger Motherboard to improve the Level-1 trigger efficiency of the CSC system. The OH design is based on a custom GBT chipset [4]. There are two GBT devices, each serving 6 VFAT3 ASICs. The OH is a mezzanine card of 19 cm x 17 cm in size, residing on top of the GEM Electronic Board (GEB) [5]. The GEB provides powers connection for the OH. Three Low Dropout (LDO) regulators are used to produce low voltage powers for the FPGA.

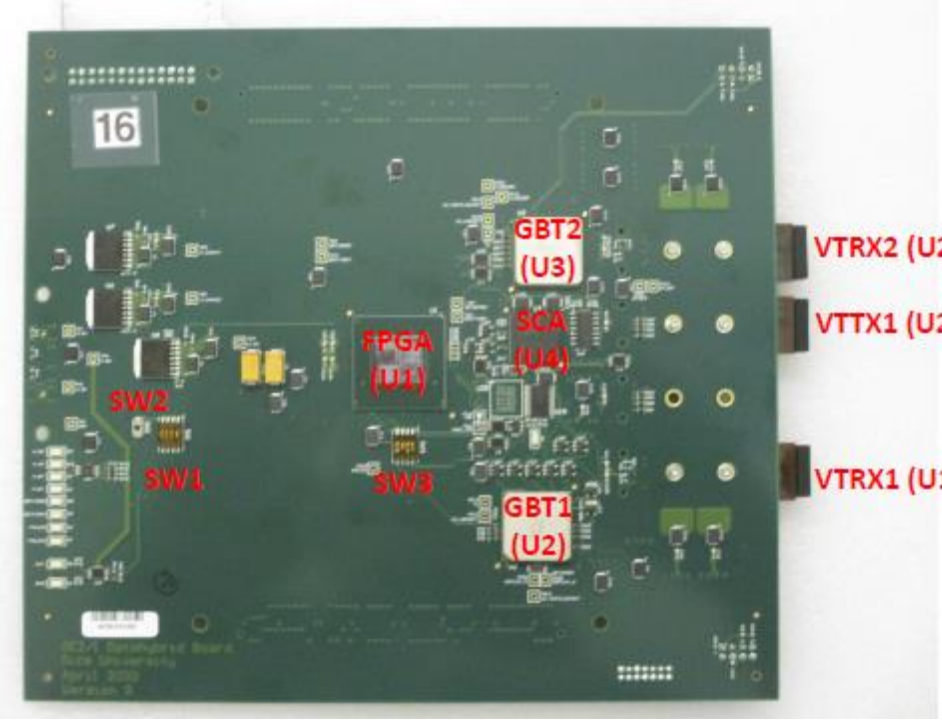


Figure 2: Top side of the OH board

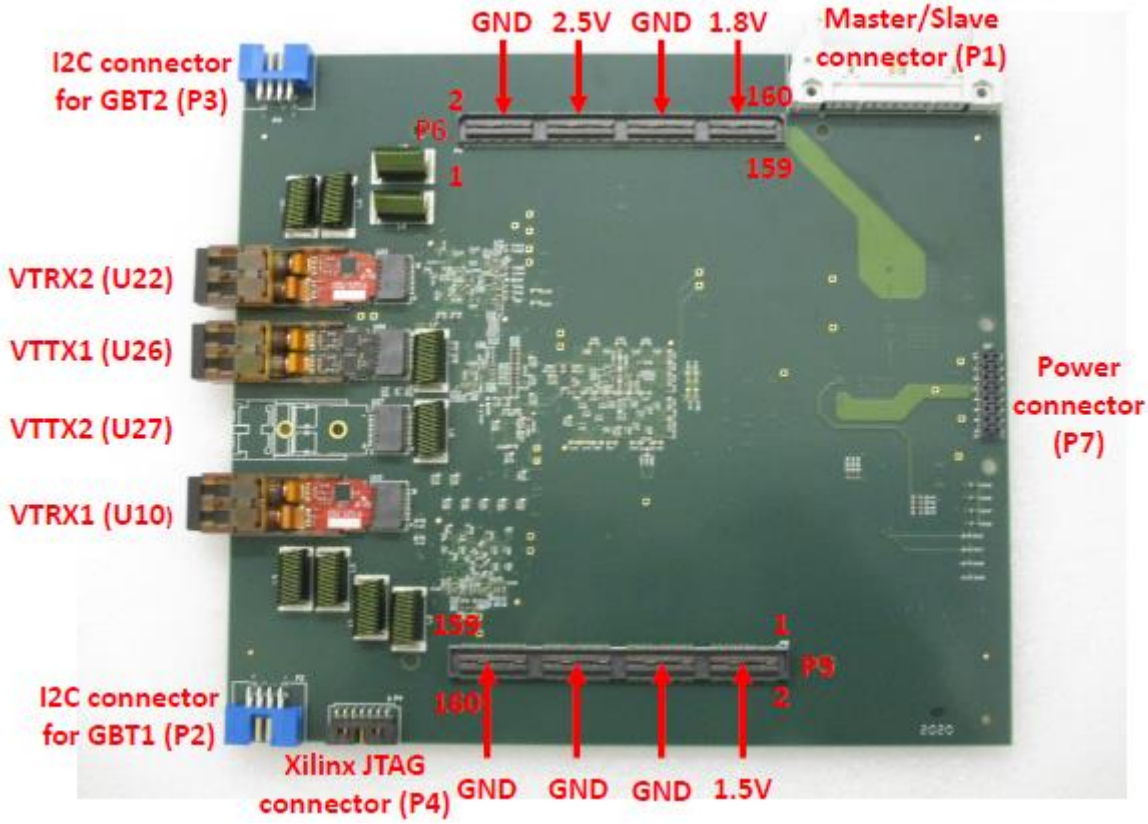


Figure 3: Bottom side of the OH board

1. FPGA

Xilinx Artix-7 XC7A200T-2FBG484C [6] (U1) has been selected due to:

- Sufficient number of Input/Output pins (285 total) and logic resources
- Low power consumption
- Flexible IODELAY block
- Low cost
- Sufficient radiation tolerance [7]-[9]

The main FPGA functions and interfaces are:

- Two Samtec QSE-080-01-L-D-A connectors are used for all links to 12 VFAT3 ASICs. Two mating Samtec QTE-080-03-L-D-A are used on the GEB baseboards. The FPGA receives 9 differential signals from each VFAT3, including 8 data bits (VFATxDyN/P, where x=1..12 and y=1..8) and one Strobe signal VFATxSTRN/P). For the optimal signal routing, some of these differential signals are inverted at the FPGA inputs.
- Banks 13,14,15,16,34,35 are used for VFAT3 connections, all VCCIO powers are 2.5V.
- Bank 0 is also powered by 2.5V. A dedicated configuration banks voltage select CFGBVS="1".
- The FPGA receives 3 status signals (GBTxRXDV, GBTxRXRDY, GBTxTXRDY, x=1,2) from each GBT ASIC [9].
- Two global clocks (FPGACLK1P/N (W19/W20, bank 14) and FPGACLK2P/N (J19/H19, bank 15) are provided from the GBT1 ASIC.
- 3 ELINKs from/to GBT1 and 8 ELINKs from/to GBT2 have been implemented. One ELINKCLK1P/N is provided from the GBT1.
- Optional Master/Slave interface (described below in Section 2) to an adjacent OH board.
- Optional Xilinx XCF32PFSG48C EPROM (not installed on production boards).
- FPGA (1st device) + optional EPROM (2nd device) in the JTAG chain, JTAG connector P4 (Molex 87833-1420) is compatible with the Xilinx JTAG cable.
- Configuration pins M0..M2 with embedded pull-ups can be grounded with a switch SW1-1..3 (Fig.4) to select the configuration mode (Slave SelectMAP is a default mode for configuration from the GBT1 ASIC; Master SelectMAP for configuration from EPROM).
- There are 4 MGT links in this FPGA. The first global clock MGTREFCLK0P/N is provided from the CLOCKDES0P/N outputs of GBT1 ASIC. The second MGTREFCLK1P/N is provided from the DCLK28P/N outputs of the GBT1 ASIC. Two MGT outputs are connected to the VTTX1 optical transmitter and the other two outputs are connected to the VTTX2 optical transmitters. MGT receivers are not used and are all grounded.
- PUDC_B input is set to "0" with the external resistor R69 to enable internal pull-ups on SelectIO pins.
- EMCCLK external master configuration clock is not used.
- Internal ADC is not used.
- The battery backup supply is not used.

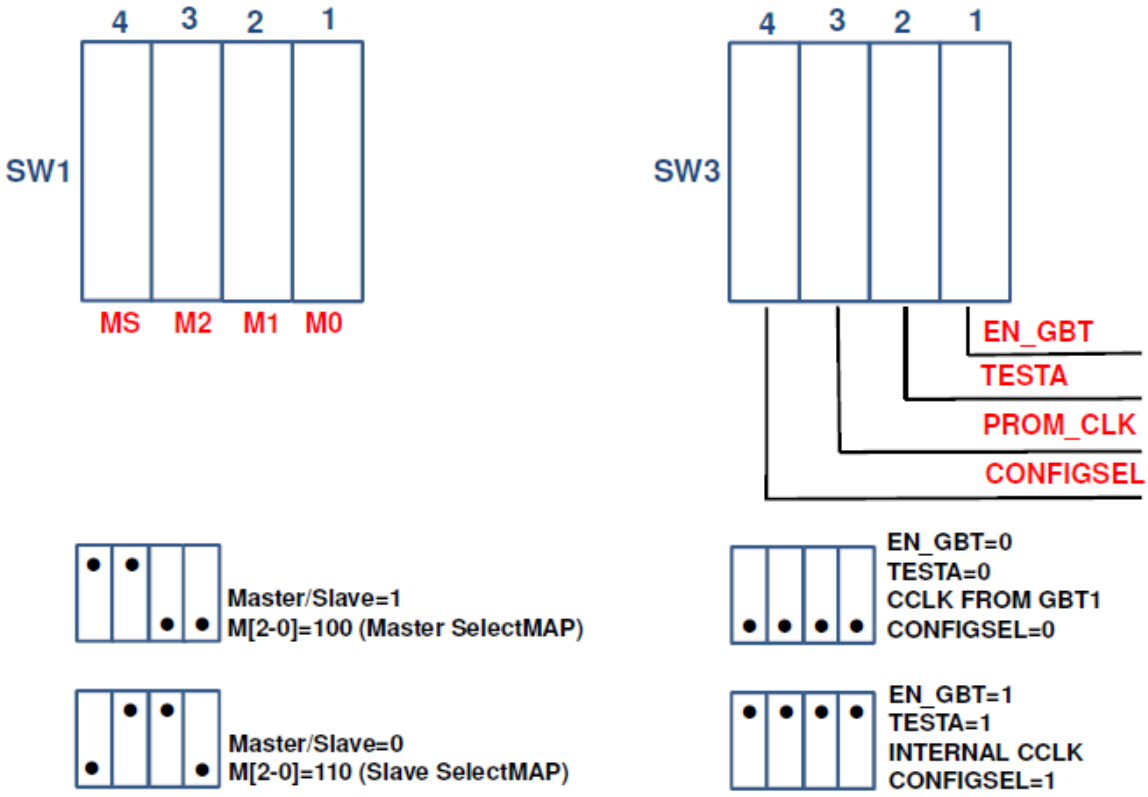


Figure 4: SW1 and SW3 switches on the top side of the OH board

The main goal of the FPGA is to construct up to five 13-bit trigger clusters and transmit them to the backend processor (via the two GBT transceivers) and to the CSC Trigger Motherboard (via the embedded MGT transmitters). A fully functional firmware for the FPGA has been designed and passed initial tests. This includes the "regular" version and a version with the Triple Modular Redundancy (TMR) to mitigate single event radiation effects. The FPGA resource usage for both versions is shown in Figure 5. In both cases the most critical parameter (LUT usage) is below 50%.

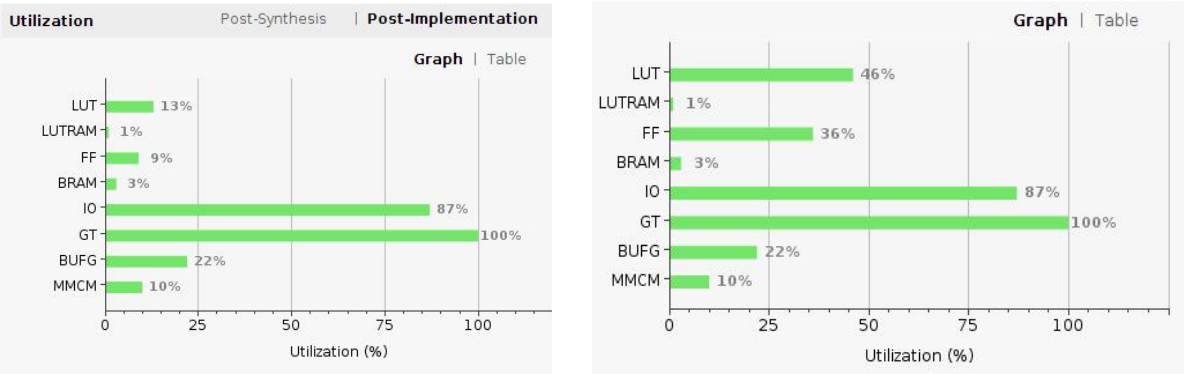


Figure 5: FPGA resource usage; "regular" design (left) and a design with the TMR (right)

2. Master/Slave Interface

This is the optional copper link between two adjacent OH boards (the transmitter is Slave and the receiver is Master). The main features are:

- Direct FPGA-to-FPGA connection without intermediate buffers;
- 6 differential data lines MSDxP/N where x=1..6, running at a data rate up to 320Mbps;
- Two spare simplex lines;
- FCI71922-126F 26-pin connector (P1) on the OH board;
- 3M HF100/26TP LSZH type flat twisted pair cable with 13 pairs;
- An identification input MASTER/SLAVE from the switch SW1-4 to the FPGA to select either Master ("1") or Slave ("0") mode (Fig.4).

3. FPGA Configuration from JTAG, EPROM and GBT ASIC

The FPGA can be configured from:

- GBT1 ASIC via the 8-bit parallel interface. This is the main operational mode;
- Optional EPROM via the 8-bit parallel interface;
- Xilinx JTAG cable;
- SCA ASIC [10] via the serial JTAG.

The configuration from the GBT1 is provided from the EPORT Data Outputs DOUT24…DOUT31 and the configuration clock comes from DCLK24 (EPORT Clock Output) to CCLK input of the FPGA. These 9 differential links are translated from the SLVS to CMOS levels (using SN65LVDT2 translators) and provided to the SN74CBTLV3861 buffer (U15). This buffer can be enabled with the EN_GBT signal coming from the switch SW3. For configuration from the GBT1 (Fig.6):

- Set EN_GBT="1" (SW3-1 off)
- Set CCLK from the GBT1 (SW3-3 on)
- Set Slave SelectMAP mode (SW1-1/2/3, M[2:0]=110)

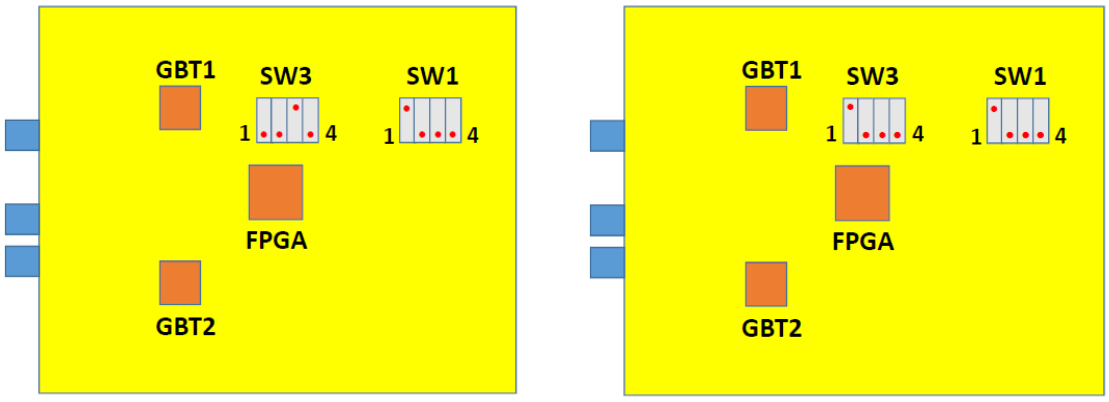


Figure 6: Switches for configuration from the GBT ASIC (left) and from the JTAG cable (right)

The TESTA switch (SW3-2) enables the SCA JTAG path when “1”. Xilinx cable should be detached. If TESTA=0, the SCA JTAG path is disabled and the Xilinx cable can be used for debugging and testing purposes.

The state of the INIT signal can be monitored on GPIO[7] line. The SCA ASIC can generate a Hard Reset pulse on GPIO[31] (active “1”). The state of the FPGA_DONE line can be monitored on GPIO[6]. The Hard Reset (/PROG=0) can also be produced from the push button SW2.

4. GBT Links

There are two GBT ASICs on the OH board (U2 and U3), each serving 6 VFAT3 ASICs. A link to each VFAT3 comprises three differential signal pairs:

- VFATxGBTOUTN/P, where x=1..12; these are the outputs from the GBT to VFAT3;

- VFATxGBTINN/P, where x=1..12; these are the inputs from the VFAT3 to GBT;

- VFATxGBTCLKN/P, where x=1..12, these are clock outputs from the GBT to VFAT3.

The first GBT1 also provides ELINKs to program the FPGA. It also supports the SCA interface and provides three differential global clocks to the FPGA (one dedicated MGT clocks and two general purpose global clocks FPGACLK1P/N and FPGACLK2P/N). Each GBT ASIC is connected to its own VTRX optical transceiver [11]. The VTRX receivers are non-inverted, but the transmitters are inverted.

The programming of each GBT is possible from an I2C dongle through a dedicated connector (8-pin FCI75867-132F).

CONFIGSEL input for both GBT devices has an external pull-down and also can be connected to 1.5V (SW3-4, Fig.4). CONFIGSEL=”0” to access the GBT from its optical link and “1” to access it from the dongle.

The GBT1 and GBT2 ASICs have 3 and 8 ELINK connections to the FPGA respectively.

5. SCA ASIC

The SCA ASIC provides the JTAG signals to the FPGA and optional EPROM.

The SCA can be controlled by the GBT1 ASIC (primary channel, default option) or by the GBT2 (AUX channel).

The SCA provides 12 Reset signals to the VFAT3 ASICs. These are dedicated outputs GPIO[8-19] with direct connections to the VFAT3 ASICs. The VFAT3 has an embedded pull-down resistor on these inputs. Active “1” for the reset.

The state of the DONE signal from the FPGA can be read to GPIO[6].

The state of the INIT signal from the FPGA can be read to GPIO[7].

GPIO[29] is connected to the test point T23.

GPIO[31]=”1” generates Hard Reset to the FPGA.

There is a 32-channel ADC in the SCA ASIC. Its inputs are assigned as below:

- IN0: 1.0 FPGA core voltage
- IN1: 1.0AVCC voltage (MGTAVCC)
- IN2: 1.2AVTT voltage (MGTAVTT)
- IN3: 1.8V
- IN4: 1.5V
- IN5: 2.5V
- IN6: VTRX1_RSSI
- IN7: VTRX2_RSSI
- IN8: MONITOR1 current monitor from FEAST1 (1.8V for the OH board)
- IN9: MONITOR2 current monitor from FEAST2 (1.5V for the OH board)
- IN10: MONITOR3 current monitor from FEAST3 (2.5V for the OH board)
- IN11: MONITOR4 current monitor from FEAST4 (analog 1.2V for all VFAT ASICs)
- IN12: MONITOR5 current monitor from FEAST5 (digital 1.2V for all VFAT ASICs)
- IN13: PT1000 Temperature sensor near U2 (GBT1), see Table 1
- IN14: PT1000 Temperature sensor near U3 (GBT2), see Table 1
- IN15: PT1000 Temperature sensor near U22 (VTRX), see Table 1
- IN16: PT1000 Temperature sensor near U8 (1.5V voltage regulator), see Table 1
- IN17: High precision 1kOhm resistor connected to GND

Table 1: PT1000 Temperature vs Resistance Chart

°C	°F	Ω	°C	°F	Ω
-10	14	961	55	131	1213
-5	23	980	60	140	1232
0	32	1000	65	149	1252
5	41	1019	70	158	1271
10	50	1039	75	167	1290
15	59	1058	80	176	1309
20	68	1078	85	185	1328
25	77	1097	90	194	1347
30	86	1117	95	203	1366
35	95	1136	100	212	1385
40	104	1155	105	221	1404
45	113	1175	110	230	1423
50	122	1194	115	239	1442
Resistance values of the Pt1000-sensors					

If, for example, channel 0 measurement is 249mV, the input FPGA core voltage is (taking into account an input resistor divider) 249mV x 4 = 996 mV, or well within the 5% tolerance. Expected values for channels 0..5 are 250mV, 250mV, 300mV, 450mV, 375mV, 625mV respectively.

Channels 6 and 7 (the Receiver Strength Signal Indicator, RSSI, for both VTRX transceivers) have 2kOhm/1kOhm resistor dividers.

MONITOR[5:1] are the outputs of five MAX4372T current sense amplifiers with voltage output. They allow to measure the currents of five FEAST [12] DC-DC converters located on the GEB boards. MAX4372T device provides 20V/V gain and with a current sensing resistor of 10mOhm on the GEB board the MONITOR[5:1] outputs are limited to 2V. These signals are provided to the SCA with a resistor divider 3kOhm/1kOhm since the SCA analog input range is between 0 and 1.0V. If the ADC output is, for example, 70mV, then the MONITOR is 70mV x 4 = 280mV (due to a resistor divider) and the current would be 280mV/10mOhm/20 = 1.4A.

For temperature measurements (channels 13-16) the 100uA current source should be enabled for each of these channels in the SCA ASIC. Then, if the output measurement is, for example, 110mV, the resistance would be R=V/I=110mV/100uA=1100 Ohm which corresponds to ~29C (Table 1).

Channel 17 is connected to a precise 1kOhm resistor. Channels 18-30 are not used. Channel 31 of the SCA ADC is connected to the internal temperature sensor. The conversion graph (Fig.7) is taken from the SCA Manual [10].

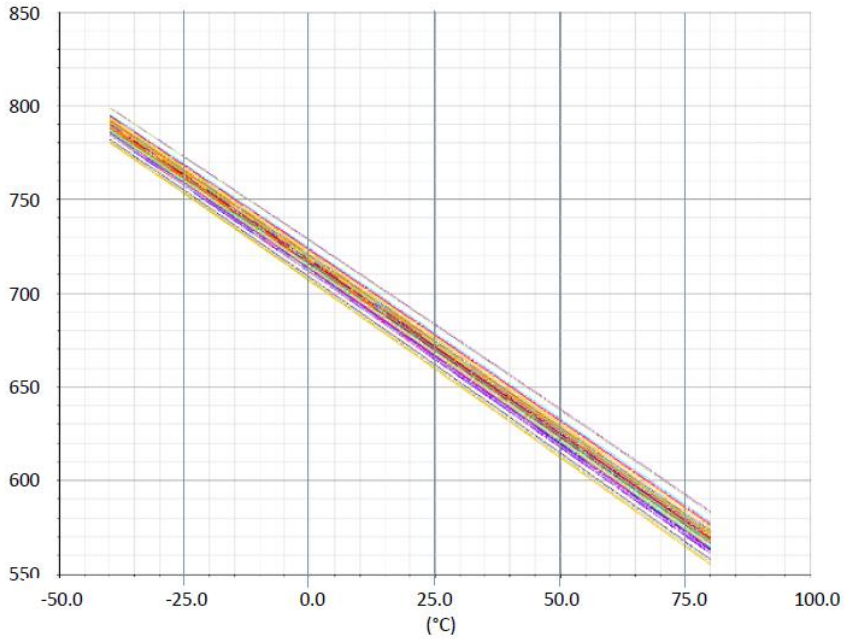


Figure 7: Conversion graph for the SCA internal temperature sensor

All SCA power pins (AVDD, DVDD, VDD) are connected to 1.5V.

6. Optical Links

There are two duplex optical links based on CERN designed radiation hard VTRX transceiver. They provide connection to the GBT ASICs for readout of the VFAT3 devices and transmission of the trigger data to the backend processor.

The other two identical optical links are based on 2-channel CERN designed VTTX transmitter [11]. Serial data is provided from four MGT transmitters in the Artix-7 FPGA (MGT[1:0] are the sources for the U28 VTTX and MGT[3:2] are the sources for the U27 VTTX). The MGT receivers are not used and permanently grounded. Only one VTTX device U26 will be used on all production boards.

All VTRX and VTTX parts are powered from 2.5V. All I2C connections are controlled by the SCA ASIC and respective pull-ups are powered from 1.5V. The VTTX receivers are not inverted.

7. Power Distribution and Consumption

Internal metal planes in the QSE/QTE connectors are used to deliver 1.5V, 1.8V and 2.5V powers from the GEB boards (Fig.3). These powers and GND are also provided from the Samtec HLE-108-02-F-DV-A connector (the GEB mating connector is HW-08-16-F-D-290-SM); pin assignment is shown in Fig.8.

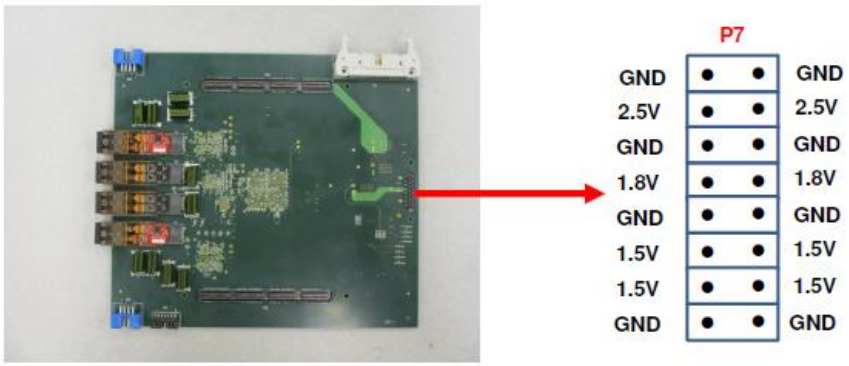


Figure 8: Pin assignment of the power connector P7 (as seen from the bottom of the OH PCB)

There are three MIC69502 voltage regulators on the OH board:

- 1.0V for the internal FPGA core,
- 1.0V for the MGT receivers
- 1.2V for the MGT transmitters.

The total power consumption is estimated to be below 11W per OH board:

- FPGA with the functional firmware: <1.8W (or <3W with the TMR firmware);
- 2 GBT ASIC: 2 x 1.5A x 1.5V = 4.5W (max);
- 1 VTTX transmitters: 1 x 0.3A x 2.5V = 0.75W (max);
- 2 VTRX transceivers: 2 x 0.2A x 2.5V = 1.0W (max);
- Other parts: < 1W.

8. LEDs and Test Points

There are the following green LEDs mounted on top of the OH board:

- FPGA_DONE output from the FPGA
- FPGA_INIT

- EN_GBT
- GBT1TXRDY
- GBT2TXRDY
- 2.5V
- 1.8V
- 1.5V
- 1.0VCCINT
- Two spare outputs from the FPGA

There are the following test points:

- 4 test points from the FPGA
- LDRESET, TESTCLOCKOUT and TESTOUTPUT from each of the GBT ASIC
- 1.0VAVCC, 1.2VAVTT, 1.0VCCINT, 1.5V, 1.8V, 2.5V, GND

9. Mechanical, PCB, Thermal, Radiation and Magnetic Requirements

The PCB dimensions and basic parameters are shown in Figs. 9-10.

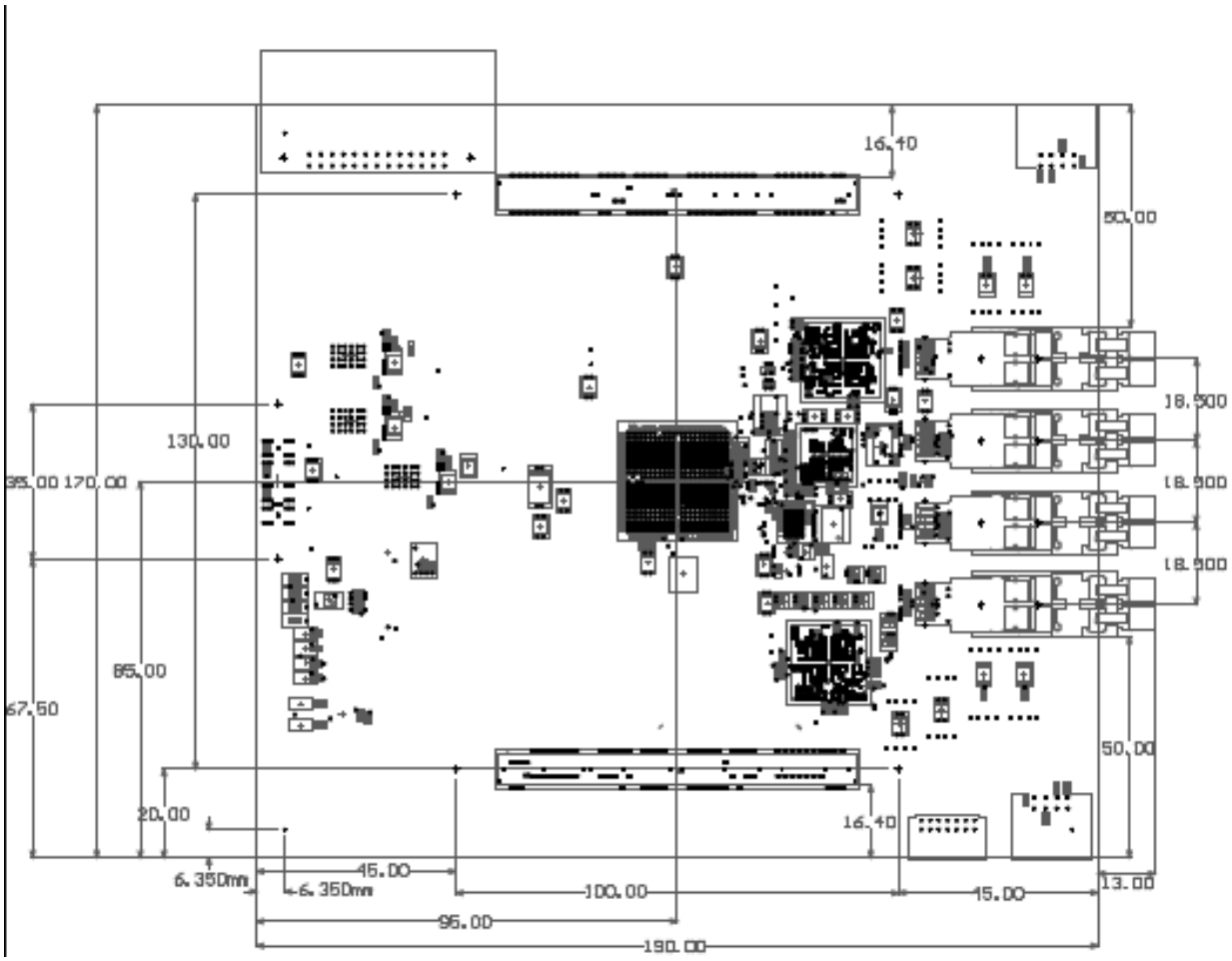
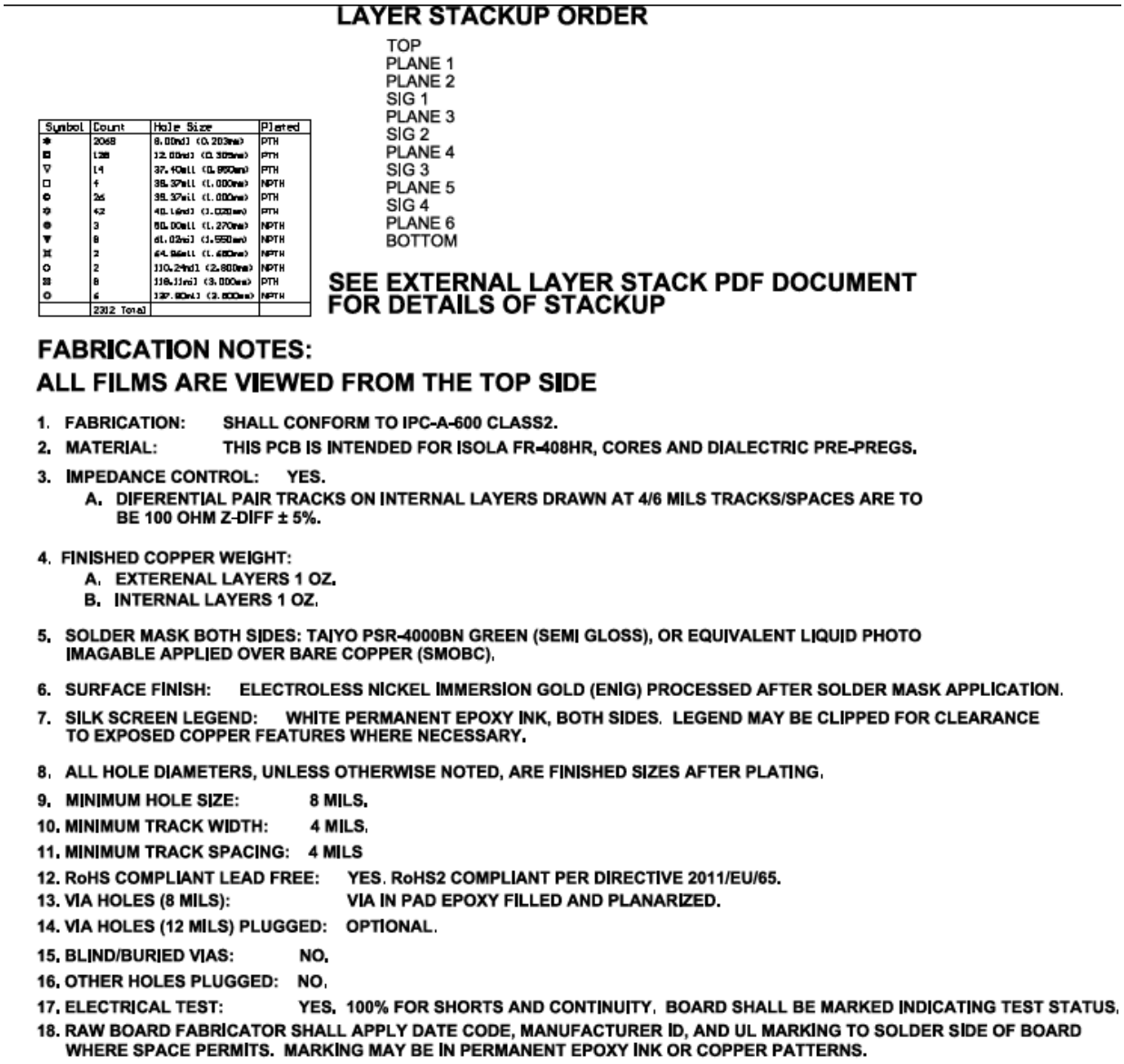


Figure 9: OH PCB Dimensions



LAYER STACKUP ORDER

TOP
PLANE 1
PLANE 2
SIG 1
PLANE 3
SIG 2
PLANE 4
SIG 3
PLANE 5
SIG 4
PLANE 6
BOTTOM

Symbol	Count	Hole Size	Plated
*	2068	8.00mil (0.203mm)	PTH
⊠	128	12.00mil (0.305mm)	PTH
▽	14	37.40mil (0.950mm)	PTH
□	4	38.37mil (1.000mm)	NPTH
⊙	26	38.37mil (1.000mm)	PTH
⊗	42	40.16mil (1.020mm)	PTH
◉	3	50.00mil (1.270mm)	NPTH
▼	8	61.02mil (1.550mm)	NPTH
⧓	2	64.96mil (1.650mm)	NPTH
○	2	110.24mil (2.800mm)	NPTH
⊠	8	118.11mil (3.000mm)	PTH
○	6	137.80mil (3.500mm)	NPTH
	2312 Total		

SEE EXTERNAL LAYER STACK PDF DOCUMENT FOR DETAILS OF STACKUP

FABRICATION NOTES:

ALL FILMS ARE VIEWED FROM THE TOP SIDE

1. FABRICATION: SHALL CONFORM TO IPC-A-600 CLASS2.
2. MATERIAL: THIS PCB IS INTENDED FOR ISOLA FR-408HR, CORES AND DIALECTRIC PRE-PREGS.
3. IMPEDANCE CONTROL: YES.
   A. DIFERENTIAL PAIR TRACKS ON INTERNAL LAYERS DRAWN AT 4/6 MILS TRACKS/SPACES ARE TO BE 100 OHM Z-DIFF ± 5%.
4. FINISHED COPPER WEIGHT:
   A. EXTERENAL LAYERS 1 OZ.
   B. INTERNAL LAYERS 1 OZ.
5. SOLDER MASK BOTH SIDES: TAIYO PSR-4000BN GREEN (SEMI GLOSS), OR EQUIVALENT LIQUID PHOTO IMAGABLE APPLIED OVER BARE COPPER (SMOBC).
6. SURFACE FINISH: ELECTROLESS NICKEL IMMERSION GOLD (ENIG) PROCESSED AFTER SOLDER MASK APPLICATION.
7. SILK SCREEN LEGEND: WHITE PERMANENT EPOXY INK, BOTH SIDES. LEGEND MAY BE CLIPPED FOR CLEARANCE TO EXPOSED COPPER FEATURES WHERE NECESSARY.
8. ALL HOLE DIAMETERS, UNLESS OTHERWISE NOTED, ARE FINISHED SIZES AFTER PLATING.
9. MINIMUM HOLE SIZE: 8 MILS.
10. MINIMUM TRACK WIDTH: 4 MILS.
11. MINIMUM TRACK SPACING: 4 MILS
12. RoHS COMPLIANT LEAD FREE: YES. RoHS2 COMPLIANT PER DIRECTIVE 2011/EU/65.
13. VIA HOLES (8 MILS): VIA IN PAD EPOXY FILLED AND PLANARIZED.
14. VIA HOLES (12 MILS) PLUGGED: OPTIONAL.
15. BLIND/BURIED VIAS: NO.
16. OTHER HOLES PLUGGED: NO.
17. ELECTRICAL TEST: YES. 100% FOR SHORTS AND CONTINUITY. BOARD SHALL BE MARKED INDICATING TEST STATUS.
18. RAW BOARD FABRICATOR SHALL APPLY DATE CODE, MANUFACTURER ID, AND UL MARKING TO SOLDER SIDE OF BOARD WHERE SPACE PERMITS. MARKING MAY BE IN PERMANENT EPOXY INK OR COPPER PATTERNS.

Figure 10: PCB parameters

As a part of the GE2/1 mechanical design, there will be a cooling infrastructure to provide heat dissipation from all critical components (FPGA, two GBT ASICs, voltage regulators, VTTX and VTRX optical parts).

All critical components of the OH board (GBT and SCA ASICs, VTTX and VTRX optical parts) are qualified to radiation levels a few orders higher than anticipated in the GE2/1 area. The other components have been tested before and found satisfactory [13].

Several inductors used in the design are the parts with air core. They can withstand the magnetic field at CMS safely.

References

[1] The Phase-2 Upgrade of the CMS Muon Detectors Technical Design Report. CERN-LHCC-2017-012 CMS-TDR-016 12 September 2017. Available at http://cds.cern.ch/record/2283189/files/CMS-TDR-016.pdf

[2] GE21 Optohybrid Board twiki. https://twiki.cern.ch/twiki/bin/viewauth/CMS/GE21OHBoardTwiki

[3] VFAT3 Manual
https://twiki.cern.ch/twiki/pub/CMS/GE21OHBoardTwiki/VFAT3_User_Manual_v2.3.pdf

[4] https://espace.cern.ch/GBT-Project/GBTX/default.aspx

[5] OH-GEB interface specification
https://twiki.cern.ch/twiki/pub/CMS/GE21GEBBoardTwiki/GE21_GEB_Interfaces_Specification_v2.pdf

[6] https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

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