GE2/1 Optohybrid Board

Draft Specification 1.1

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Introduction

The GE2/1 Optohybrid (OH) board provides readout and trigger interfaces for 12 VFAT3 ASICs residing on the GEB board. A comprehensive description of the GE2/1 GEM design and electronics can be found in the Technical Design Report [1]. A block diagram of the OH board is shown on Fig.1.

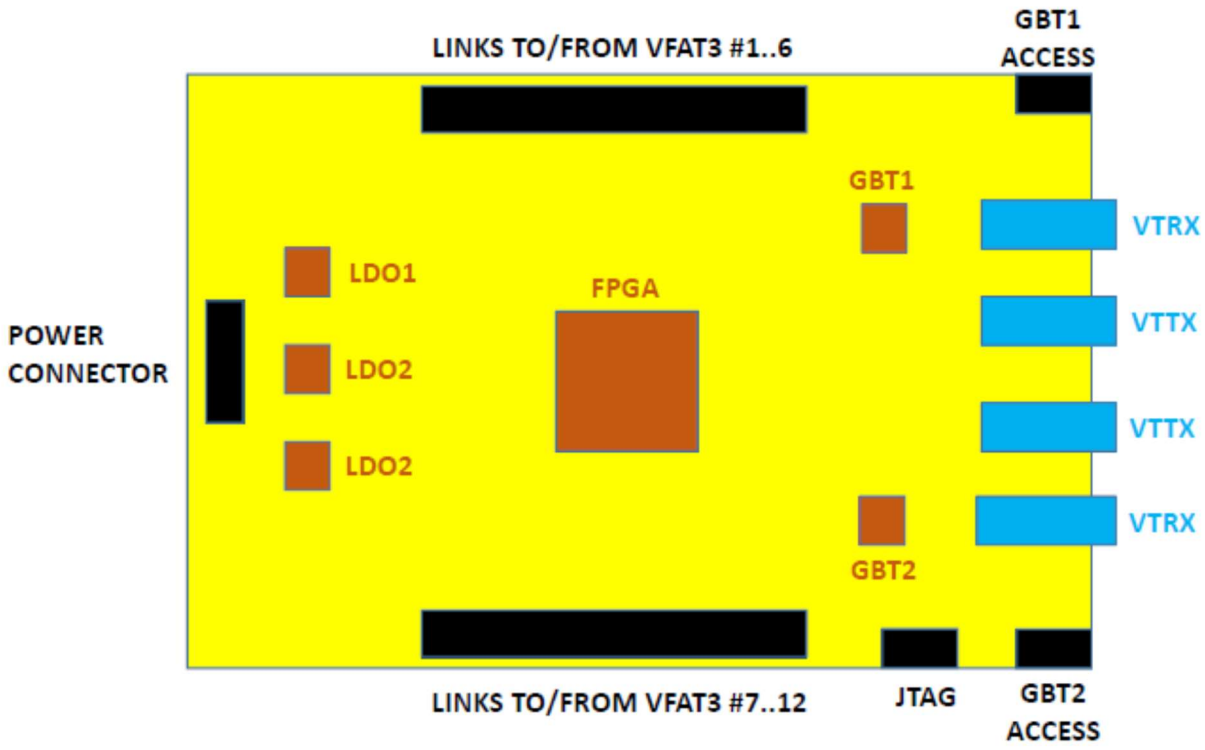

Fig.1. Block diagram of the OH board

1. FPGA

Xilinx Artix-7 XC7A75T-2FGG484C [2] (U1) has been selected due to:

- Sufficient number of IO pins (285 total) and logic resources
- Low power consumption
- Flexible IODELAY block
- Availability and low cost
- Sufficient radiation tolerance [3]-[5]

The main functions and interfaces are:

- Two Samtec QSE-080-01-L-D-A connectors are used for all links to 12 VFAT3 ASICs. Two mating Samtec QTE-080-03-L-D-A are used on GEB boards.
- FPGA receives 9 differential signals from each VFAT3, including 8 data bits (VFATxDyN/P, where x=1..12 and y=1..8) and one Strobe signal VFATxSTRN/P)
- Banks 13,14,15,16,34,35 are used for VFAT3 connections, all VCCIO powers are 2.5V
- Bank 0 is also powered by 2.5V. A dedicated configuration banks voltage select CFGBVS="1".
- Two global clocks (FPGACLK1P/N (W19/W20, bank 14) and FPGACLK2P/N (J19/H19, bank 15) are provided from the GBTX1 ASIC
- FPGA receives 3 status signals (GBTxRXDV, GBTxRXRDY, GBTxTXRDY, x=1,2) from each GBT ASIC, and transmits GBTxTXDV to each GBT ASIC. SN74AVC2T45 level translators are used for level conversion (2.5V to/from 1.5V).
- 2 ELINK connections (ELINK1P/N and ELINK2P/N) from/to GBT1 and 2 ELINK connections (ELINK3P/N and ELINK4P/N) from/to GBT2. One ELINKCLK1P/N from GBT1.
- VTRX1_MABS and VTRX2_MABS status inputs from both optical transceivers
- Master/Slave interface (described below in Section 2) to a neighbor OH
- Xilinx XCF32PFSG48C (BGA48) EPROM
- FPGA (1st device) + EPROM (2nd device) in the JTAG chain, JTAG connector P4 (Molex 87833-1420) is compatible with Xilinx JTAG cable.
- Configuration pins M0..M2 with embedded pull-ups can be grounded with a switch SW1-1..3to select the configuration mode (Slave SelectMAP default for configuration from the GBT1 ASIC; Master SelectMAP for configuration from EPROM).
- There are 4 MGT links in this FPGA. Two global clocks MGTREFCLK0P/N and MGTREFCLK1P/N are coming from the GBT1 ASIC (CLOCKDES0 and CLOCKDES1 with programmable frequency and phase). Two MGT outputs are connected to VTTX1 optical transmitter (trigger outputs to OTMB) and the other two outputs are connected to VTTX2 optical transmitters (trigger outputs to uTCA processor). MGT receivers are not used and are all grounded.
- PUDC_B inputs could be either "1" or "0" with external resistors R67/R69 to enable or disable internal pull-ups on SelectIO pins
- EMCCLK external master configuration clock is not used
- Internal ADC is not used
- The battery backup supply is not used

2. Master/Slave Interface

This is a simplex link between two OH boards (Transmitter/Slave and Receiver/Master) to reduce the number of trigger optical links from the GE21 chamber. The main features are:

- Direct FPGA-to-FPGA connection without intermediate buffers
- 12 differential data lines MSDxP/N where x=1..12, running at 320Mbps

- Two spare simplex lines
- FCI71922-126F 26-pin connector (P1) on the OH board
- 3M HF100/26TP LSZH type flat twisted pair cable with 13 pairs
- An identification input MASTERSLAVE from the switch SW1-4 to the FPGA to select either Master (“1”) or Slave (“0”) mode

3. EPROM and Configuration from GBT ASIC

The FPGA can be configured either from the XCF32P EPROM or from the GBT1 ASIC; in both cased via the 8-bit parallel interface.

The configuration from GBT1 is provided from EPORT Data Outputs DOUT24…DOUT31 and the configuration clock comes from DCLK24 (EPORT Clock Output) to CCLK input of the FPGA. These 9 differential links are translated from SLVS to CMOS levels (using SN65LVDT2 translators) and provided to the SN74CBTLV3861 buffer (U15). This buffer can be enabled with the EN_GBT signal coming from the switch SW3. For initial debugging the EPROM would be chosen (EN_GBT=”0”). For configuration from GBT1 the EN_GBT=”1”. In this case the GPIO29 output of SCA ASIC SCA_ENGBTLOAD disables EPROM (active “0”) . The state of the INIT signal can be monitored on GPIO7 line. The SCA ASIC can also enable propagation of Hard Reset signal from GBT1 (GBTIO30=”1”) and generate this Hard Reset on GPIO31 (active “1”). The state of FPGA_DONE line can be monitored on GPIO6. Hard Reset can also be produced from a push button SW2.

4. GBTx Links

There are two GBTx ASICs on the OH board (U2 and U3). The first one, GBT1, serves VFAT3 ASICs 1..6 and the second one, GBT2, serves ASICs 7..12. A link to each VFAT3 comprises three differential signal pairs:

- VFATxGBTOUTN/P, where x=1..12; these are the outputs from the GBTx (GIO outputs) to VFAT3

- VFATxGBTINN/P, where x=1..12; these are the inputs from VFAT3 to GBTx (GIN inputs)

- VFATxGBTCLKN/P, where x=1..12, these are clock outputs from GBTx to VFAT3 (DCLK outputs)

The first GBT1 also provides ELINKs to download the FPGA. It also supports the SCA interface and provides four global clocks to the FPGA (two dedicated MGT clocks and two general purpose global clocks). Each GBTx ASIC is connected to its own VTRX optical transceiver.

CONFIGSEL input for both GBTx devices has an external pull-down and also can be connected to +1.5V.

The programming of each GBTx is possible from a dedicated connector (8-pin FCI75867-132F with CERN used pin assignment).

Each GBTx also provides two general purpose ELINKs to the FPGA.

5. SCA ASIC

The SCA ASIC (U4) provides JTAG signals to the FPGA and EPROM. External 1.5V-to/from-2.5V level converters are used.

The SCA is controlled by GBT1 ASIC.

The SCA provides 12 Reset signals to VFAT3 ASICs. These are dedicated outputs GPIO8..GPIO19 with direct connections to VFAT3. VFAT3 has an embedded pull-down resistor on these inputs. Active “1” for reset.

The state of INIT can be read to GPIO7.

GPIO29=”0” disables the EPROM and allows to configure the FPGA from GBT1 when EN_GBT=”1”.

GPIO30=”1” enables propagation of Hard_Reset from GPIO31 to the FPGA when EN_GBT=”1”.

GPIO31=”1” generates Hard Reset when EN_GBT=”1”.

ADC inputs are assigned as below:

- IN0: +1.0 FPGA core voltage
- IN1: +1.0AVCC voltage (MGTAVCC)
- IN2: +1.2AVTT voltage (MGTAVTT)
- IN3: +1.8V
- IN4: +1.5V
- IN5: +2.5V
- IN6: VTRX1_RSSI
- IN7: VTRX2_RSSI
- IN8: MONITOR1 current monitor from FEAST1
- IN9: MONITOR2 current monitor from FEAST2
- IN10: MONITOR3 current monitor from FEAST3
- IN11: MONITOR4 current monitor from FEAST4
- IN12: MONITOR5 current monitor from FEAST5

All SCA powers (AVDD, DVDD, VDD) are 1.5V.

6. Optical Links

There are two duplex optical links based on CERN designed radiation hard VTRX transceiver. They provide connection to the GBTx ASICs for readout of VFAT3 devices to the backend uTCA processor.

The other two optical links are based on a 2-channel CERN designed VTTX transmitter. Two channels are needed to provide trigger bits to the OTMB board for local triggering (3.2Gbps transmission with 8B/10B decoding) and the other two channels provide the same data to the Endcap Muon Track Finder at 3.2Gbps or higher rate. These four channels are required only for the Master OH.

All VTRX and VTTX parts are powered from 2.5V. All I2C connections are controlled by the SCA ASIC and respective pull-ups are powered from 1.5V.

7. Power Distribution

Internal metal planes in the QSE connectors are used to deliver +1.5V, +1.8V and +2.5V powers from GEB boards. These powers and GND can also be provided from a Samtec HLE-108-02-F-DV-A connector (this option should be very convenient for testing and debugging). The GEB board may also provide powers through mating HW-08-16-F-D-290-SM connector (11.05 mm total mating height).

+1.5V is needed for the SCA, GBT ASICs and level conversion parts.

+2.5V is used by the FPGA, VTRX, VTTX, SN65LVDT2, and some other digital logic parts.

There are three MIC69502 voltage regulators on the OH board:
- +1.0V for the internal FPGA core,
- +1.0V for MGT receivers
- +1.2V for MGT transmitters.

The input for all three regulators is +1.8V. +1.8V is also used by EPROM.

Based on Xilinx Power Analyzer, the expected power consumption of the FPGA is <1.8W.

8. LEDs and Test Points

There are the following green LEDs mounted on top of the OH board:

- FPGA_DONE output from the FPGA
- FPGA_INIT
- EN_GBT
- GBT1TXRDY
- GBT2TXRDY
- +2.5V
- +1.8V
- Two spare outputs from the FPGA

There are the following test points:

- 4 test points from the FPGA
- LDRESET, TESTCLOCKOUT and TESTOUTPUT from each GBTx ASIC
- +1.0VAVCC, +1.2VAVTT, +1.0VCCINT, +1.5V, +1.8V, +2.5V, GND

References

[1] CMS TECHNICAL DESIGN REPORT FOR THE MUON ENDCAP GEM UPGRADE CERN-LHCC-2015-012 CMS-TDR-013 30 September 2015. Available at https://cds.cern.ch/record/2021453/files/CMS-TDR-013.pdf

[2] https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

[3] https://www.xilinx.com/support/documentation/user_guides/ug116.pdf

[4] https://indico.cern.ch/event/489996/contributions/2291857/attachments/1345403/2028662/TWEPP_Artix7.pdf

[5] http://cds.cern.ch/record/2119894/files/ATL-MUON-SLIDE-2016-010.pdf