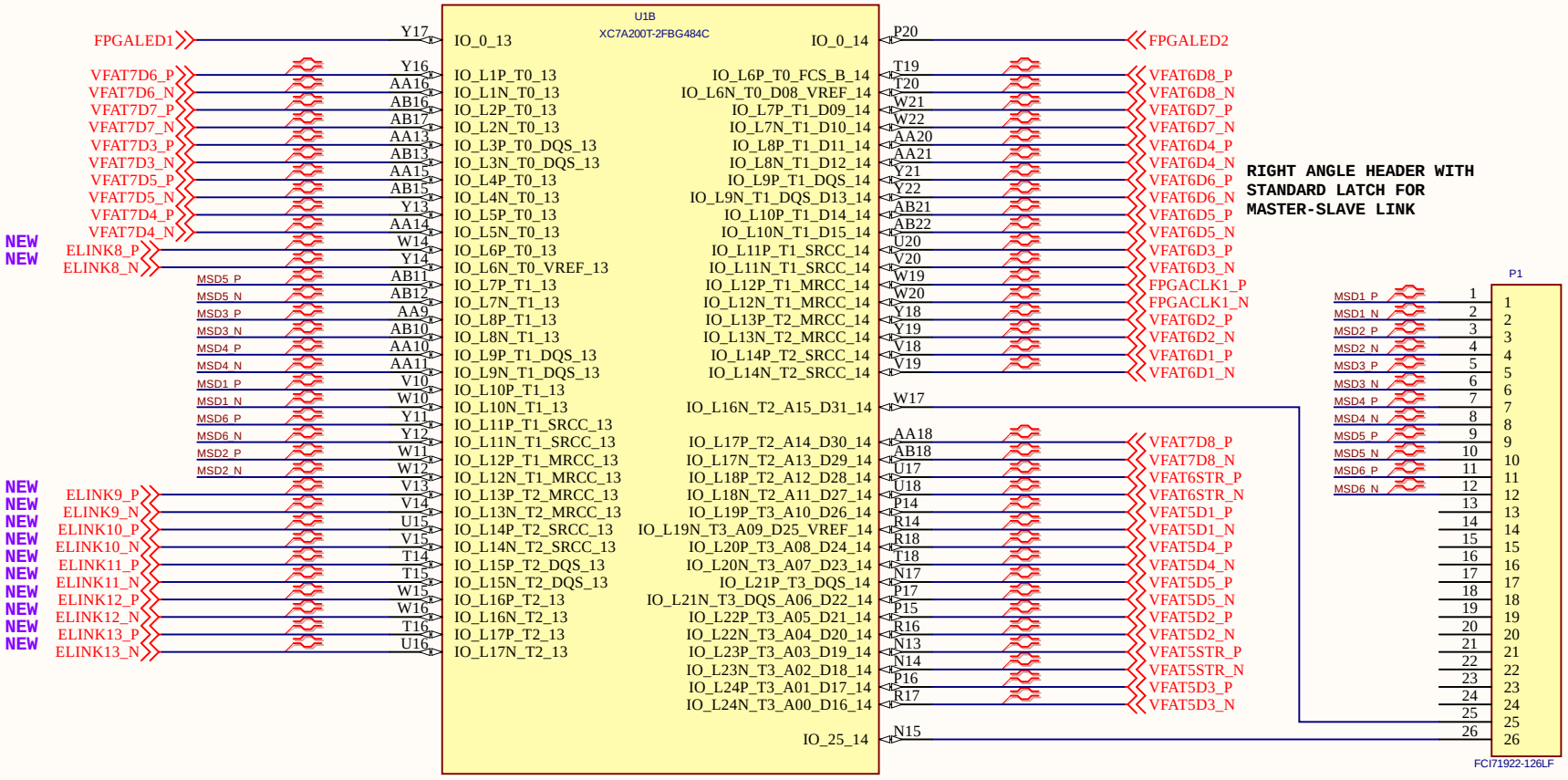
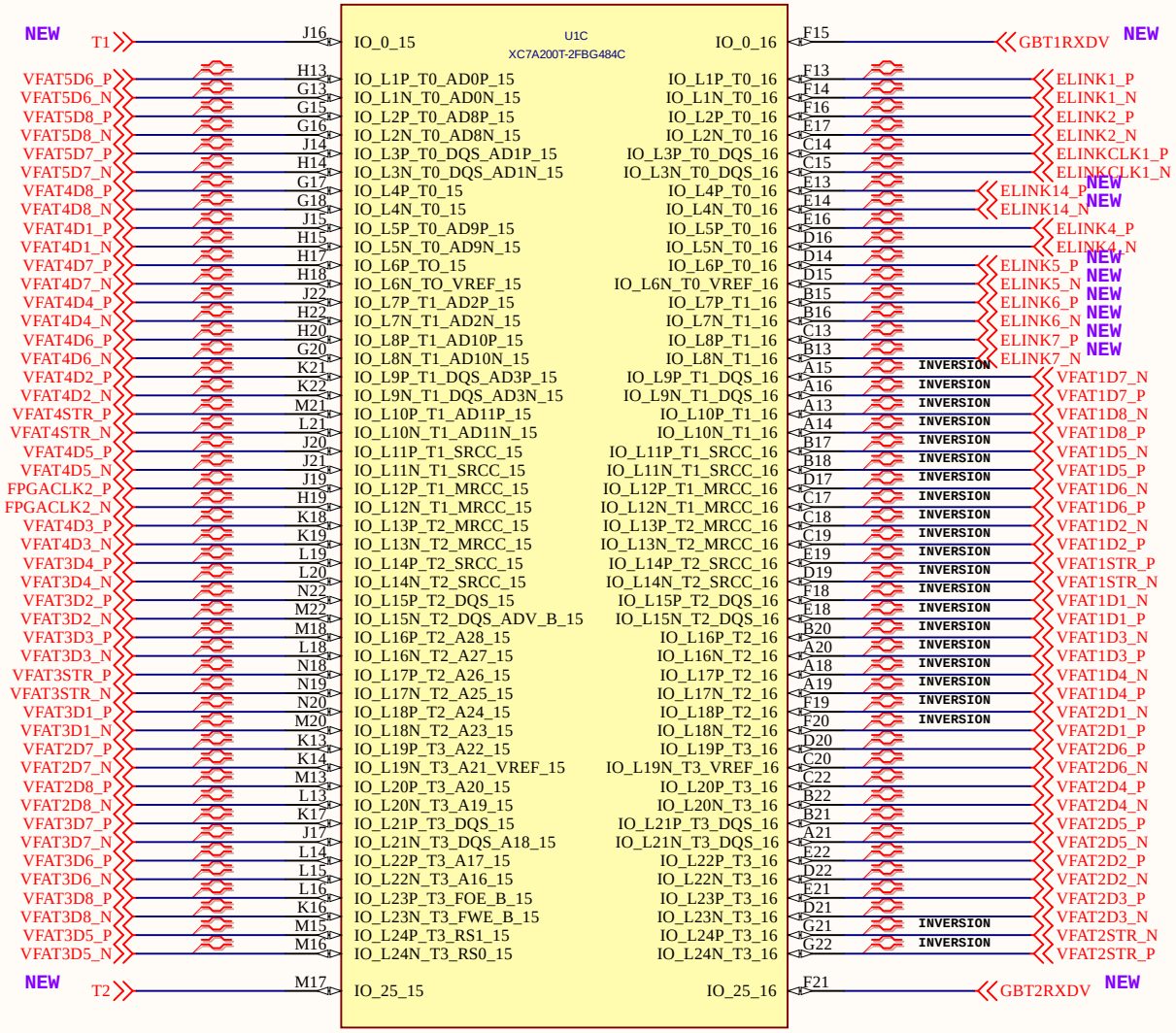
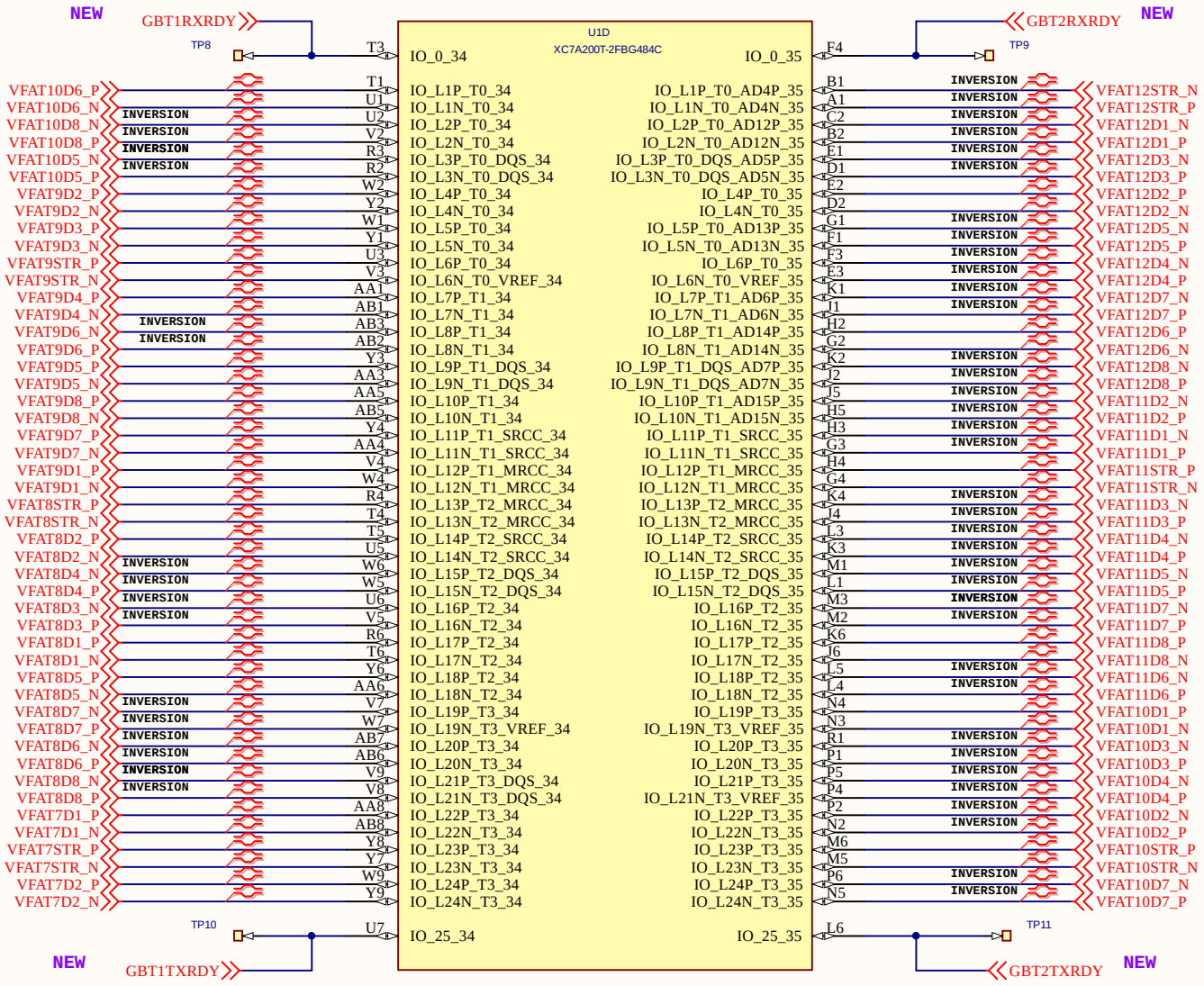



| | |
|---|---|
| Title | FPGA IO BANKS 13 & 14 |
| Size | A |
| Document Number | |
| Rev | 3.0 |
| Date: | 04-03-2020 |
| Sheet | 1 of 12 |

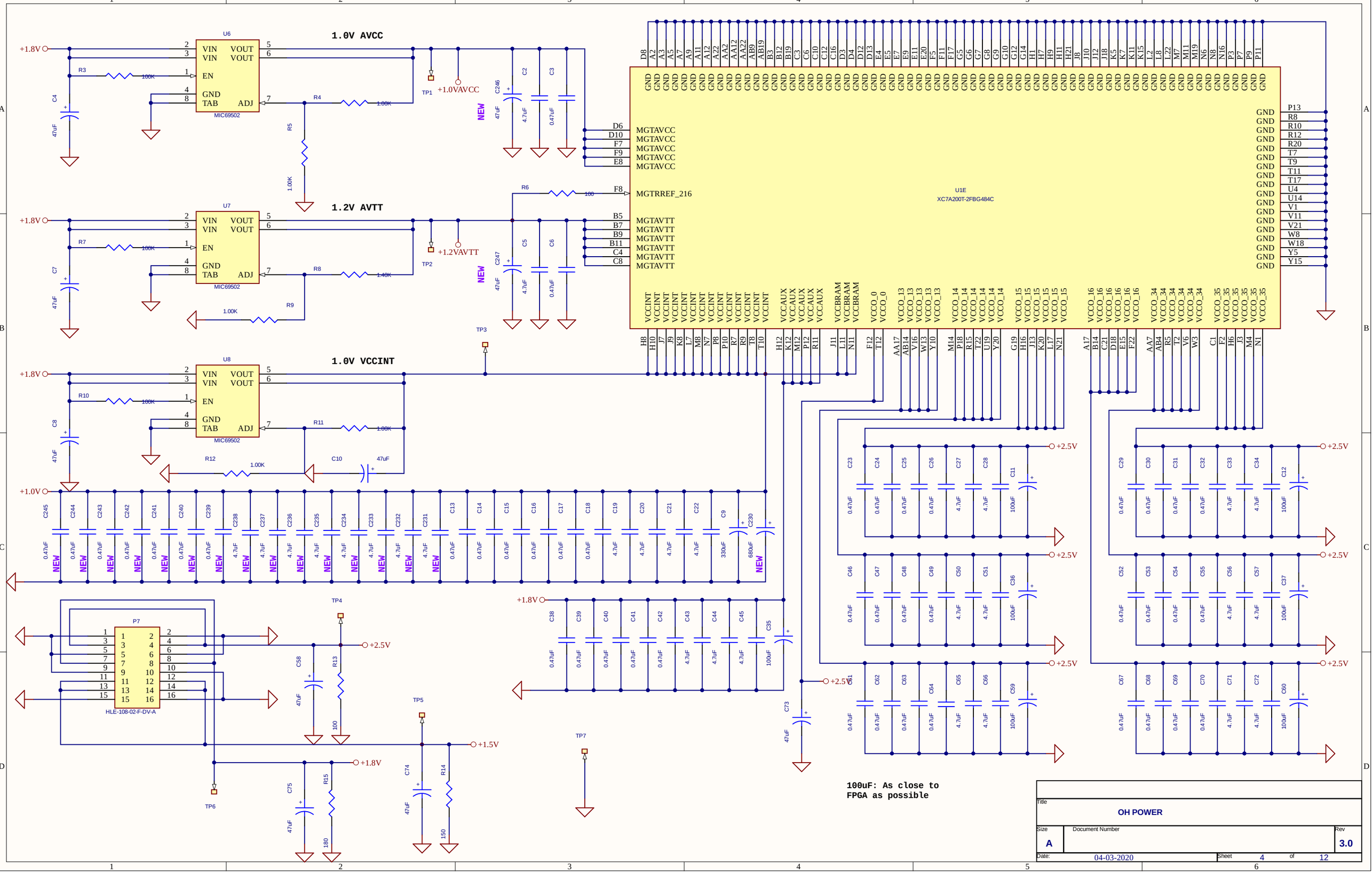



| | |
|---|---|
| Title | FPGA IO BANKS 15 & 16 |
| Size | A |
| Document Number | |
| Rev | 3.0 |
| Date: | 04-03-2020 |
| Sheet | 2 of 12 |

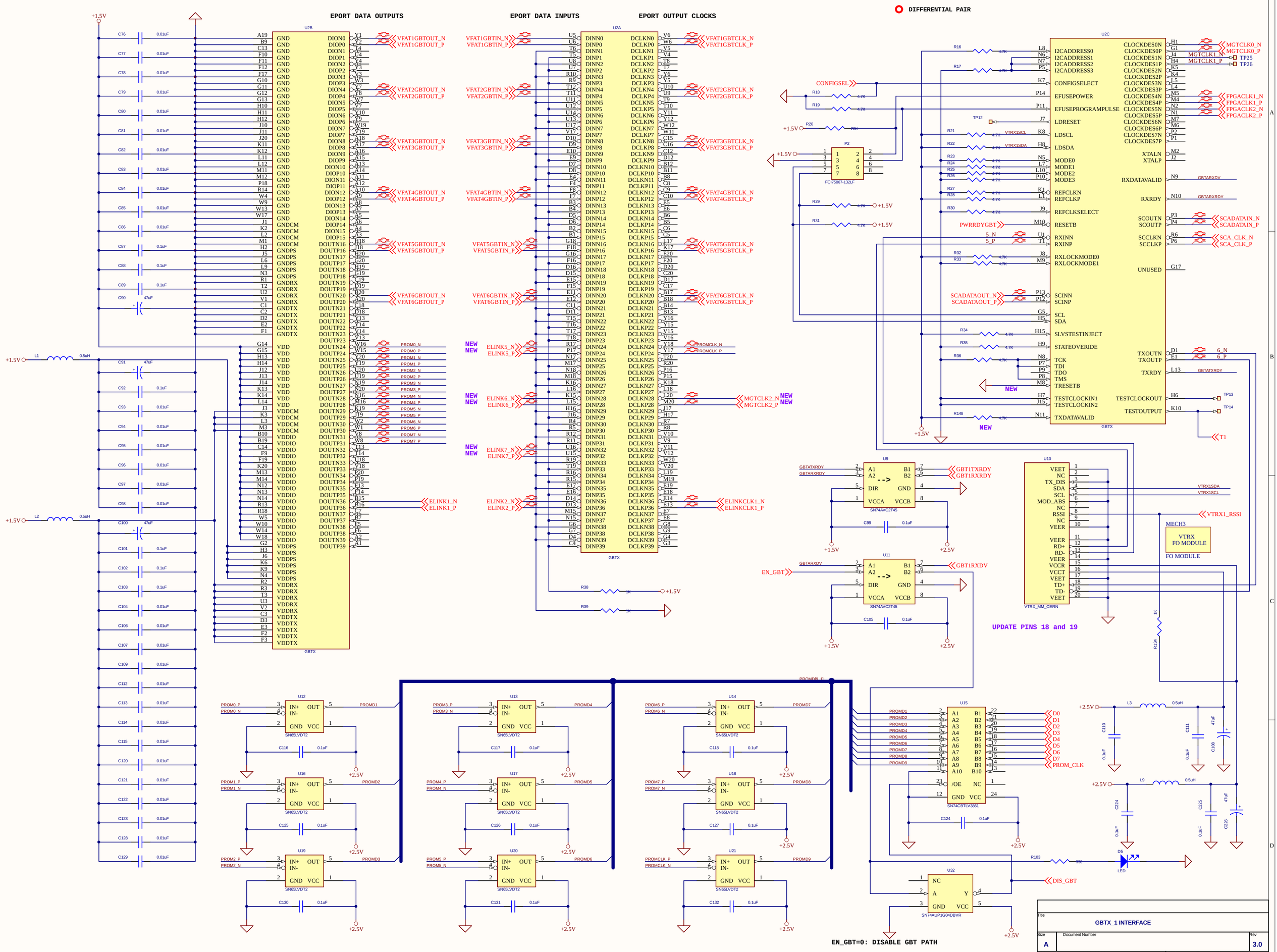


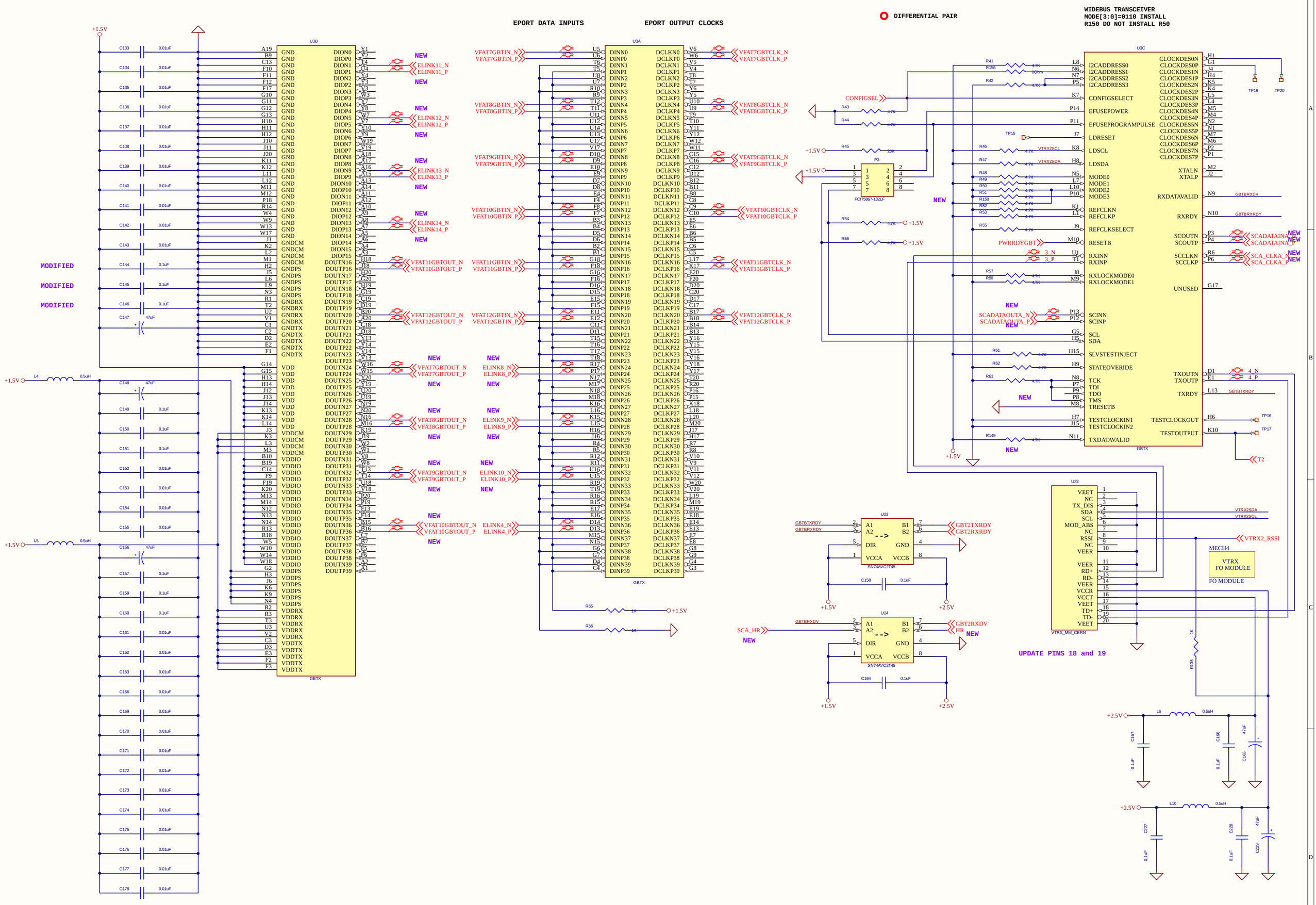

DIFFERENTIAL PAIR

| | |
|---|---|
| Title | FPGA IO BANKS 34 & 35 |
| Size | A |
| Document Number | |
| Rev | 3.0 |
| Date: | 04-03-2020 |
| Sheet | 3 of 12 |

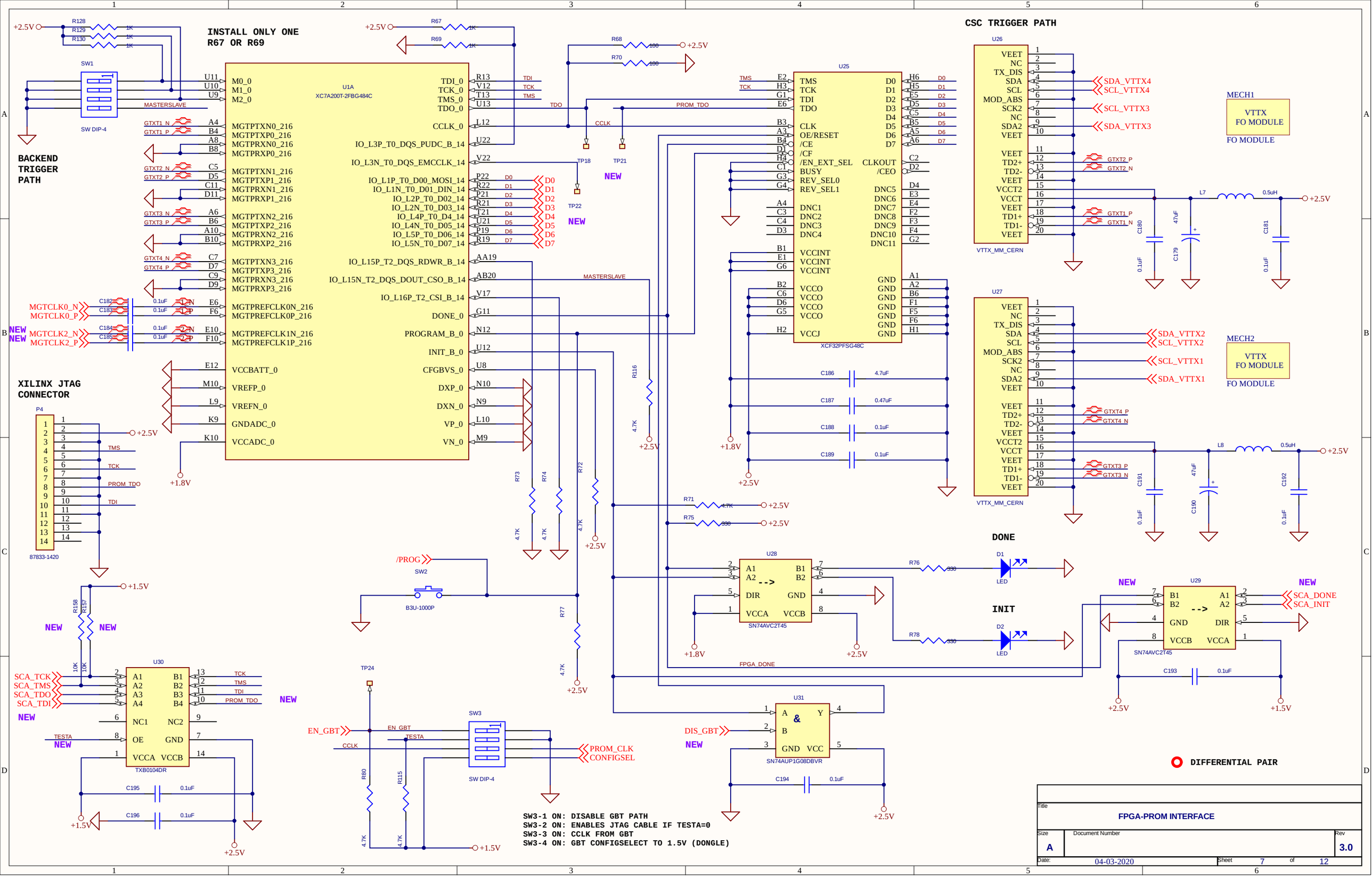


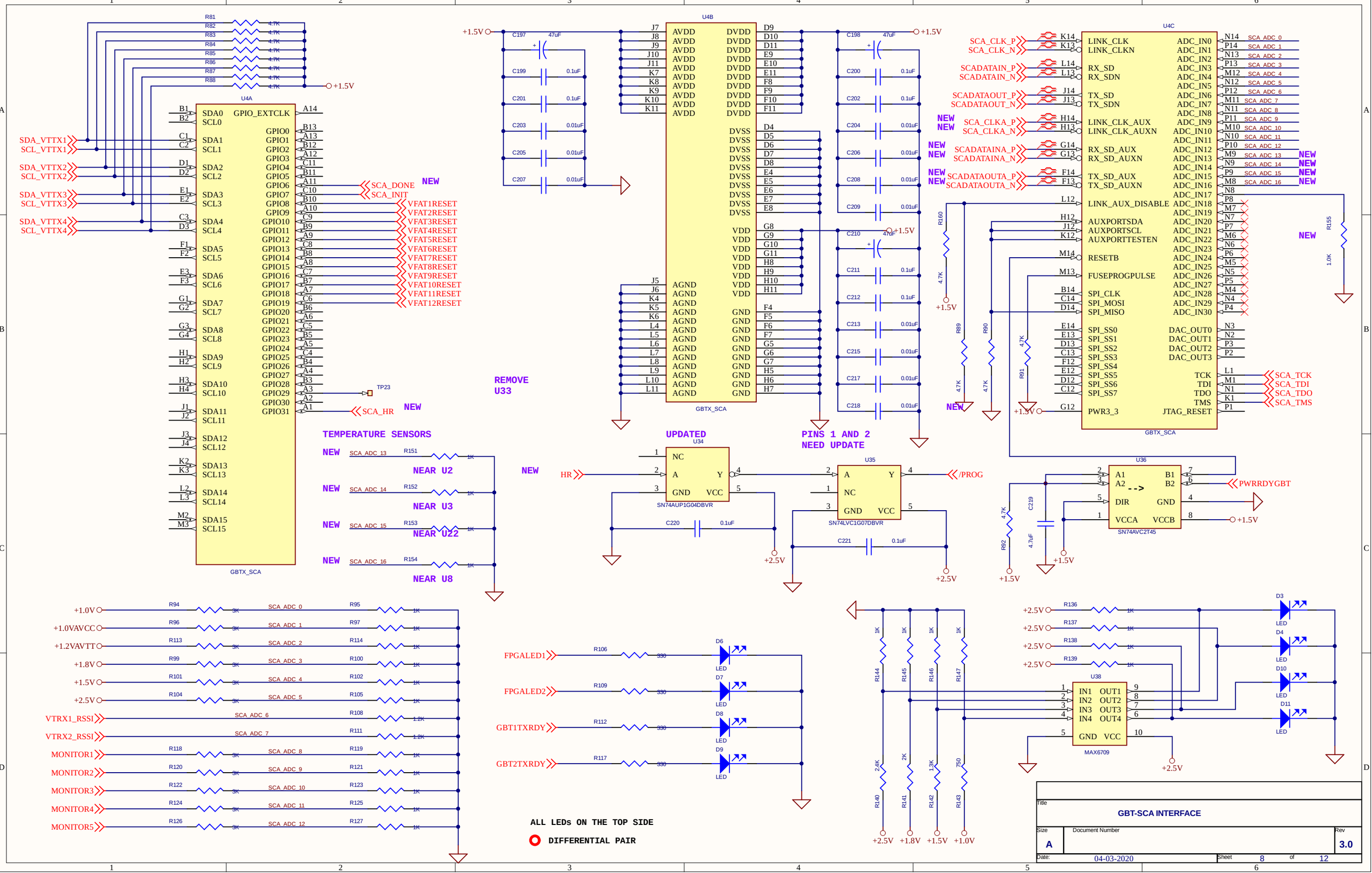

| | |
|---|---|
| Title | OH POWER |
| Size | A |
| Document Number | |
| Rev | 3.0 |
| Date: | 04-03-2020 |
| Sheet | 4 of 12 |


EPORT DATA OUTPUTS
EPORT DATA INPUTS
EPORT OUTPUT CLOCKS
DIFFERENTIAL PAIR
U2B
GBTX
U2A
GBTX
U2C
GBTX
U9
SN74AVC2T245
U10
VTRX_MM_CERN
U11
SN74AVC2T245
MECH3
VTRX
FO MODULE
FO MODULE
UPDATE PINS 18 and 19
U12
U13
U14
U15
SN74CBTLV3861
U16
U17
U18
U19
U20
U21
SN65LVDT2
U32
SN74AUP1G04DBVR
EN_GBT=0: DISABLE GBT PATH
Title
GBTX_1 INTERFACE
Size
A
Document Number
Rev
3.0
Date:
04-03-2020
Sheet
5
of
12




| | |
|---|---|
| Title | GBTX_2 INTERFACE |
| Size | A |
| Document Number | |
| Rev | 3.0 |
| Date: | 04-03-2020 |
| Sheet | 6 of 12 |


INSTALL ONLY ONE
R67 OR R69
CSC TRIGGER PATH
BACKEND
TRIGGER
PATH
XILINX JTAG
CONNECTOR
U1A
XC7A200T-2FBG484C
U25
XCF32PFSG48C
U26
VTTX_MM_CERN
U27
VTTX_MM_CERN
MECH1
VTTX
FO MODULE
FO MODULE
MECH2
VTTX
FO MODULE
FO MODULE
SW1
SW DIP-4
P4
87833-1420
U30
TXB0104DR
U28
SN74AVC2T45
U29
SN74AVC2T45
U31
SN74AUP1G08DBVR
SW2
B3U-1000P
SW3
SW DIP-4
DONE
INIT
NEW
DIFFERENTIAL PAIR
SW3-1 ON: DISABLE GBT PATH
SW3-2 ON: ENABLES JTAG CABLE IF TESTA=0
SW3-3 ON: CCLK FROM GBT
SW3-4 ON: GBT CONFIGSELECT TO 1.5V (DONGLE)
Title
FPGA-PROM INTERFACE
Size
A
Document Number
Rev
3.0
Date:
04-03-2020
Sheet
7
of
12


U4A
GBTX_SCA
U4B
GBTX_SCA
U4C
GBTX_SCA
U34
SN74AUP1G04DBVR
U35
SN74LVC1G07DBVR
U36
SN74AVC2T45
U38
MAX6709
SDA_VTTX1
SCL_VTTX1
SDA_VTTX2
SCL_VTTX2
SDA_VTTX3
SCL_VTTX3
SDA_VTTX4
SCL_VTTX4
SCA_DONE
SCA_INIT
VFAT1RESET
VFAT2RESET
VFAT3RESET
VFAT4RESET
VFAT5RESET
VFAT6RESET
VFAT7RESET
VFAT8RESET
VFAT9RESET
VFAT10RESET
VFAT11RESET
VFAT12RESET
SCA_HR
TP23
NEW
REMOVE
U33
UPDATED
PINS 1 AND 2
NEED UPDATE
TEMPERATURE SENSORS
NEAR U2
NEAR U3
NEAR U22
NEAR U8
SCA_ADC_13
SCA_ADC_14
SCA_ADC_15
SCA_ADC_16
SCA_CLK_P
SCA_CLK_N
SCADATAIN_P
SCADATAIN_N
SCADATAOUT_P
SCADATAOUT_N
SCA_CLKA_P
SCA_CLKA_N
SCADATAINA_P
SCADATAINA_N
SCADATAOUTA_P
SCADATAOUTA_N
LINK_CLK
LINK_CLKN
RX_SD
RX_SDN
TX_SD
TX_SDN
LINK_CLK_AUX
LINK_CLK_AUXN
RX_SD_AUX
RX_SD_AUXN
TX_SD_AUX
TX_SD_AUXN
LINK_AUX_DISABLE
AUXPORTSDA
AUXPORTSCL
AUXPORTTESTEN
RESETB
FUSEPROGPULSE
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS0
SPI_SS1
SPI_SS2
SPI_SS3
SPI_SS4
SPI_SS5
SPI_SS6
SPI_SS7
PWR3_3
TCK
TDI
TDO
TMS
JTAG_RESET
SCA_TCK
SCA_TDI
SCA_TDO
SCA_TMS
PWRRDYGBT
/PROG
HR
+1.0V
+1.0VAVCC
+1.2VAVTT
+1.8V
+1.5V
+2.5V
VTRX1_RSSI
VTRX2_RSSI
MONITOR1
MONITOR2
MONITOR3
MONITOR4
MONITOR5
FPGALED1
FPGALED2
GBT1TXRDY
GBT2TXRDY
ALL LEDs ON THE TOP SIDE
DIFFERENTIAL PAIR
Title
GBT-SCA INTERFACE
Size
A
Document Number
Rev
3.0
Date:
04-03-2020
Sheet
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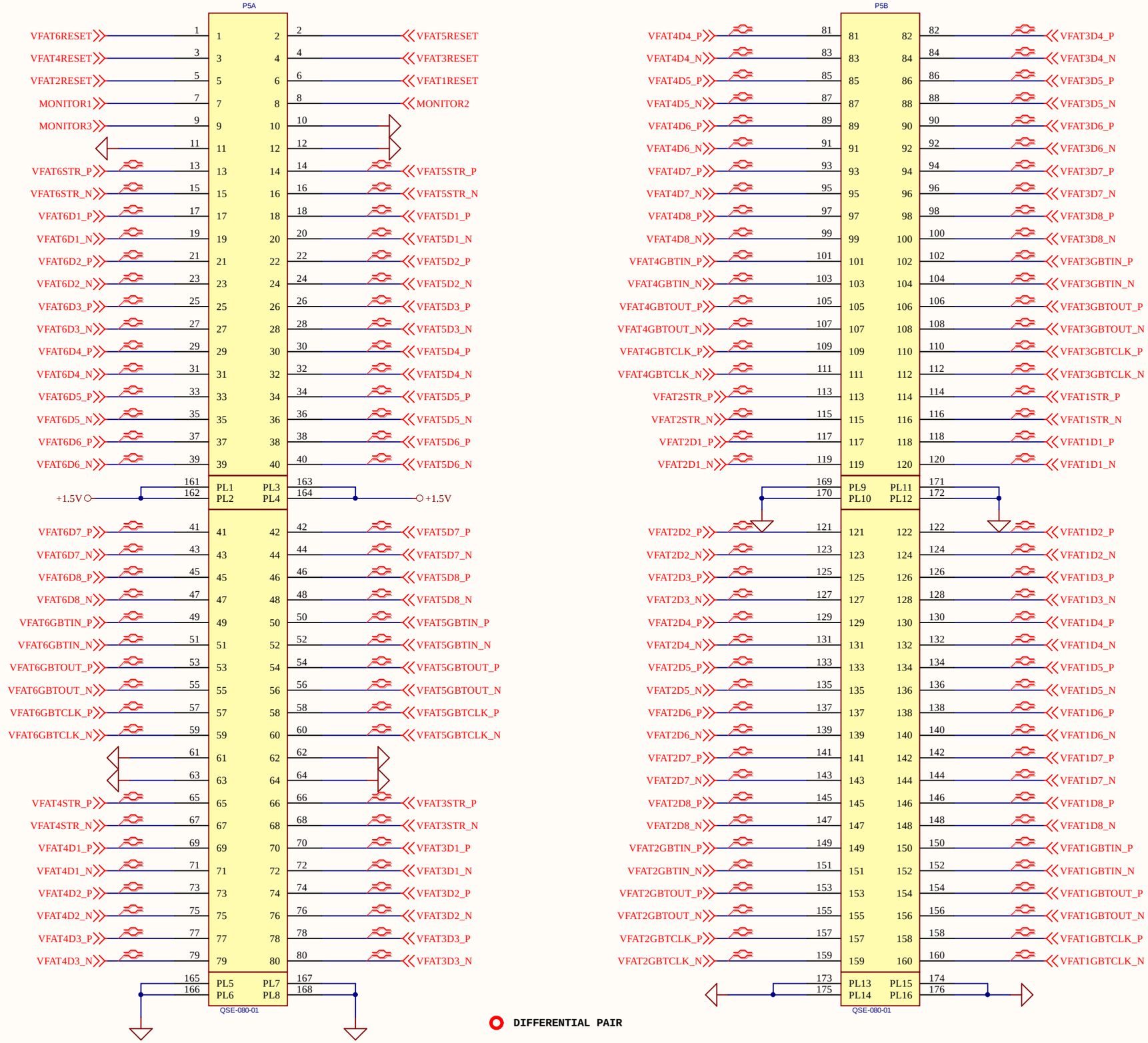
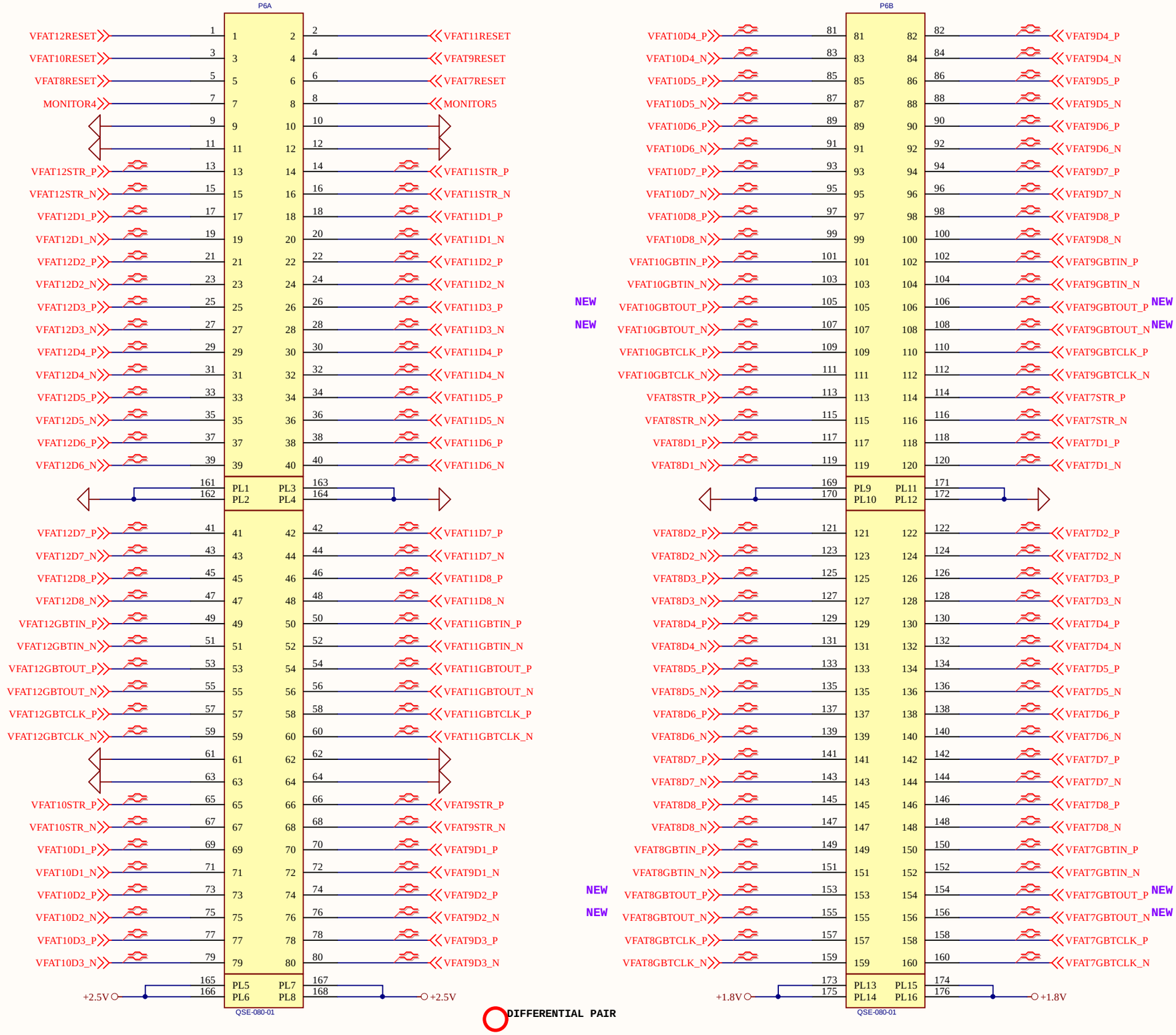
of
12



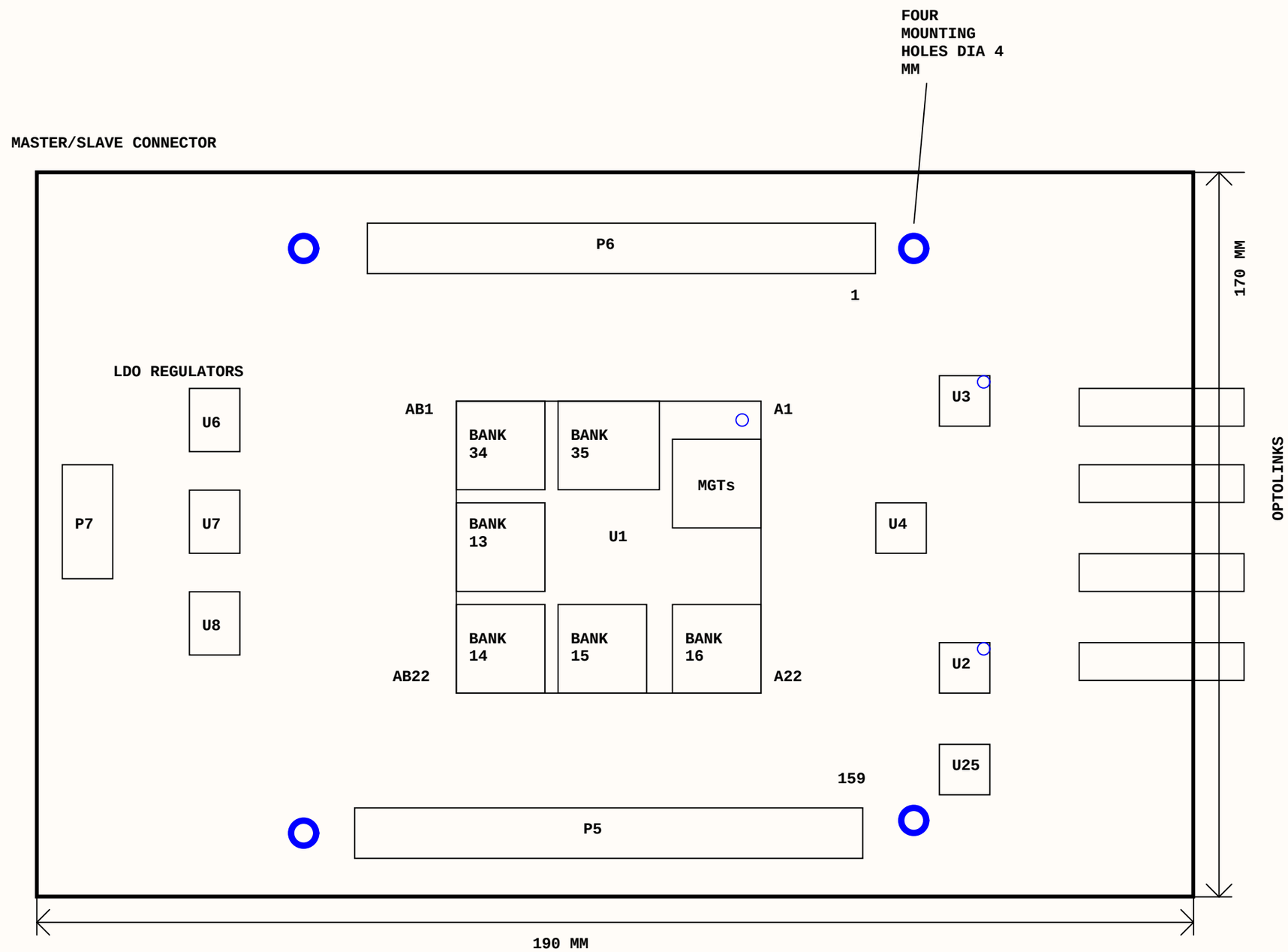

Title: GEB CONNECTOR P5

| Size | Document Number | Rev |
|---|---|---|
| A | | 3.0 |

Date: 04-03-2020 Sheet 9 of 12

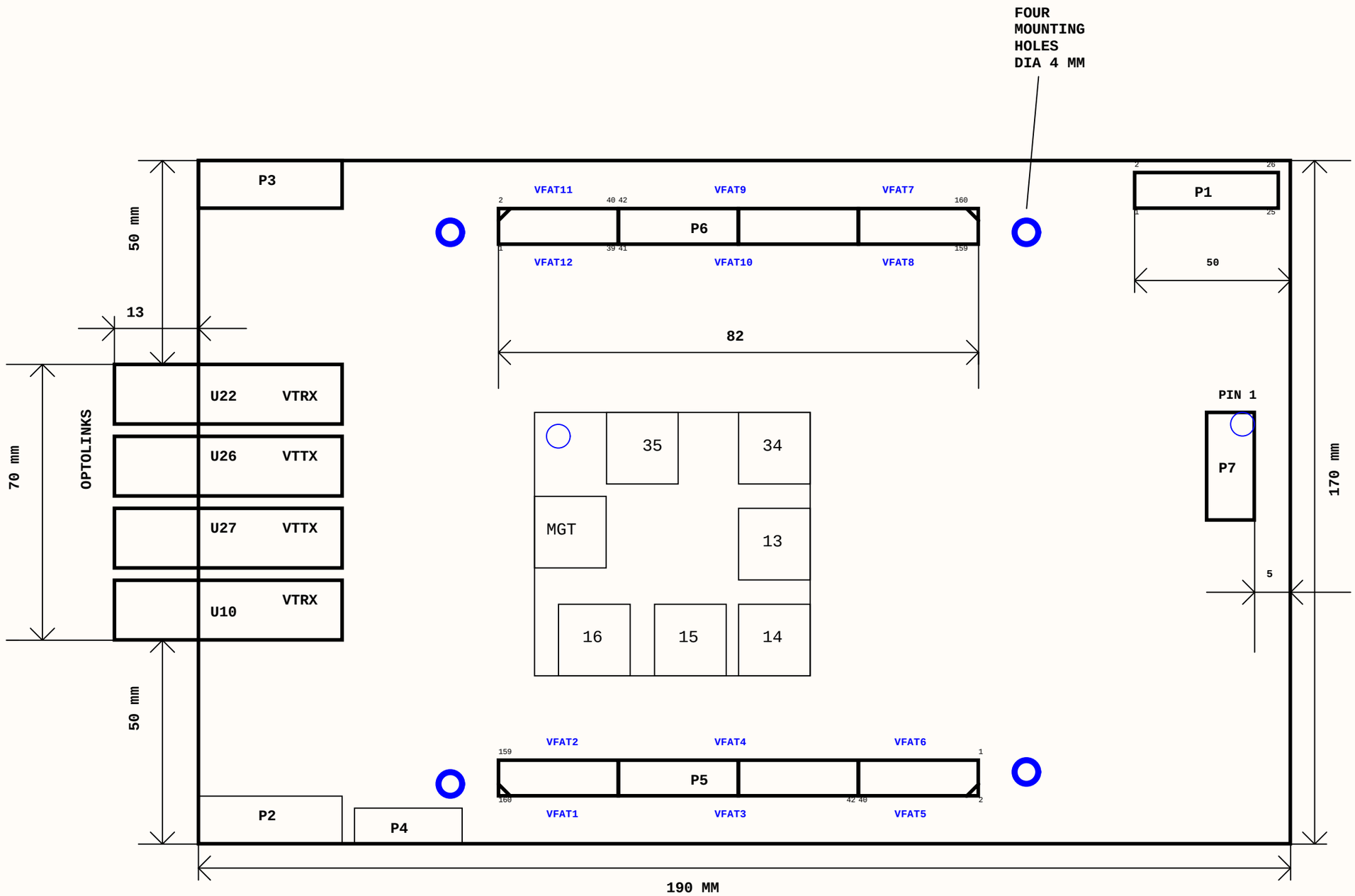



| | | | |
|---|---|---|---|
| Title | GEB CONNECTOR P6 | | |
| Size | A | Document Number | Rev 3.0 |
| Date: | 04-03-2020 | Sheet 10 of 12 | |




U1, U2, U3, U4, U6, U7, U8, U25 ARE
MOUNTED ON THE TOP OF PCB

| | | |
|---|---|---|
| Title: PRELIMINARY PLACEMENT, TOP VIEW | | |
| Size: A | Document Number | Rev: 3.0 |
| Date: 04-03-2020 | Sheet 11 of 12 | |




PCB DIMENSIONS NEED TO BE CAREFULLY REVIEWED AND
APPROVED BEFORE THE PCB DESIGN STARTS

| | | |
|---|---|---|
| Title | PRELIMINARY PLACEMENT BOTTOM | |
| Size A | Document Number | Rev 3.0 |
| Date: 04-03-2020 | Sheet 12 of 12 | |