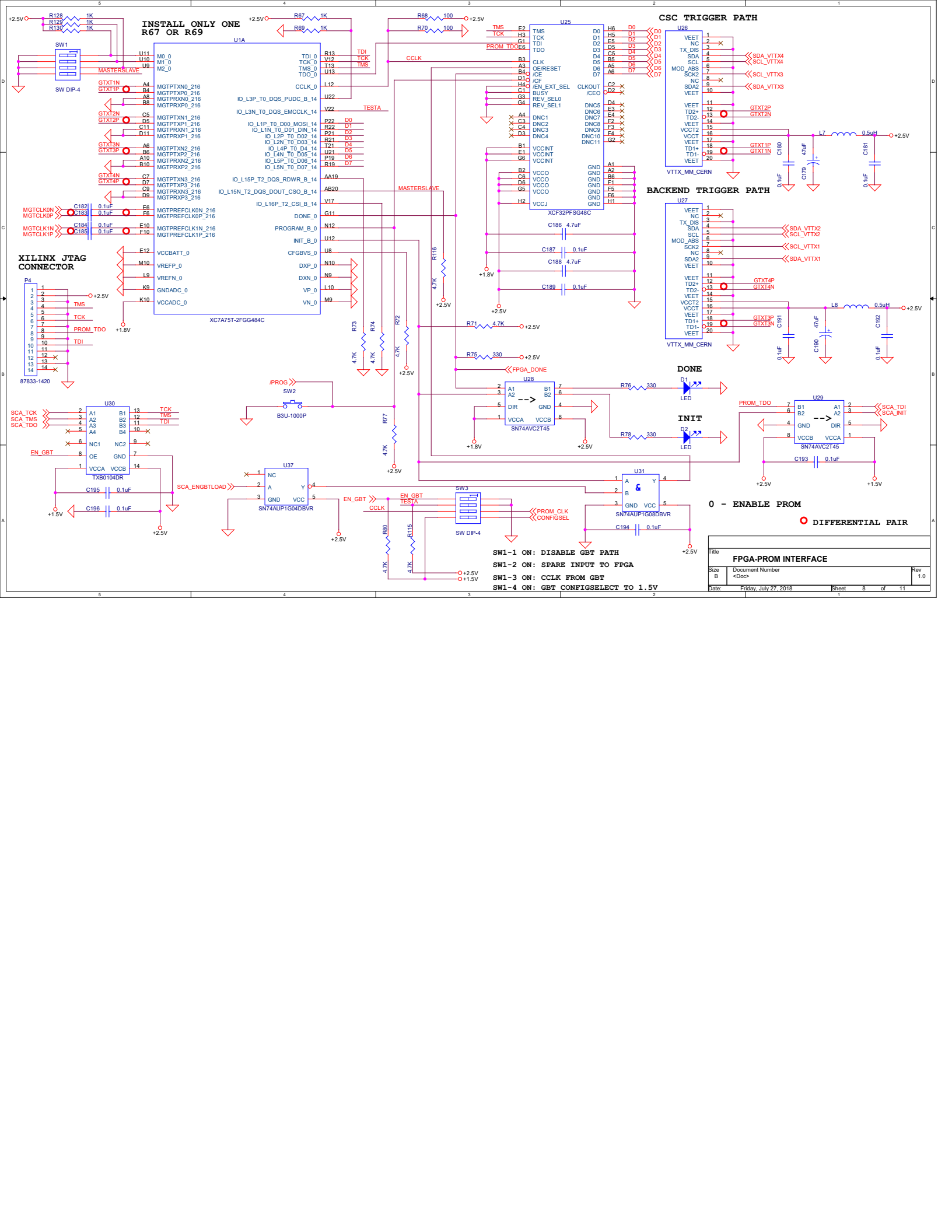
INSTALL ONLY ONE
R67 OR R69
CSC TRIGGER PATH
BACKEND TRIGGER PATH
XILINX JTAG
CONNECTOR
DONE
INIT
0 - ENABLE PROM
DIFFERENTIAL PAIR
SW1-1 ON: DISABLE GBT PATH
SW1-2 ON: SPARE INPUT TO FPGA
SW1-3 ON: CCLK FROM GBT
SW1-4 ON: GBT CONFIGSELECT TO 1.5V
FPGA-PROM INTERFACE
Date: Friday, July 27, 2018
Sheet 8 of 11
Rev 1.0
XC7A75T-2FGG484C
XCF32PFSG48C
VTTX_MM_CERN
SW DIP-4
SN74AVC2T45
SN74AUP1G04DBVR
SN74AUP1G08DBVR
TXB0104DR
87833-1420
B3U-1000P
LED