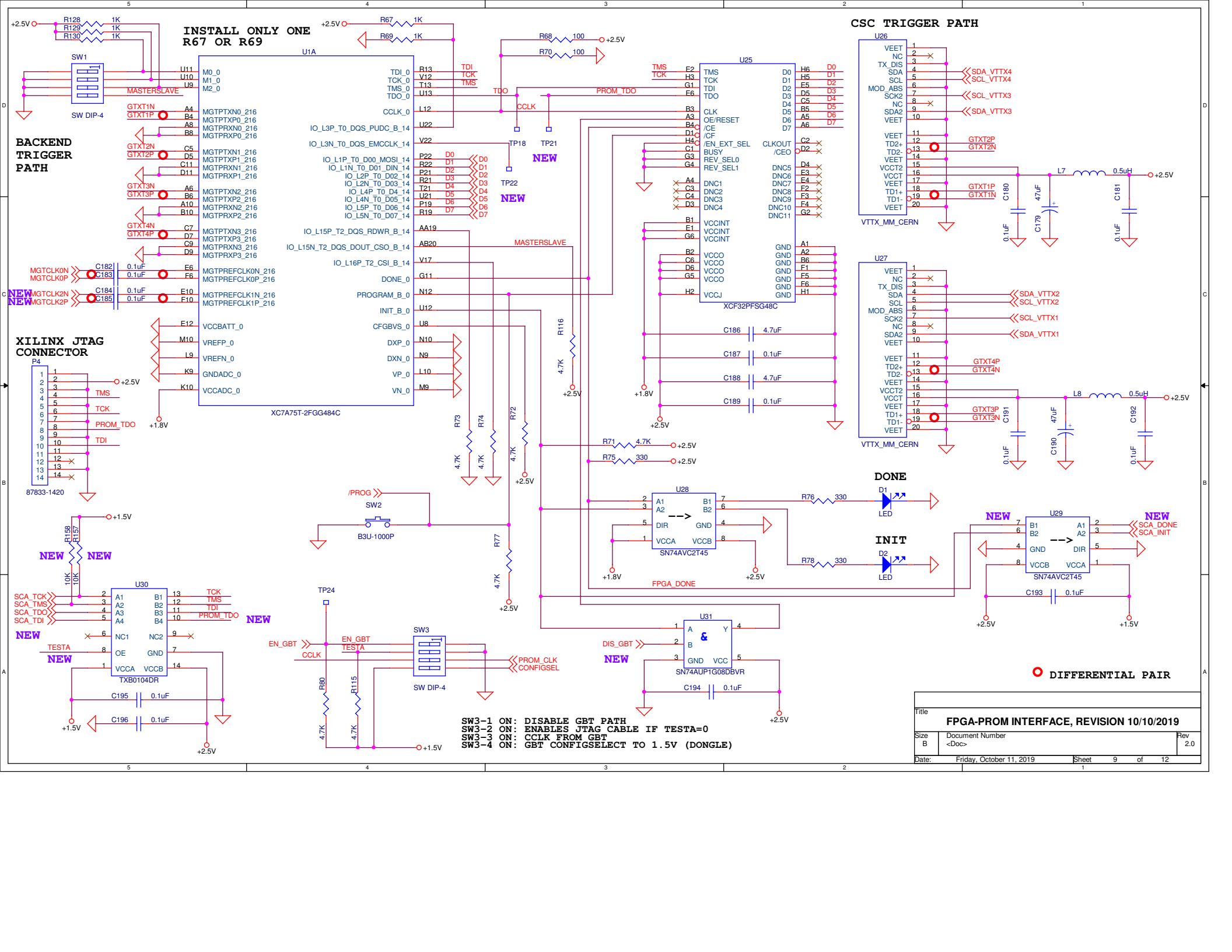
INSTALL ONLY ONE
R67 OR R69
BACKEND
TRIGGER
PATH
XILINX JTAG
CONNECTOR
CSC TRIGGER PATH
U1A
XC7A75T-2FGG484C
U25
XCF32PFSG48C
U26
VTTX_MM_CERN
U27
VTTX_MM_CERN
U28
SN74AVC2T45
U29
SN74AVC2T45
U30
TXB0104DR
U31
SN74AUP1G08DBVR
P4
87833-1420
SW1
SW DIP-4
SW2
B3U-1000P
SW3
SW DIP-4
MASTERSLAVE
PROM_TDO
FPGA_DONE
DONE
INIT
LED
NEW
DIFFERENTIAL PAIR
SW3-1 ON: DISABLE GBT PATH
SW3-2 ON: ENABLES JTAG CABLE IF TESTA=0
SW3-3 ON: CCLK FROM GBT
SW3-4 ON: GBT CONFIGSELECT TO 1.5V (DONGLE)
Title
FPGA-PROM INTERFACE, REVISION 10/10/2019
Size B
Document Number <Doc>
Rev 2.0
Date: Friday, October 11, 2019
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