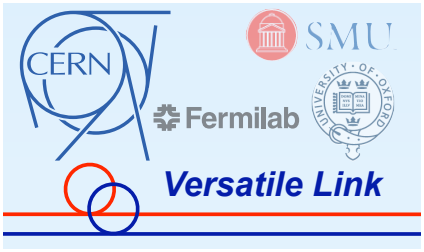

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1140665

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https://cern.ch/project-versatile-link/

Date: 30 May 2017
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Versatile Link Technical Specification, part 2.1

VERSATILE TRANSCEIVER (VTRX)
VERSATILE TWIN TRANSMITTER (VTTX)

Abstract

This document describes the mechanical, electro-optical and environmental specifications of the Versatile Transceiver (VTRx) and the Versatile Twin Transmitter (VTTx) for use in HL-LHC detector front-end component for the Versatile Link optical system.

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History of Changes

Rev. No.	*Date*	*Pages*	*Description of Changes*
0.1	27 Nov. 2008		First prototype version
1.0	14 Dec. 2009		First version for internal distribution
1.1	12 May 2010		Updated i/o specs to include electrical interface and match overall link spec.
1.2	15 Dec. 2010		Updated power levels for Tx out and Rx Sensitivity
1.3	19 Jan. 2011		Added explicit environmental test levels
1.4	13 Apr. 2011		Added EDMS document number
1.5	11 May 2011		Added pinout specification
1.6	17 May 2011		Added related documents
1.7	14 Jun. 2011		Adopted new document template
1.8	20 Jun. 2011		Harmonised environmental constraints
1.81	27 Jun. 2011		Updated with comments from T. Huffman
1.82	24 Aug. 2011		Updated with comments from F. Vasey
1.83	25 Sep. 2011		Increased TX rise/fall times to 70 ps from 60 ps; Updated GBLD jitter contribution from 0.03 to 0.12 UI as per GBLD spec.
1.84	31 Jan.2012		Updated default settings for GBLD-based VTRx; added references to PCB manufacturing files; added info on VTTx variant.
1.9	31 May 2012		Clarification of Pinout
2.0	15 Aug. 2012		Update mention of VTTx explicitly in name of doc and abstract, various comments by FV
2.1	30 Sep. 2013		Pinout and mechanical outline update
2.2	30 May 2017		Change of Tx rise- and fall-times increased from 70 ps to 80 ps due to as-built performance of GBLD

Specification Tree

The hierarchy of the Versatile Link system specification is shown below. The position of the present specification document is highlighted in bold. Line items in italic will not result in specification documents but are shown to ease understanding of the structure.

		EDMS Document Number
Part 1	System	1140664
Part 2	*Components*	
Part 2.1	**Front-end Transceiver**	**1140665**
Part 2.1.1	Transmitter Optical Sub-Assembly (TOSA)	1141155
Part 2.1.2	Laser Driver	1141163
Part 2.1.3	Receiver Optical Sub-Assembly (ROSA)	1141157
Part 2.1.4	Trans-impedance Amplifier	1141160
Part 2.2	*Back-end Components*	
Part 2.2.1	SFP+ Transceiver	1146246
Part 2.2.2	Parallel Optics	1146248
Part 2.3	*Passive Optical Components*	
Part 2.3.1	Optical Fibres and Connectors	1146253

Table of Contents

INTRODUCTION

The Versatile Link project [1] aims to provide a multi-gigabit per second optical physical data transmission layer for the readout and control of High-Luminosity LHC (HL-LHC) experiments. A point-to-point bidirectional system architecture is proposed for which components are currently being assessed and developed, as shown in Figure 1.

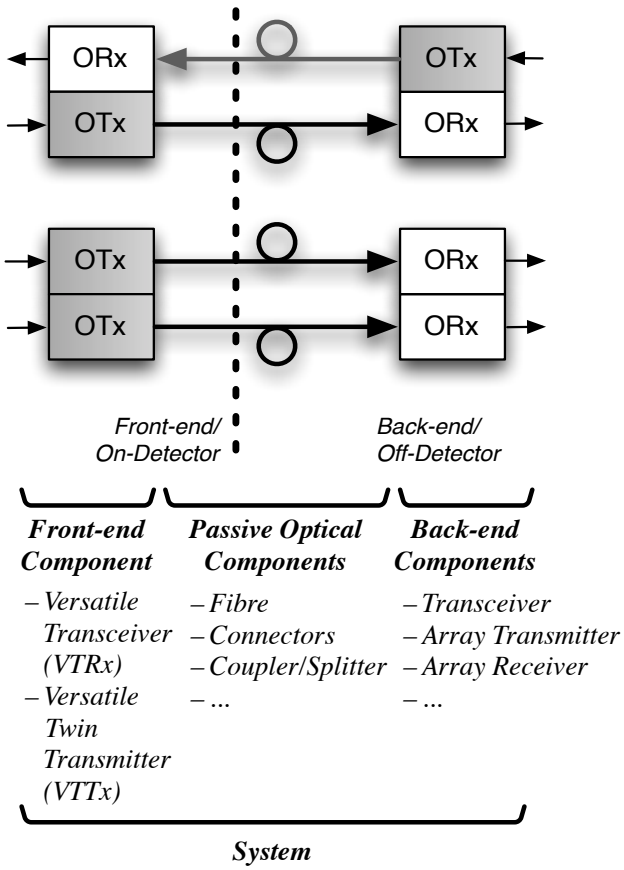

Figure 1: A point-to-point radiation hard optical link for HL-LHC

The front-end component that will enable the configuration of any of the Versatile Link's supported architectures is either a bi-directional module composed of both optical transmitter and receiver – the Versatile Transceiver (VTRx); or a twin transmitter for uni-directional applications. Both SingleMode (SM) and MultiMode (MM) flavours of the VTRx and a MM VTTx will be developed to support the various types of installed fibre-plant in the LHC experiments.

Components situated on the detectors at the front-end must meet strict requirements imposed by the operational environment for radiation- and magnetic-field tolerance, low temperature operation (down to -30°C for tracker-type applications), low mass and volume, and low power consumption. The radiation environment is particularly challenging, as any device placed at the front-end must survive the Si-equivalent of 2×10^{15} n (1MeV)/cm^2, 1×10^{15} hadrons/cm^2 fluence and 500kGy ionizing dose. Experience with optical links deployed in LHC experiments has indicated that even the opto-electronic modules situated on the detectors should be sufficiently rugged to allow handling by integration teams relatively unfamiliar with their use. For this reason the VTRx development aims to minimally customize a commercial form factor bidirectional transceiver module that features a direct optical connector interface.

1. GENERAL SPECIFICATIONS

The VTRx is to be based upon the SFP+ module MSA. Figure 2 shows the block diagram comparison of the VTRx with a standard SFP+. The VTRx is simplified versus the standard transceiver because both the Limiting Amplifier and microcontroller are removed.

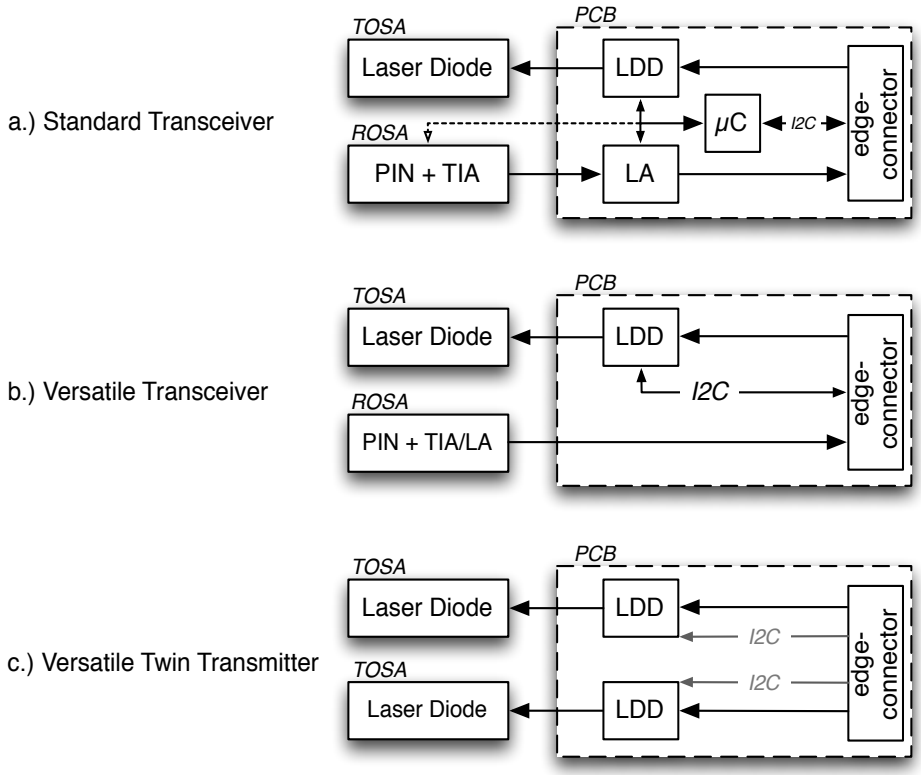

Figure 2: block diagram comparison of a standard SFP+ transceiver, the VTRx, and VTTx showing: Transmitter Optical Sub-Assembly (TOSA), Laser Diode Driver (LDD), Microcontroller (µC), Limiting Amplifier (LA), TransImpedance Amplifier (TIA), PIN photodiode

CERN will supply custom radiation-tolerant LDD ASIC and ROSA component for inclusion in the VTRx and/or VTTx and specify the manufacturer and model of Laser Diode TOSA to be used based upon environmental qualification tests.

Three variants are required

1. Bi-directional variant (VTRx) compatible with SM optical fibre interfaces operating at 1310nm wavelength
2. Bi-directional variant (VTRx) compatible with MM optical fibre interfaces operating at 850nm wavelength.
3. Dual transmitter variant compatible with MM optical fibre interfaces operating at 850nm wavelength (VTTx).

Note that EEL-based variants invert the data passing through the transmitter side of the VTRx and that the Rx side inverts the data w.r.t. a standard SFP+.

Table 1: General specifications

#	Specification	Min	Typ	Max	Unit	Notes
1.1	Data-rate		4.8	5	Gb/s	

2. MECHANICAL SPECIFICATIONS

The VTRx outline mechanical specifications are loosely based upon the SFP+ transceiver specification [2]. See below.

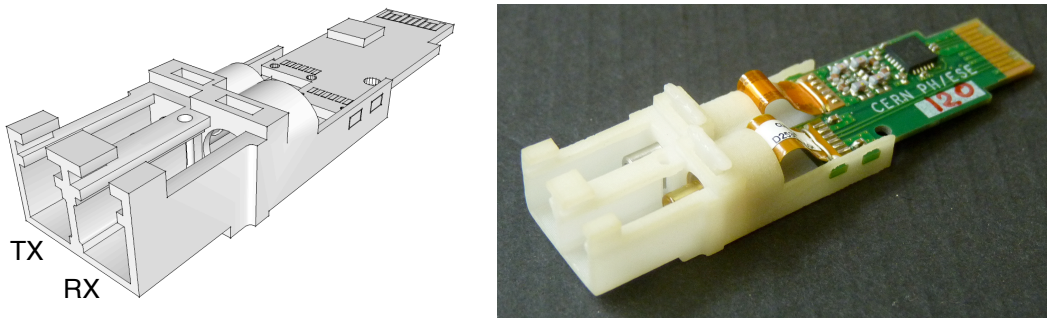

Figure 3: Mechanical sketch (left) and photograph (right) of fully assembled VTRx in SM configuration

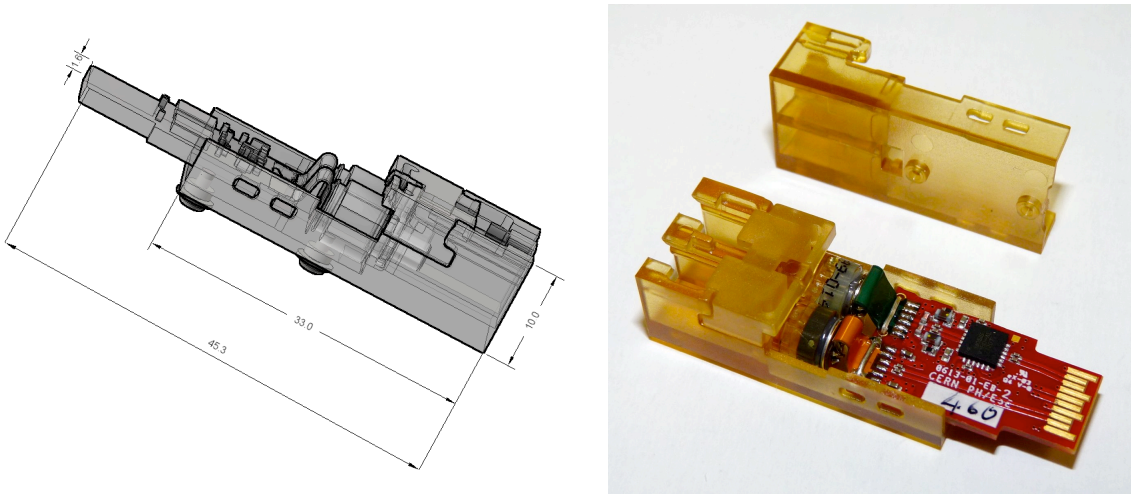

Figure 4: Mechanical sketch of VTTx (left) and photograph of VTRx (right) in MM configuration

Table 2: Mechanical specifications

#	Specification	Min	Typ	Max	Unit	Notes
2.1a	Length of SM variant		55		mm	From connector to edge-connector
2.1b	Length of MM variant		45		mm	From connector to edge-connector
2.2	Width		14.5		mm	Across both connectors
2.3	Height		10		mm	With connector mated
2.4	Mass		5		g	VTRx
			4		g	VTTx
2.5	Material					Non magnetic, low-Z
2.6	Optical Interface					Receptacle for LC connector, 1.25mm ferrule

3. INTERFACE SPECIFICATIONS

The VTRx uses the same card-edge connector specified for the SPF+ module by SFF-8431 [2].

The connector pinout is given in Table 3, Table 4 and shown in Figure 5.

VccR = VccT = 2.5V typ. ±5%

Typical current consumption (TBC):

~200-250 mA (MM VTRx)

~250-300 mA (SM VTRx)

~300-400 mA (MM VTTx)

Table 3: VTRx Connector pinout

Pin #	Signal Name	Description
1	$V_{EE}T$	
2	n/c	
3	Tx_Disable	TX output is on when 0V applied (internal pull-up)
4	SDA	To be pulled up to 1.5 V on Host Board
5	SCL	
6	Mod_ABS	Connected to GND internally
7	n/c	
8	RSSI	Output voltage equivalent to DC current (Iavg) in RX RSSI = $V_{CC}R$ – Iavg*1000
9	n/c	
10	$V_{EE}R$	
11	$V_{EE}R$	
12	RD+	Note that these two pins are inverted w.r.t. a std. SFP+
13	RD-	
14	$V_{EE}R$	
15	$V_{CC}R$	
16	$V_{CC}T$	
17	$V_{EE}T$	
18	TD+	Inverted in the case of SM variants
19	TD-	
20	$V_{EE}T$	

Table 4: VTTx Connector pinout.

Pin #	Signal Name	Description
1	$V_{EE}T$	
2	n/c	
3	Tx_Disable	TX output is on when 0V applied (internal pull-up)
4	SDA	Control for LD1. To be pulled up to 1.5 V on Host Board
5	SCL	
6	Mod_ABS	Connected to GND internally
7	SCK2	Control for LD2. To be pulled up to 1.5 V on Host Board
8	n/c	
9	SDA2	Control for LD2. To be pulled up to 1.5 V on Host Board
10	$V_{EE}T$	
11	$V_{EE}T$	
12	TD2+	Inputs for LD2
13	TD2-	
14	$V_{EE}T$	
15	$V_{CC}T2$	
16	$V_{CC}T$	
17	$V_{EE}T$	
18	TD+	Inputs for LD1
19	TD-	
20	$V_{EE}T$	

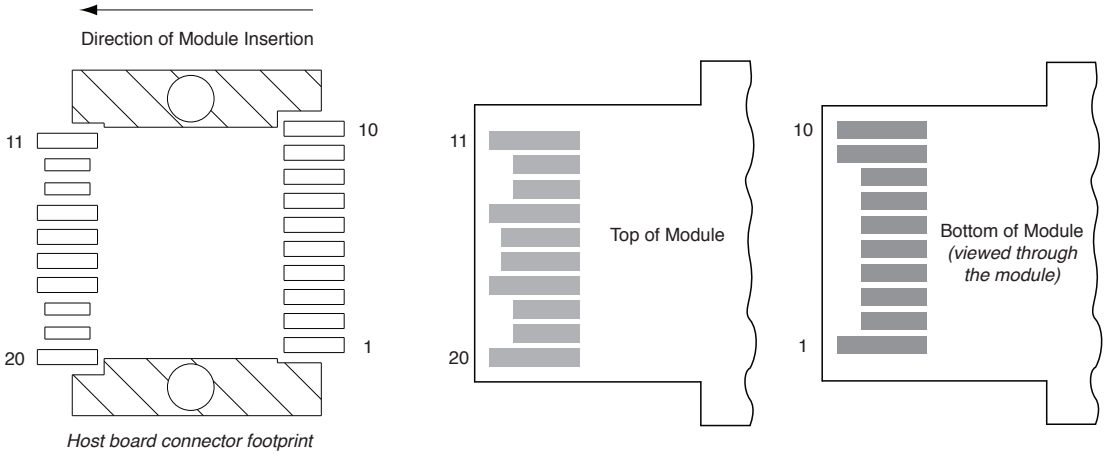

Figure 5: Connector footprints of host board connector (left) and VTRx card-edge (centre & right) showing the pin numbering.

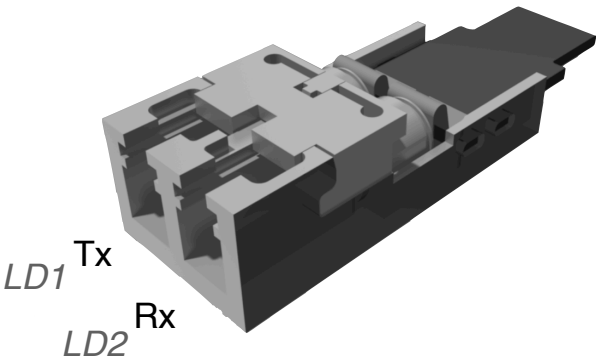

Figure 6: showing the channels of the VTRx and position of LD1 (connected to TD+/-) and LD2 (connected to TD2+/-) on VTTx.

4. ELECTRO-OPTICAL SPECIFICATIONS

Table 5: VTRx electro-optical specifications. In case of dual transmitter (VTTx) only specifications 4.1.1 through 4.1.8 and 4.1.30 through 4.1.35 apply.

#	Specification	Min	Typ	Max	Unit	Notes
4.1.1	TX OMA	300			µW	(-5.2 dBm)
4.1.2	TX Extinction Ratio	3			dB	
4.1.3	TX Eye Opening	60			%	of OMA
4.1.4	TX rise/fall time			80	ps	20%-80%
4.1.5	TX output Total Jitter			0.44	UI	VTRx contribution is 0.25 UI, corresponding to 52 ps at 4.8 Gb/s
4.1.6	TX output Deterministic Jitter			0.26	UI	GBLD spec 0.12 UI (25 ps at 4.8 Gb/s) VTRx contribution is 0.12 UI (25 ps at 4.8 Gb/s)
4.1.7	TX Eye Mask					See Appendix
4.1.8	TX output wavelength		1310		nm	Single-mode variant
			850		nm	Multi-mode variant
4.1.20	RX input Total Jitter			0.48	UI	@ BER = 10^{-12}, OMA = 90 µW GBTIA spec. 40ps
4.1.21	RX input Deterministic Jitter			0.28	UI	OMA = 90 µW
4.1.22	RX Sensitivity			29	µW	Single-mode fibre variant Wavelength = 1310 nm BER = 10^{-12} start of life (-15.4 dBm)
				49	µW	Multi-mode fibre variant Wavelength = 850 nm BER = 10^{-12} start of life (-13.1 dBm)
4.1.30	TX Differential input voltage	100		1200	mV	
4.1.31	TX Input rise/fall time		60	80	ps	20%-80%, Electrical input GBLD spec.
4.1.32	TX Input Total Jitter			0.26	UI	@ BER= 10^{-12}, Electrical input
4.1.33	TX Input Deterministic Jitter			0.14	UI	Electrical input
4.1.34	TX Input Eye Mask					See Appendix
4.1.35	TX Differential input impedance	90	100	110	Ω	

#	Specification	Min	Typ	Max	Unit	Notes
4.1.40	RX Differential output voltage	200		600	mV	
4.1.41	RX Output rise/fall time			50	ps	20%-80%, Electrical output
4.1.42	RX Output total jitter			0.7	UI	@ BER= 10^{-12}, Electrical output, VTRx contribution is 0.34 UI
4.1.43	RX Output deterministic jitter			0.42	UI	Electrical output, VTRx contribution is 0.14 UI
4.1.44	RX Output Eye Mask					See Appendix

5. ENVIRONMENTAL SPECIFICATIONS

Operating Temperature Range: -30 to +60°C

Storage temperature: -30 to +60°C

Relative Humidity: 5 to 85 % (non-condensing)

Magnetic Field: 4T – use of non-magnetic materials is mandatory

Radiation Field: the device will be qualified by CERN for use in upgraded LHC detectors to the following levels depending on the tolerance level required –

- Tracker tolerance level
  - 500 kGy ionizing dose
  - 6 x 10^{15} n/cm^2 20 MeV neutrons
- Calorimeter tolerance level
  - 10 kGy ionizing dose
  - 5 x 10^{14} n/cm^2 20 MeV neutrons

6. CONTROL INTERFACE

The I2C interface of the VTRx/VTTx allows the user to set the operating point of the transmitter by programming the LDD ASIC. The default configuration of the LDD upon power up depends upon the variant. Variants based on the CERN custom LDD and edge-emitters start with a bias current of 40 mA and a modulation current of 20 mA. Variants based on the CERN custom LDD and VCSELs start with a bias current of 6 mA and a modulation current of 6 mA. Full details of the LDD programming registers are given in the specification of the LDD (see EDMS document no. 1141163). The tables below give an overview of the register maps with typical settings for different VTRx/VTTx variants:

Table 6: showing typical LDD programming values for SM VTRx with GBLD v.4 LDD and edge-emitter TOSA. LDD I2C base address is 0x7E.

Register Address	Register Name	Typical Setting	Notes
0x0	Control	0xC7	Both Drivers enabled, pre-emphasis off
0x1	Modulation Current	0x26	20 mA
0x2	Bias Current	0xAF	20 mA
0x3	Pre-emphasis	0x00	0 mA
0x4	Modulation mask	0xFF	
0x5	Bias mask	0xFF	
0x6	Pre-driver	0x06	

Table 7: showing typical LDD programming values for MM VTRx/VTTx with GBLD v.4 LDD and VCSEL TOSA. LDD I2C base address is 0x7E.

Register Address	Register Name	Typical Setting	Notes
0x0	Control	0x97	Driver A enabled, pre-emphasis off
0x1	Modulation Current	0x19	6 mA
0x2	Bias Current	0x19	6 mA
0x3	Pre-emphasis	0x00	0 mA
0x4	Modulation mask	0xFF	
0x5	Bias mask	0xFF	
0x6	Pre-driver	0x06	

7. GLOSSARY

Diagrams of measurement definitions

8. APPENDIX

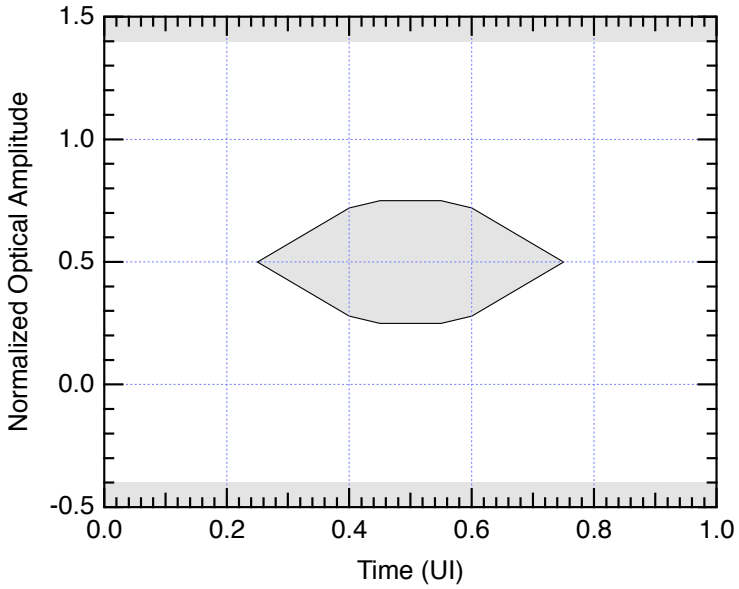

Figure 7: Optical output mask

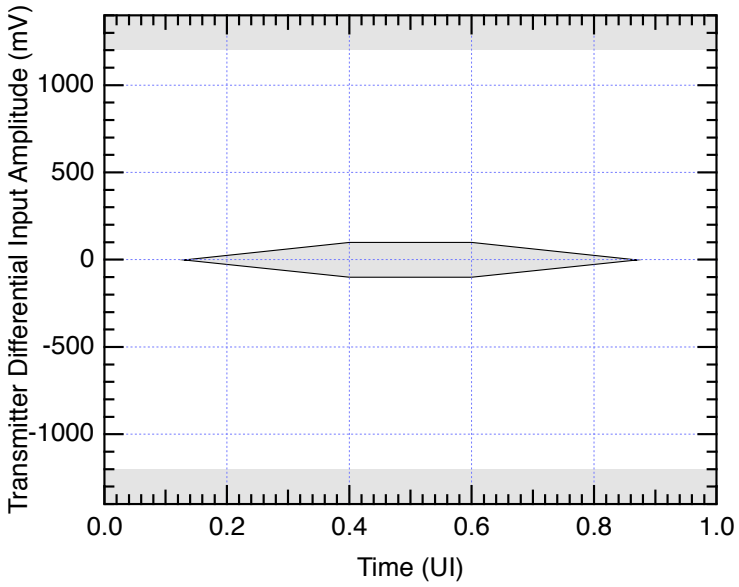

Figure 8: Transmitter electrical input mask

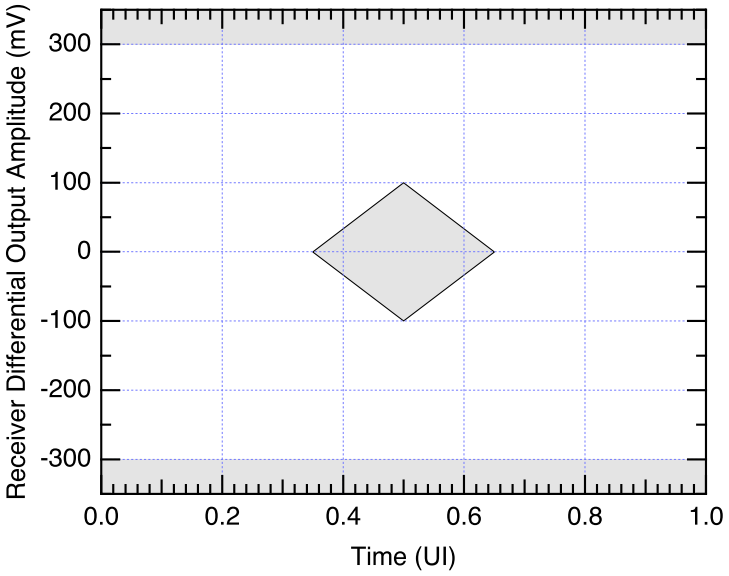

Figure 9: Receiver electrical output mask

9. REFERENCES

[1] "The Versatile Link, A Common Project For Super-LHC", L. Amaral et al., JINST 4 P12003, Journal of Instrumentation, Volume 4, December 2009

[2] "SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+ Revision 4.1", The SFF Committee, 6th of July 2009

[3] "VTRx design files", EDMS item id: CERN-0000078404, available to registered users at https://edms.cern.ch/item/CERN-0000078404/0