GE2/1 Optohybrid Board OH2 (LpGBT)

Draft Specification 1.0

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Introduction

The GE2/1 Optohybrid board OH2 is the second revision of the original OH design [1]. It provides readout and trigger interfaces for 12 VFAT3 ASICs residing on the GEB board. A comprehensive description of the GE2/1 GEM design and electronics can be found in the Technical Design Report [2]. While the first revision of the GE2/1 OH was based on two GBTx [3] ASICs and one SCA [4] ASIC, the second revision utilizes only one newer LpGBT [5] ASIC. A block diagram of the OH2 board is shown on Fig.1.

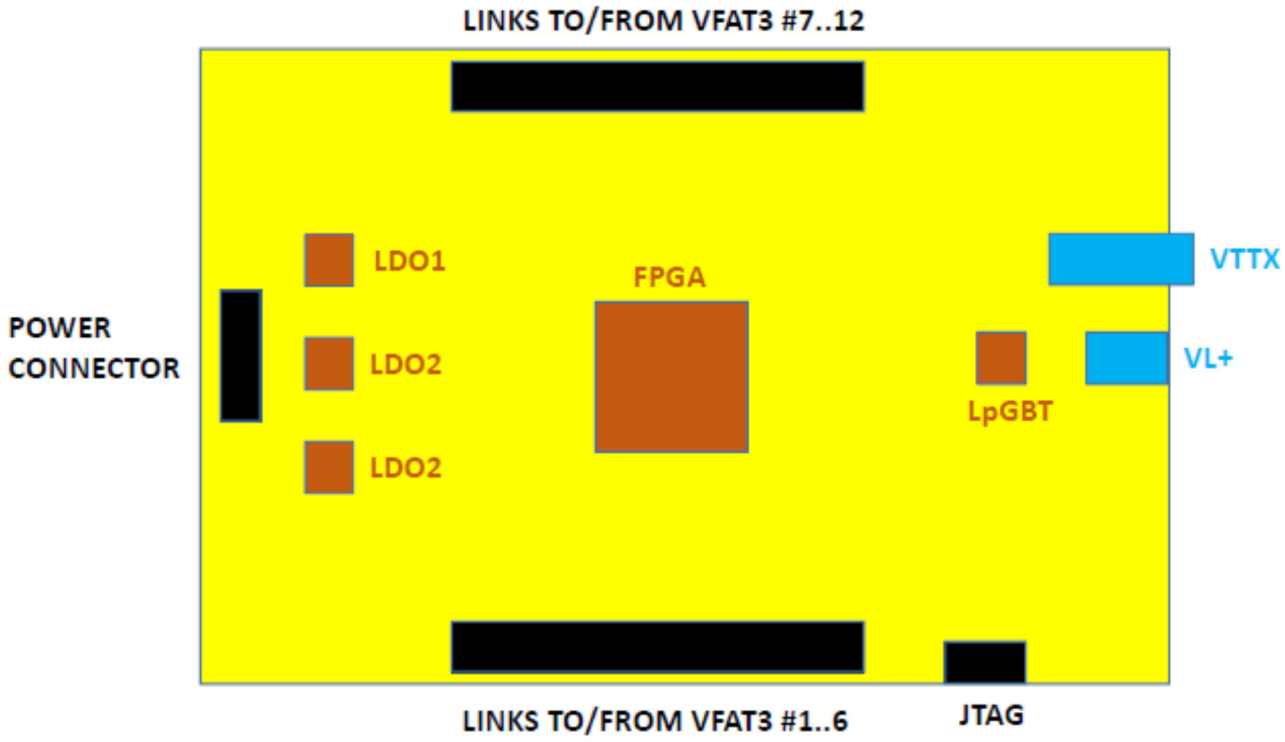

Fig.1: Block diagram of the OH board

1. FPGA

The FPGA is needed to build trigger clusters and transmit them to the local processor (CSC OTMB) and to central (backend) trigger processor farm. Xilinx Artix-7 XC7A75T-2FGG484C [6] (U1) has been selected due to:

- Sufficient number of IO pins (285 total) and logic resources
- Low power consumption
- Flexible IODELAY block
- Availability and low cost
- Sufficient radiation tolerance [7]-[9]

The main FPGA functions and interfaces are:

- Two Samtec QSE-080-01-L-D-A connectors are used for all links to 12 VFAT3 ASICs. Two mating Samtec QTE-080-03-L-D-A are used on GEB boards. The FPGA receives 9 differential signals from each VFAT3, including 8 data bits (VFATxDyN/P, where x=1..12 and y=1..8) and one Strobe signal VFATxSTRN/P). For optimal signal routing, some of these differential signals are inverted at the FPGA inputs, see Appendix A for details.
- Banks 13,14,15,16,34,35 are used for VFAT3 connections, all VCCIO powers are 2.5V
- Bank 0 is also powered by 2.5V. A dedicated configuration banks voltage select CFGBVS="1".
- One global clock (FPGACLK1P/N) are provided from the LpGBT ASIC
- 12 differential outputs from the FPGA to the LpGBT ASIC (FPGA[1..12]GBTIN).
- The FPGA is accessible via the JTAG connector P4 (Molex 87833-1420)
- Configuration pins M0..M2 with embedded pull-ups can be grounded with a switch SW1-1..3 to select the configuration mode (Slave SelectMAP is a default mode).
- There are 4 MGT links in this FPGA. Two global clocks MGTREFCLK0P/N and MGTREFCLK1P/N are coming from the LpGBT clock outputs with programmable frequency and phase). Two MGT outputs are connected to the VTTX optical transmitter. The other two are not used. All MGT receivers are not used and are all grounded.
- PUDC_B input is set to "0" with an external resistor R69 to enable internal pull-ups on SelectIO pins.
- EMCCLK external master configuration clock is not used.
- Internal ADC is not used.
- The battery backup supply is not used.

2. FPGA Configuration from the LpGBT ASIC

The configuration from the LpGBT is provided from the EDOUT[20…23] and EDOUT[30..33] outputs and the configuration clock comes from the ECLK28 to CCLK input of the FPGA. These 9 differential links are translated from the SLVS to CMOS levels (using SN65LVDT2 translators) and provided to the FPGA dedicated inputs.

The state of the FPGA_DONE line can be monitored on GPIO13. Hard Reset (/PROG=0) can be produced from the GPIO12 and also from a push button SW2.

3. LpGBT GBT Links and Control Circuitry

The LpGBT ASIC serves all 12 VFAT3 ASICs residing on the GEB board. A link to each VFAT3 comprises three differential signal pairs:

- VFATxGBTOUTN/P, where x=1..12; these are the outputs from the LpGBT to VFAT3. A single output EDOUT00 is used with a 1-to-12 fan-out (Micrel part number SY89113U). The GEB and VFAT boards must implement addressing scheme to be able to decode its unique addresses.

- VFATxGBTINN/P, where x=1..12; these are the inputs from VFAT3 to the LpGBT; 12 differential pairs in total.

- VFATxGBTCLKN/P, where x=1..12, these are clock outputs from the LpGBT to VFAT3. A single output ECLK0 is used with a 1-to-12 fan-out (Micrel part number SY89113U). The GEB and VFAT boards must implement addressing scheme to be able to decode its unique addresses.

The LpGBT ASIC operates in 10G transceiver mode with FEC12 protocol, so all MODE[3:0] pins are set to "1111" with external pull-up resistors.

12 differential inputs FPGAxGBTIN (x=1..12) from the FPGA to the LpGBT are provided to deliver the trigger clusters constructed in the FPGA to the backend processor.

The **SC_I2C pin** selects I2C (if "1") or serial (if "0") interface channel for ASIC configuration. It has an internal pull down resistor. With an SW4-1 switch this pin can be connected to a pull up resistor to allow I2C access.

STATEOVRD pin disables the automatic power-up state machine ("0" – normal operation; "1" – power-up state machine halted). It has an internal pull down resistor, but can be set to "1" with the SW4-2 and external pull up resistor.

PORDIS disables build-in power on reset (POR) circuit ("0" – normal operation, "1" – power on reset block disabled). It has an internal pull down resistor, but can be set to "1" with the SW4-3 and external pull up resistor.

RSTOUTB output delivers an active low reset pulse. With a SW4-4 it can be provided to the RESET input of the VL+ optical transceiver.

REFCLKP and **REFCLKN** pins are connected to test points.

LOCKMODE is permanently set to "1" (reference-less locking; recover frequency from the data stream).

VCOBYPASS is permanently set to "0" (normal operation; system clocks come from PLL/CDR).

ADR[0..3] pins specify the lower significant bits of the LpGBT chip address used in I2C and/or serial control interfaces. They all are permanently set to "0".

M0SCL/M0SDA I2C Master channel 0 is connected to the VL+ module. **M1SCL/M1SDA** I2C Master channel 1 is connected to the VTTX module. **M2SCL/M2SDA** I2C channel 2 is not used. All three channels have external pull up resistors to 1.2V. **SLSCL/SLSDA** Slave I2C channel is not used and has external pull up resistors to 1.2V as well.

TSTCLKIN_N/P are not used and left unconnected.

VDAC signal is provided to a test point.

VREF power of 1.0V is provided from the ADR130BLUZ voltage reference.

4. LpGBT General Purpose IO Pins and ADC Inputs

The LpGBT ASIC provides 12 Reset signals to VFAT3 ASICs. These are dedicated outputs GPIO[0..11] with direct connections to VFAT3. VFAT3 has an embedded pull-down resistor on these inputs. Active "1" for reset.

The state of the FPGA_DONE output can be read to GPIO13.

GPIO12="1" generates Hard Reset to /PROG inputs of the FPGA.

GPIO14 and GPIO15 are provided to test points and reserved for future use.

ADC inputs of the LpGBT ASIC are assigned as below:

- IN0: +1.8V (from GEB)
- IN1: +1.2V (from GEB)
- IN2: +2.5V (from GEB)
- IN3: MONITOR1 current monitor from FEAST1 on GEB (1.8V for the OH board)
- IN4: MONITOR2 current monitor from FEAST2 on GEB (1.2V for the OH board)
- IN5: MONITOR3 current monitor from FEAST3 on GEB (2.5V for the OH board)
- IN6: MONITOR4 current monitor from FEAST4 on GEB (1.2V for VFAT1..VFAT6)
- IN7: MONITOR5 current monitor from FEAST5 on GEB (1.2V for VFAT7..VFAT12)

5. Optical Links

The LpGBT ASIC uses a custom multi-mode VL+ [10] optical transceiver.

The FPGA uses one custom multi-mode 2-channel VTTX transmitter.

6. Power Distribution

Internal metal planes in the QSE connectors are used to deliver +1.2V, +1.8V and +2.5V powers from GEB boards (Fig.3). These powers and GND can also be provided from the Samtec HLE-108-02-F-DV-A connector (this option should be very convenient for testing and debugging). The GEB board may also provide powers through mating HW-08-16-F-D-290-SM connector (11.05 mm total mating height). Pin assignment is shown in Fig.6.

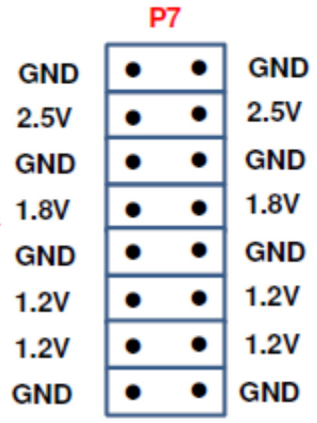

Fig.6: Pin assignment of the power connector P7 (as seen from the bottom of the PCB)

+1.2V is needed for the LpGBT ASIC.

+2.5V is used by the FPGA, VTTX, SN65LVDT2, and some other digital logic parts.

There are three MIC69502 voltage regulators on the OH board:

- +1.0V for the internal FPGA core,
- +1.0V for MGT receivers
- +1.2V for MGT transmitters.

The input for all three regulators is +1.8V. Estimates of power consumption are the following:

- FPGA with functional design: <2W;
- LpGBT ASIC 1.5A x 1.2V = 1.8W (est)
- VTTX: 0.3A x 2.5V = 0.75W (max)
- VL+: 0.5A x 2.5V = 1.25W (est)
- Other parts: < 1W
  Total: < 7W

7. LEDs and Test Points

There are the following green LEDs mounted on top of the OH board:

- FPGA_DONE output from the FPGA
- FPGA_INIT
- LpGBT READY
- +2.5V
- +1.8V
- +1.2V
- +1.0V
- Two spare outputs from the FPGA

There are the following test points:

- 4 test points from the FPGA
- +1.0VAVCC, +1.2VAVTT, +1.0VCCINT, +1.2V, +1.8V, +2.5V, GND.

References

[1] https://twiki.cern.ch/twiki/bin/view/CMS/GE21OHBoardTwiki

[2] CMS TECHNICAL DESIGN REPORT FOR THE MUON ENDCAP GEM UPGRADE CERN-LHCC-2015-012 CMS-TDR-013 30 September 2015. Available at https://cds.cern.ch/record/2021453/files/CMS-TDR-013.pdf

[3] https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf

[4] https://espace.cern.ch/GBT-Project/GBT-SCA/Manuals/GBT-SCA-UserManual.pdf

[5] https://lpgbt.web.cern.ch/lpgbt/manual/

[6] https://www.xilinx.com/products/silicon-devices/fpga/artix-7.html

[7] https://www.xilinx.com/support/documentation/user_guides/ug116.pdf

[8] https://indico.cern.ch/event/489996/contributions/2291857/attachments/1345403/2028662/TWEPP_Artix7.pdf

[9] http://cds.cern.ch/record/2119894/files/ATL-MUON-SLIDE-2016-010.pdf

[10] https://edms.cern.ch/ui/#!master/navigator/project?P:1930058715:1767090345:subDocs

Appendix A

Inverted differential inputs from VFAT3[1..12] to the FPGA

VFAT1D1
VFAT1D2
VFAT1D3
VFAT1D4
VFAT1D5
VFAT1D6
VFAT1D7
VFAT1D8

VFAT2D1
VFAT2STR

VFAT8D3
VFAT8D4
VFAT8D6
VFAT8D7
VFAT8D8

VFAT9D6

VFAT10D2
VFAT10D3
VFAT10D4
VFAT10D5
VFAT10D7
VFAT10D8

VFAT11D1
VFAT11D2
VFAT11D3
VFAT11D4
VFAT11D5
VFAT11D6
VFAT11D7

VFAT12D1
VFAT12D3
VFAT12D4
VFAT12D5
VFAT12D7
VFAT12D8
VFAT12STR