7 Series FPGAs Packaging and Pinout

Product Specification

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/14/2018	1.16	In Chapter 2: Updated the links to individual ZIP files in Table 2-1 and Table 2-2. In Chapter 3: Added XC7A12T, XC7A25T, and Spartan-7 device diagrams. In Chapter 4: In response to XCN16004: Forged to Stamped Lid Conversion for Monolithic FPGA Flip Chip Packages, added Figure 4-34: FF900 and FFG900 (XC7K325T and XC7K410T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid and Figure 4-36: FF1156 and FFG1156 (XC7K420T and XC7K480T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid.
07/24/2017	1.15	Added the XC/XA Spartan-7 devices, the XC7A12T/XA7A12T and XC7A25T/XA7A25T devices, and the CPG238 package. Removed the *Preface*. In Chapter 1: Added an Important note on page 21. Updated the DDR DQS strobe pin direction in Table 1-12. Added the Migrating between Devices section. Updated the CPG236 package on page 39. Corrected the package list in XC7VX485T and XQ7VX485T Banks. In Chapter 2: Added Package Specifications Designations section. In Chapter 4: Revised Figure 4-47, the RF1761 mechanical drawing. In Chapter 5: Added devices to Table 5-1. In Table 5-3, changed the Peak Package Reflow Body Temperature for some packages to 245°C. In Chapter 6: Added Figure 6-1: Spartan-7 Device Package Marking. Updated Figure 6-2, Figure 6-3, and Figure 6-4 to add the bar code marking and the Pb-free character. Added the Pb-free Character description as outlined in XCN16022: *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages*. Revised the Bar Code section of Table 6-1 to include changes outlined in XCN16014: *Top Marking change for 7 Series, UltraScale, and UltraScale+ Products*. In Chapter 7: Added packages to Table 7-1. Added Appendix C, Additional Resources and Legal Notices. Moved the Disclaimer Notices and References sections to Appendix C.
03/23/2016	1.14	Updated to add the XQ7VX690T in the RF1158 package. Added RoHS compliant options (FFV packages) where applicable. In Table 1-12, updated the SRCC description. Updated Figure 4-7 with solder ball composition changes. Refined the A2 dimensions in Figure 4-12 and Figure 4-22. Added the FFV1761 package (Figure 4-42). Added the RF1158 to Figure 4-46. Completely revised Chapter 5, Thermal Specifications with industry standard guidelines for all sections. Updated the Thermal Management Strategy section. Updated the Thermal Interface Material section previously in Appendix B. Added the Applied Pressure from Heat Sink to the Package via Thermal Interface Materials section. In Appendix B: Moved and renamed the *Reasons for Thermal Management* section to Chapter 5. Removed the *Package Loading Specifications* section.
11/13/2014	1.13	Added XC7A15T and XA7A15T devices throughout the specification.

Date	Version	Revision
10/28/2014	1.12	Added a discussion on ULA materials on page 16. Added clarifications with regards to Artix-7 devices throughout the document including Pin Compatibility between Packages and Note 1 to Table 3-2. Updated *Note* on page 71. In Table 5-2 and Figure 5-7, revised the Peak temperature (body) values and the Ramp-up rate and Ramp-down rate to 2°C/s. Removed references to CL/CLG packages in Table 5-3 and Appendix A. Updated Figure 5-4. Also added the Peak Package Reflow Body Temperature values to Table 5-3. Added Heat Sink Removal Procedure, Package Pressure Handling Capacity, Post Reflow/Cleaning/Washing, and Conformal Coating. Added Chapter 7, Packing and Shipping.
03/18/2014	1.11	Added the XC7A35T, XC7A50T, and XC7A75T throughout document including Table 1-3, Table 1-8, Figure 1-6, Figure 1-7, Figure 1-8, Table 2-2, Table 3-2, Table 5-1, and added or updated Figure 3-41 through Figure 3-80. Also added the automotive XA Artix-7 FPGA versions (XA7A35T, XA7A50T, XA7A75T, and XA7A100T) and the defense-graded Artix-7Q device (XQ7A50T) with applicable packages. In Table 1-1, updated Note 1. In Table 1-12, updated Note 2 and the description of PUDC_B. Added links to all the ruggedized packages in Chapter 2, 7 Series FPGAs Package Files. Updated the DCI pin description in the legends for all the Memory Groupings diagrams in Chapter 3, Device Diagrams. Added CPG236 package to document including Figure 4-7, Table 5-1, and Table A-1. Added CSG325 to document including updating Figure 4-9. This update includes a change in the A_2 dimensions for the CSG324. Replaced Figure 4-16: FG484 and FGG484 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs, page 273 with a new drawing with updated dimensions. Replaced Figure 4-17: FG676 and FGG676 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs, page 274 with a new drawing with an updated mechanical drawing. Updated the M specification in Figure 4-19: RB484 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs, page 276. Replaced Figure 4-33: FF676, FFG676, and FFV676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs, page 290 with a new drawing where the lid is updated with four corner posts. Updated the References links in Chapter 5, Thermal Specifications. Revised the M diameter for FF/FFG, FB/FBG, FH/FHG, FL/FLG, and RF/RB/RS packages in Table A-1.

Date	Version	Revision
11/15/2013	1.10	Updated disclaimer. Added the XQ devices and RB/RF/RS package information throughout document. Added Note 1 to Table 1-2 and Note 6 to Table 1-12. Revised the super logic region numbers in Figure 1-20. Removed the Virtex-7 HT devices (HCG packages). Before removal, revised the super logic region numbers in Figure 1-20: XC7VH870T Banks. For packaging and pinout information on the Virtex-7 HT devices see www.xilinx.com/member/gtz/index.htm. Updated the legend in Figure 3-141, Figure 3-144, Figure 3-145, Figure 3-148, Figure 3-209, Figure 3-212, Figure 3-213, Figure 3-216, Figure 3-217, and Figure 3-220. Updated the A and A2 dimensions in Figure 4-18: FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Artix-7 FPGAs, page 275. Added Note 1 and updated the data in Table 5-1. Updated the Pb-Free Reflow Soldering in Chapter 5 discussion. Removed the engineering sample notation from the top mark drawings in Figure 6-2, Figure 6-3, and Figure 6-4. Updated the L2E description in Table 6-1. Updated Appendix A.
02/14/2013	1.9	Clarified pins in Figure 3-89. Updated Figure 4-18 and Figure 4-22 and added Figure 4-23 and Figure 4-24. Revised Figure 4-35 and Figure 4-40. In Table 5-1, updated data for Artix-7 FPGAs, XC7K160T FF/FFG/FFV676, Virtex-7 T FPGAs and XC7VX1140T. Updated Appendix B.
10/15/2012	1.8	Removed the following devices: XC7A350T, XC7V1500T, XC7VH290T. Added Figure 4-26 and updated drawing in Figure 4-27. Added Note 5 to Figure 4-40. Updated A2 dimension in Figure 4-44. Updated the aaa dimension in Figure 4-43 and Figure 4-45. Updated the JEDEC Moisture Sensitivity Level (MSL) for the Flip-Chip packages on page 323.
07/20/2012	1.7	In Table 1-12, updated the Other Pins section. Added the XC7VH290T, XC7VH580T, and XC7VH870T and associated HCG packages to all appropriate chapters, tables, and figures. Added the SBG484 package for the XC7A200T devices to all appropriate chapters, tables, and figures. Updated the XC7VX1140T-FLG1926 headings in Table 2-5, Figure 3-209 through Figure 3-212, and Figure 4-45. Updated GTP Quad numbers in Figure 1-9, Figure 3-74, and Figure 3-78. Also added numbers to Figure 3-77 and Figure 3-80. Updated the XC7V585T-FFG1761 figures: Figure 3-137 and Figure 3-140. Added new mechanical drawings for the Artix-7 FPGAs in Chapter 4 along with Figure 4-27, Figure 4-35, and Figure 4-36, and updated Figure 4-35. In Table 5-1, updated data throughout and added XC7VX1140T (FL1926) and XC7VH580T data. Added Figure 6-2: Artix-7 Device Package Marking.

Date	Version	Revision
05/24/2012	1.6	Removed the FFG1933 and FLG1933 packages throughout. Added the FLG1926 package where appropriate. Updated the Introduction in Chapter 1. Updated XC7K420T in Table 1-10. Added Note 7 to Table 1-12. Updated the description and figure in the XC7K420T Banks and XC7VX550T Banks sections. Updated Figure 3-86, Figure 3-90, Figure 3-94, and Figure 3-34. Added Figure 3-209 through Figure 3-212. Added Figure 4-14: FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs. Revised specifications and added capacitor location figures for: Figure 4-25: FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs Figure 4-28: XC7K325T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations Figure 4-29: XC7K410T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations Figure 4-30: FB900, FBG900, and FBV900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs Figure 4-31: XC7K325T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations Figure 4-32: XC7K410T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations Figure 4-37: FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs Figure 4-40: FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 Flip-Chip BGA Package Specification for Virtex-7 FPGAs Added Thermal Management Strategy, Heat Sink Removal Procedure, and updated Soldering Guidelines in Chapter 5. Updated Table A-1.

Date	Version	Revision
02/03/2012	1.5	Updated Table 1-3 and Table 1-5 and added Table 1-6. Updated Table 1-7 and Table 1-9 and added Table 1-10. Revised Note 2 in Table 1-12. Removed Figures 1-1 and 1-2 along with references to the XC7A8, XC7A15, XC7A30T, and XC7A50T. Added Figure 1-10 and Figure 1-3. Clarified Figure 1-14 though Figure 1-17, Figure 1-19, Figure 1-23, and Figure 1-26. Updated Table 2-4 and added Table 2-5. Added devices to Table 3-2 and revised Table 3-3 (XC7K420T and XC7K480T). Updated Table 3-4 and added Table 3-5 and Table 3-5. Revised specifications in: Figure 4-22: FB484, FBG484, and FBV484 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch). Figure 4-25: FB676, FBG676, and FBV676 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch). Figure 4-30: FB900, FBG900, and FBV900 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch) and combined with Figure 4-6. Figure 4-40: FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch). Added thermal resistance data to Table 5-1 and added the Soldering Guidelines section. Added Appendix B.
10/17/2011	1.4	Revised the FBG484 and FBV484 Package section describing XC7K160T Banks. Added the mechanical drawings: Figure 4-41 and Figure 4-45. Updated Figure 4-44 to include the FF(G)1928 package. Added thermal resistance data to Table 5-1.
10/03/2011	1.3	Added Artix-7 device information including updating Table 1-1, adding Table 1-3, Table 1-8, Table 2-2, and Table 3-2. Clarified the interposer in Figure-12 and Figure 1-19. Revised horizontal center for the XC7VX415T in Figure 1-21. Updated the DXP_0, DXN_0 description and notes in Table 1-12. Added devices to the Die Level Bank Numbering Overview section. Clarified the I/O banks summary section. Added Artix-7 device diagrams in the CSG324 package. Added XC7V585T device diagrams Figure 3-133 through Figure 3-140. Moved AD4P/N, AD12P/N, and AD5P/N pins from [IO_L2P_T0_35:IO_L4N_T0_35] to [IO_L1P_T0_35:IO_L3N_T0_35] in Figure 3-141, Figure 3-145, Figure 3-165, Figure 3-169, Figure 3-173, Figure 3-177, and Figure 3-181. Fixed the labeling for EMCCLK in Figure 3-125, Figure 3-133, Figure 3-141, Figure 3-145, Figure 3-165, Figure 3-169, Figure 3-173, Figure 3-177, and Figure 3-181. Updated the mechanical drawings for Figure 4-41 and Figure 4-44. Updated thermal resistance data in Table 5-1. Updated Chapter 6, Package Marking.

Date	Version	Revision
06/14/2011	1.2	Added Virtex-7 device information including updating Table 1-1, adding Table 1-3, Table 1-10, Table 2-4, and Table 3-4. In Table 1-12, updated Note 3, the Configuration Pins section, and the Analog to Digital Converter (XADC) Pins section. Updated Figure 3-99, Figure 3-100, Figure 3-103, Figure 3-104, Figure 3-107, Figure 3-108, Figure 3-111, Figure 3-112, Figure 3-115, Figure 3-116, Figure 3-119, and Figure 3-120. Added Figure 3-120 through Figure 3-184. Added Figure 4-37 the mechanical drawing for the Kintex-7 devices FFG1156 package. Also added some Virtex-7 device mechanical drawings in Figure 4-37 through Figure 4-44. Added thermal resistance data to Table 5-1.
04/06/2011	1.1	Removed the SBG324 package from the entire document. Added three Kintex®-7 devices: XC7K355T, XC7K420T, and XC7K480T. Updated disclaimer and copyright on page 340. Updated package size of FF1156 in Table 1-1. Updated DXP_0, DXN_0 in Table 1-12. The Table 2-3 single ASCII device files have been updated for both the XC7K70T and XC7K160T. All ASCII TXT files and the overall ZIP file have been updated on the web. Updated the XC7K70TFBG676 figures: Figure 3-101, Figure 3-102, Figure 3-103, and Figure 3-104. Added information to Chapter 4, Mechanical Drawings, Chapter 5, Thermal Specifications, and Chapter 6, Package Marking.
03/01/2011	1.0	Initial Xilinx release.

Table of Contents

Chapter 1: Packaging Overview

About this Guide **15**

Introduction **15**

Device/Package Combinations and Maximum I/Os **16**

Serial Transceiver Channels by Device/Package 18

User I/O Pins by Device/Package 21

Pin Definitions **26**

Pin Compatibility between Packages **31**

Migrating between Devices 31

Die Level Bank Numbering Overview **32**

Banking and Clocking Summary 32

XC7S6 and XC7S15 Banks 34

FTGB196 Package 34

CPGA196 Package 34

CSGA225 Package 34

XC7S25 Banks 35

FTGB196 Package 35

CSGA225 Package 35

CSGA324 Package 35

XC7S50 Banks 36

FTGB196 Package 36

CSGA324 Package 36

FGGA484 Package 36

XC7S75 and XC7S100 Banks 37

FGGA484 Package 37

FGGA676 Package 37

XA7A12T and XC7A25T Banks 38

CPG238 Package 38

CSG325 Package 38

XC7A15T, XC7A35T, XA7A15T, and XA7A35T Banks 39

CPG236 Package 39

FTG256 Package (XC7A15T and XC7A35T only) 39

CSG324 Package 39

CSG325 Package 39

FGG484 Package (XC7A15T and XC7A35T only) 39

XC7A50T, XA7A50T, and XQ7A50T Banks 40

CPG236 Package 40

FTG256 Package (XC7A50T only) 40

CSG324 Package 40

CSG325 Package 40

FGG484 Package (XC7A50T and XQ7A50T only) 40

XC7A75T and XA7A75T Banks 41

FTG256 Package (XC7A75T only) 41

CSG324 Package . . . 41
FGG484 Package . . . 41
FGG676 Package (XC7A75T only) . . . 41
XC7A100T, XQ7A100T, and XA7A100T Banks . . . 42
FTG256 Package (XC7A100T only) . . . 42
CSG324 Package . . . 42
FGG484 Package . . . 42
FGG676 Package (XC7A100T only) . . . 42
XC7A200T and XQ7A200T Banks . . . 43
SBG484, SBV484, and RS484 Packages . . . 43
FBG484, FBV484, and RB484 Packages . . . 43
FBG676, FBV676, and RB676 Packages . . . 43
FFG1156 and FFV1156 Package (XC7A200T only) . . . 43
XC7K70T Banks . . . 44
FBG484 and FBV484 Package . . . 44
FBG676 and FBV676 Package . . . 44
XC7K160T Banks . . . 45
FBG484 and FBV484 Package . . . 45
FBG676, FBV676, FFG676, and FFV676 Packages . . . 45
XC7K325T and XQ7K325T Banks . . . 46
FBG676, FBV676, FFG676, FFV676, and RF676 Packages . . . 46
FBG900, FBV900, FFG900, FFV900, and RF900 Packages . . . 46
XC7K355T Banks . . . 47
FFG901 and FFV901 Package . . . 47
XC7K410T and XQ7K410T Banks . . . 48
FBG676, FBV676, FFG676, FFV676, and RF676 Packages . . . 48
FBG900, FBV900, FFG900, FFV900, and RF900 Packages . . . 48
XC7K420T Banks . . . 49
FFG901 and FFV901 Package . . . 49
FFG1156 and FFV1156 Package . . . 49
XC7K480T Banks . . . 50
FFG901 and FFV901 Package . . . 50
FFG1156 and FFV1156 Package . . . 50
XC7V585T and XQ7V585T Banks . . . 51
FFG1157 and RF1157 Packages . . . 51
FFG1761 and RF1761 Packages . . . 51
XC7V2000T Banks . . . 52
FHG1761 Package . . . 52
FLG1925 Package . . . 52
XC7VX330T and XQ7VX330T Banks . . . 54
FFG1157, FFV1157, and RF1157 Packages . . . 54
FFG1761, FFV1761, and RF1761 Packages . . . 54
XC7VX415T Banks . . . 55
FFG1157 and FFV1157 Package . . . 55
FFG1158 and FFV1158 Package . . . 55
FFG1927 and FFV1927 Package . . . 55
XC7VX485T and XQ7VX485T Banks . . . 56
FFG1157 Package . . . 56
FFG1158 Packages . . . 56
FFG1761 and RF1761 Packages . . . 56
FFG1927 Package . . . 56
FFG1930 and RF1930 Packages . . . 56
XC7VX550T Banks . . . 58
FFG1158 Package . . . 58
FFG1927 Package . . . 58
XC7VX690T and XQ7VX690T Banks . . . 59
FFG1157 and RF1157 Packages . . . 59

FFG1158 and RF1158 Packages . . . 59
FFG1761 and RF1761 Packages . . . 59
FFG1926 Package . . . 59
FFG1927 Package . . . 59
FFG1930 and RF1930 Packages . . . 59
XC7VX980T and XQ7VX980T Banks . . . 61
FFG1926 Package . . . 61
FFG1928 Package . . . 61
FFG1930 and RF1930 Packages . . . 61
XC7VX1140T Banks . . . 63
FLG1926 Package . . . 63
FLG1928 Package . . . 63
FLG1930 Package . . . 63

Chapter 2: 7 Series FPGAs Package Files

About ASCII Package Files . . . 65
Package Specifications Designations . . . 66
ASCII Pinout Files . . . 67

Chapter 3: Device Diagrams

Summary . . . 71
Spartan-7 FPGAs Device Diagrams . . . 72
CPGA196 Package—XC7S6 and XC7S15 . . . 73
FTGB196 Package—XC7S6 and XC7S15 . . . 75
FTGB196 Package—XC7S25 and XC7S50 . . . 77
CSGA225 Package—XC7S6 and XC7S15 . . . 79
CSGA225 Package—XC7S25 . . . 81
CSGA324 Package—XC7S25 . . . 83
CSGA324 Package—XC7S50 . . . 85
FGGA484 Package—XC7S50 . . . 87
FGGA484 Package—XC7S75 and XC7S100 . . . 89
FGGA676 Package—XC7S75 and XC7S100 . . . 92
Artix-7 FPGAs Device Diagrams . . . 95
CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T . . . 96
CPG238 Package—XC7A12T and XC7A25T . . . 98
CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T . . . 100
CSG325 Package—XC7A12T . . . 102
CSG325 Package—XC7A25T . . . 104
CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T . . . 106
FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T . . . 108
FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T . . . 110
FG484 and FGG484 Packages—XC7A75T and XC7A100T . . . 113
FG676 and FGG676 Packages—XC7A75T and XC7A100T . . . 116
SB484, SBG484, SBV484, and RS484 Packages—XC7A200T . . . 119
FB484, FBG484, FBV484, and RB484 Packages—XC7A200T . . . 122
FB676, FBG676, FBV676, and RB676 Packages—XC7A200T . . . 125
FF1156, FFG1156, and FFV1156 Packages—XC7A200T . . . 128
Kintex-7 FPGAs Device Diagrams . . . 132
FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T . . . 133
FB676, FBG676, and FBV676 Packages—XC7K70T . . . 136
FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T . . . 139

FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T 142
FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T 146
FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T 150
FF901, FFG901, and FFV901 Packages—XC7K355T 154
FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T 158
FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T 162
Virtex-7 FPGAs Device Diagrams 166
FF1157, FFG1157, and RF1157 Packages—XC7V585T 167
FF1761, FFG1761, and RF1761 Packages—XC7V585T 171
FL1925 and FLG1925 Packages—XC7V2000T 175
FH1761 and FHG1761 Packages—XC7V2000T 179
FF1157, FFG1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T 183
FF1761, FFG1761, and RF1761 Packages—XC7VX330T 187
FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T 191
FF1927, FFG1927, and FFV1927 Packages—XC7VX415T 195
FF1157, FFG1157, and FFV1157 Packages—XC7VX485T 199
FF1158, FFG1158, and FFV1158 Packages—XC7VX485T 203
FF1761, FFG1761, and RF1761 Packages—XC7VX485T 207
FF1927 and FFG1927 Packages—XC7VX485T 211
FF1930, FFG1930, and RF1930 Packages—XC7VX485T 215
FF1761, FFG1761, and RF1761 Packages—XC7VX690T 219
FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T 223
FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T 227
FF1930, FFG1930, and RF1930 Packages—XC7VX690T 231
FF1928 and FFG1928 Packages—XC7VX980T 235
FF1930, FFG1930, and RF1930 Packages—XC7VX980T 239
FL1926 and FLG1926 Packages—XC7VX1140T 243
FL1928 and FLG1928 Packages—XC7VX1140T 247
FL1930 and FLG1930 Packages—XC7VX1140T 251

Chapter 4: Mechanical Drawings

Summary 255
Spartan-7 FPGAs 255
Artix-7 FPGAs 255
Kintex-7 FPGAs 256
Virtex-7 FPGAs 257
CPGA196 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.5 mm Pitch) 258
FTGB196 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (1.0 mm Pitch) 259
CSGA225 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.8 mm Pitch) 260
CSGA324 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.8 mm Pitch) 261
FGGA484 (Spartan-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch) 262
FGGA676 (Spartan-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch) 263
CP236 and CPG236 (Artix-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.5 mm Pitch) 264

CPG238 (Artix-7 FPGAs: XC7A12T and XC7A25T)
Wire-Bond Chip-Scale BGA (0.5 mm Pitch) 265
CS/CSG324 and CS/CSG325 (Artix-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.8 mm Pitch) 266
FT/FTG256 (Artix-7 FPGAs) Wire-Bond Fine-Pitch Thin BGA (1.0 mm Pitch) 267
SB484, SBG484, and SBV484 (Artix-7 FPGAs)
Flip-Chip Lidless BGA (0.8 mm Pitch) 268
FB484, FBG484, and FBV484 (Artix-7 FPGAs)
Flip-Chip Lidless BGA (1.0 mm Pitch) 269
FB676, FBG676, and FBV676 (Artix-7 FPGAs)
Flip-Chip Lidless BGA (1.0 mm Pitch) 271
FG484 and FGG484 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch) 273
FG676 and FGG676 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch) 274
FF1156, FFG1156, and FFV1156 (Artix-7 FPGAs)
Flip-Chip BGA (1.0 mm Pitch) 275
RB484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA
(1.0 mm Pitch) 276
RS484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA
(0.8 mm Pitch) 277
RB676 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA
(1.0 mm Pitch) 278
FB484, FBG484, and FBV484 (Kintex-7 FPGAs)
Flip-Chip Lidless BGA (1.0 mm Pitch) 279
FB676, FBG676, and FBV676 (Kintex-7 FPGAs)
Flip-Chip Lidless BGA (1.0 mm Pitch) 282
FB900, FBG900, and FBV900 (Kintex-7 FPGAs)
Flip-Chip Lidless BGA (1.0 mm Pitch) 287
FF676, FFG676, and FFV676 (Kintex-7 FPGAs)
Flip-Chip BGA (1.0 mm Pitch) 290
FF900 and FFG900 (XC7K325T and XC7K410T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid . 291
FF900, FFG900, FFV900, FF901, FFG901, and FFV901
(Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch) 292
FF1156 and FFG1156 (XC7K420T and XC7K480T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid . . . 293
FF1156, FFG1156, and FFV1156 (Kintex-7 FPGAs)
Flip-Chip BGA (1.0 mm Pitch) 294
RF676 (Kintex-7 FPGAs) Flip-Chip BGA
(1.0 mm Pitch) 295
RF900 (Kintex-7 FPGAs) Flip-Chip BGA
(1.0 mm Pitch) 296
FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs)
Flip-Chip BGA (1.0 mm Pitch) 297
FF1761 and FFG1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch) 298

FFV1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch) 299
FH1761 and FHG1761 (Virtex-7 T FPGAs) Flip-Chip BGA (1.0 mm Pitch) 300
FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 (Virtex-7 XT FPGAs) Flip-Chip BGA (1.0 mm Pitch) 301
FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch) 302
RF1157 and RF1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch) 303
RF1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch) 304
RF1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch) 305

Chapter 5: Thermal Specifications

Introduction 306
Thermal Resistance Data 306
Support for Thermal Models 312
Thermal Management Strategy 313
Cavity-Up Plastic BGA Packages 313
Wire-Bond Packages 313
Flip-Chip Packages 314
System Level Heat Sink Solutions 315
Thermal Interface Material 315
Types of TIM 316
Guidelines for Thermal Interface Materials 316
Thermal Conductivity of the Material 316
Electrical Conductivity of the Material 317
Spreading Characteristics of the Material 317
Long-Term Stability and Reliability of the Material 317
Ease of Application 317
Applied Pressure from Heat Sink to the Package via Thermal Interface Materials 317
Heat Sink Removal Procedure 318
Soldering Guidelines 319
Sn/Pb Reflow Soldering 320
Pb-Free Reflow Soldering 320
Post Reflow/Cleaning/Washing 324
Conformal Coating 324

Chapter 6: Package Marking

Introduction 325

Chapter 7: Packing and Shipping

Introduction 329

Appendix A: Recommended PCB Design Rules for BGA Packages

BGA Packages **331**

Appendix B: Heat Sink Guidelines for Lidless Flip-Chip Packages

Heat Sink Attachments for Lidless Flip-chip BGA (FB/FBG/FBV and SB/SBG/SBV) **333**
Silicon and Decoupling Capacitors Height Consideration 333
Types of Heat Sink Attachments **334**
Heat Sink Attachment 335
Component Pick-up Tool Consideration 335
Heat Sink Attachment Process Considerations 336

Appendix C: Additional Resources and Legal Notices

Xilinx Resources **339**
Solution Centers **339**
References **339**
Please Read: Important Legal Notices **340**

Packaging Overview

About this Guide

Xilinx® 7 series FPGAs include four FPGA families that are all designed for lowest power to enable a common design to scale across families for optimal power, performance, and cost. The Spartan®-7 family is the lowest density with the lowest cost entry point into the 7 series portfolio. The Artix®-7 family is optimized for highest performance-per-watt and bandwidth-per-watt for cost-sensitive, high-volume applications. The Kintex®-7 family is an innovative class of FPGAs optimized for the best price-performance. The Virtex®-7 family is optimized for highest system performance and capacity.

This 7 series packaging and pinout product specification, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/documentation.

Introduction

This section describes the pinouts for the 7 series FPGAs in various fine pitch and flip-chip 1.0 mm pitch BGA packages, 0.8 mm and 0.5 mm pitch chip-scale packages, and 0.5 mm pitch wire-bond lead frame packages.

Spartan-7, Artix-7, and Kintex-7 devices are offered in low-cost, space-saving packages that are optimally designed for the maximum number of user I/Os.

Virtex-7 T and Virtex-7 XT devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter.

For pinout and packaging information on the Virtex-7 HT devices, see www.xilinx.com/member/gtz/index.htm.

Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

The FFG, FLG, FHG, FBG, SBG, and RFG flip-chip packages are RoHS 6 of 6 compliant, with exemption 15 where there is lead in the C4 bumps that are used to complete a viable electrical connection between the semiconductor die and the package substrate. The FFV,

FBV, and SBV flip-chip packages marked with the Pb-free Character are RoHS 6 of 6 compliant (without the use of exemption 15). The CPG, CSG, FTG, and FGG non-flip chip packages are RoHS 6 of 6 compliant.

All of the 7 series devices supported in a particular package are pinout compatible. See Pin Compatibility between Packages, page 31. Pins that are available in a device but are not available in a smaller device with a compatible package are listed as *No Connects*.

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see the *7 Series FPGAs SelectIO Resources User Guide* (UG471). Table 1-12 provides definitions for all pin types.

7 series device's flip-chip assembly materials are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm^2 or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in the 7 series FPGAs BGA packages.

Table 1-1: **7 Series FPGAs Package Specifications**

Packages[1]	Description	Package Specifications			
		Package Type	Pitch (mm)	Size (mm)	Maximum I/Os[2]
CPGA196	Wire-bond chip-scale	BGA	0.5	8 x 8	100
FTB196/FTGB196		BGA	1.0	15 x 15	100
CP236/CPG236		BGA	0.5	10 x 10	106
CPG238		BGA	0.5	10 x 10	110
CSA225/CSGA225		BGA	0.8	13 x 13	100
CS324/CSG324		BGA	0.8	15 x 15	210
CSGA324		BGA	0.8	15 x 15	210
CS325/CSG325		BGA	0.8	15 x 15	150
FT256/FTG256	Wire-bond fine-pitch	BGA	1.0	17 x 17	170
FG484/FGG484		BGA	1.0	23 x 23	285
FGGA484		BGA	1.0	23 x 23	338
FG676/FGG676		BGA	1.0	27 x 27	300
FGGA676		BGA	1.0	27 x 27	400

Table 1-1: **7 Series FPGAs Package Specifications *(Cont'd)***

Packages[1]	Description	Package Specifications			
		Package Type	Pitch (mm)	Size (mm)	Maximum I/Os[2]
SB484/SBG484/SBV484	Flip-chip lidless	BGA	0.8	19 x 19	285
FB484/FBG484/FBV484		BGA	1.0	23 x 23	285
RS484	Ruggedized flip-chip	BGA	0.8	19 x 19	285
RB484		BGA	1.0	23 x 23	285
FB676/FBG676/FBV676	Flip-chip lidless	BGA	1.0	27 x 27	400
RB676	Ruggedized flip-chip	BGA	1.0	27 x 27	400
RF676	Ruggedized flip-chip fine-pitch	BGA	1.0	27 x 27	400
FB900/FBG900/FBV900	Flip-chip lidless	BGA	1.0	31 x 31	500
RF900	Ruggedized flip-chip fine-pitch	BGA	1.0	31 x 31	500
FF676/FFG676/FFV676	Flip-chip fine-pitch	BGA	1.0	27 x 27	400
FF900/FFG900/FFV900		BGA	1.0	31 x 31	500
FF901/FFG901/FFV901		BGA	1.0	31 x 31	380
FF1156/FFG1156/FFV1156		BGA	1.0	35 x 35	600
FF1157/FFG1157/FFV1157		BGA	1.0	35 x 35	600
FF1158/FFG1158/FFV1158		BGA	1.0	35 x 35	350
FF1761/FFG1761/FFV1761		BGA	1.0	42.5 x 42.5	850
FF1926/FFG1926		BGA	1.0	45 x 45	720
FF1927/FFG1927/FFV1927		BGA	1.0	45 x 45	600
FF1928/FFG1928		BGA	1.0	45 x 45	480
FF1930/FFG1930		BGA	1.0	45 x 45	1000
FL1925/FLG1925	SSI flip-chip fine-pitch	BGA	1.0	45 x 45	1200
FL1926/FLG1926		BGA	1.0	45 x 45	720
FL1928/FLG1928		BGA	1.0	45 x 45	480
FL1930/FLG1930		BGA	1.0	45 x 45	1100
FH1761/FHG1761	SSI flip-chip fine-pitch (overhang)	BGA	1.0	45 x 45	850
RF1157	Ruggedized flip-chip fine-pitch	BGA	1.0	35 x 35	600
RF1158		BGA	1.0	35 x 35	600
RF1761		BGA	1.0	42.5 x 42.5	850
RF1930		BGA	1.0	45 x 45	1000

Notes:

1. Leaded package options are available upon request for all packages listed in this table.
2. The maximum I/O numbers do not include pins in the configuration Bank 0 (Table 1-2) or the GT serial transceivers.

Table 1-2 lists the 21 dedicated I/O pins.

Table 1-2: **7 Series FPGAs I/O Pins in the Dedicated Configuration Bank (Bank0)**

DXP_0	VCCBATT_0	INIT_B_0	M0_0	TDO_0	TDI_0	GNDADC_0(1)
DXN_0	DONE_0	VN_0	M1_0	TCK_0	VREFN_0	VCCADC_0(1)
PROGRAM_B_0	CCLK_0	VP_0	M2_0	TMS_0	VREFP_0	CFGBVS_0

Notes:
1. In SSI technology devices, GNDADC and VCCADC do not have an _0 in the pin name.

Serial Transceiver Channels by Device/Package

Spartan-7 FPGAs do not contain serial transceivers. Table 1-3 lists the quantity of GTP serial transceiver channels for the Artix-7 FPGAs.

Table 1-3: **Serial Transceiver Channels (GTPs) by Device/Package (Artix-7 FPGAs)**

Device	GTP Channels by Package													
	CPG 236	CPG 238	CSG 324	CSG 325	FTG 256	SBG SBV 484	FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RS 484	RB 484	RB 676
XA7A12T	–	2	–	2	–	–	–	–	–	–	–	–	–	–
XC7A15T	2		0	4	0	–	4	–	–	–	–	–	–	–
XC7A25T	–	2	–	4		–	–	–	–	–	–	–	–	–
XC7A35T	2	–	0	4	0	–	4	–	–	–	–	–	–	–
XC7A50T	2	–	0	4	0	–	4	–	–	–	–	–	–	–
XC7A75T	–	–	0	–	0	–	4	8	–	–	–	–	–	–
XC7A100T	–	–	0	–	0	–	4	8	–	–	–	–	–	–
XC7A200T	–	–	–	–	–	4	–	–	4	8	16	–	–	–
XA7A12T	–	2	–	2	–	–	–	–	–	–	–	–	–	–
XA7A15T	2	–	0	4	0	–	4	–	–	–	–	–	–	–
XA7A25T	–	2	–	4		–	–	–	–	–	–	–	–	–
XA7A35T	2	–	0	4	–	–	–	–	–	–	–	–	–	–
XA7A50T	2	–	0	4	–	–	–	–	–	–	–	–	–	–
XA7A75T	–	–	0	–	–	–	4	–	–	–	–	–	–	–
XA7A100T	–	–	0	–	–	–	4	–	–	–	–	–	–	–
XQ7A50T	–	–	–	4	–	–	4	–	–	–	–	–	–	–
XQ7A100T	–	–	0	–	–	–	4	–	–	–	–	–	–	–
XQ7A200T	–	–	–	–	–	–	–	–	–	–	–	4	4	8

Table 1-4 lists the quantity of GTX serial transceiver channels for the Kintex-7 FPGAs.

Table 1-4: **Serial Transceiver Channels (GTXs) by Device/Package (Kintex-7 FPGAs)**

Device	GTX Channels by Package								
	FBG484 FBV484	FBG676 FBV676	FBG900 FBV900	FFG676 FFV676	FFG900 FFV900	FFG901 FFV901	FFG1156 FFV1156	RF676	RF900
XC7K70T	4	8	–	–	–	–	–	–	–
XC7K160T	4	8	–	8	–	–	–	–	–
XC7K325T	–	8	16	8	16	–	–	–	–
XC7K355T	–	–	–	–	–	24	–	–	–
XC7K410T	–	8	16	8	16	–	–	–	–
XC7K420T	–	–	–	–	–	28	32	–	–
XC7K480T	–	–	–	–	–	28	32	–	–
XQ7K325T	–	–	–	–	–	–	–	8	16
XQ7K410T	–	–	–	–	–	–	–	8	16

Table 1-5 lists the quantity of GTX serial transceiver channels for the Virtex-7 T FPGAs.

Table 1-5: **Serial Transceiver Channels (GTX) by Device/Package (Virtex-7 T FPGAs)**

Device	FFG1157	FFG1761	FLG1925	FHG1761	RF1157	RF1761
XC7V585T	20	36	–	–	–	–
XC7V2000T	–	–	16	36	–	–
XQ7V585T	–	–	–	–	20	36

Table 1-6 lists the quantity of GTX and GTH serial transceiver channels for the Virtex-7 XT FPGAs. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-6: **Serial Transceiver Channels (GTX/GTH) by Device/Package (Virtex-7 XT FPGAs)**

Device	FFG1157 FFV1157 RF1157		FFG1158 FFV1158 RF1158		FFG1761 FFV1761 RF1761		FFG1926		FFG1927 FFV1927		FFG1928		FFG1930 RF1930		FLG1926		FLG1928		FLG1930	
	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH	GTX	GTH
XC7VX330T	0	20	–		0	28	–		–		–		–		–		–		–	
XC7VX415T	0	20	0	48	–		–		0	48	–		–		–		–		–	
XC7VX485T	20	0	48	0	28	0	–		56	0	–		24	0	–		–		–	
XC7VX550T	–		0	48	–		–		0	80	–		–		–		–		–	
XC7VX690T	0	20	0	48	0	36	0	64	0	80	–		0	24	–		–		–	
XC7VX980T	–		–		–		0	64	–		0	72	0	24	–		–		–	
XC7VX1140T	–		–		–		–		–		–		–		0	64	0	96	0	24
XQ7VX330T	0	20	–		0	28	–		–		–		–		–		–		–	
XQ7VX485T	–		–		28	0	–		–		–		24	0	–		–		–	
XQ7VX690T	0	20	0	48	0	36	–		–		–		0	24	–		–		–	
XQ7VX980T	–		–		–		–		–		–		0	24	–		–		–	

User I/O Pins by Device/Package

IMPORTANT: *Because of package inductance, each device/package supports a limited number of simultaneous switching outputs. Limitations for specific applications can be determined using the Vivado Design Suite report_ssn tool. See the Simultaneous Switching Outputs section of the 7 Series FPGAs SelectIO Resources User Guide (UG471) for more information.*

Table 1-7 shows the number of available I/Os and the number of differential I/Os for each Spartan-7 device/package combination.

Table 1-7: **Available I/O Pin/Device/Package Combinations for Spartan-7 FPGAs**

Spartan-7 Devices	User I/O Pins	Spartan-7 FPGA Packages: HR I/O Banks Only					
		CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
XC7S6	User I/O	100	100	–	100	–	–
	Differential	96	96	–	96	–	–
XC7S15	User I/O	100	100	–	100	–	–
	Differential	96	96	–	96	–	–
XC7S25	User I/O	–	150	150	100	–	–
	Differential	–	144	144	96	–	–
XC7S50	User I/O	–	–	210	100	250	–
	Differential	–	–	202	96	240	–
XC7S75	User I/O	–	–	–	–	338	400
	Differential	–	–	–	–	324	384
XC7S100	User I/O	–	–	–	–	338	400
	Differential	–	–	–	–	324	384

Table 1-8 shows the number of available I/Os and the number of differential I/Os for each Artix-7 device/package combination.

Table 1-8: **Available I/O Pin/Device/Package Combinations for Artix-7 FPGAs**

Artix-7 Devices	User I/O Pins	Artix-7 FPGA Packages: HR I/O Banks Only												
		CPG 236	CPG 238	CSG 324	CSG 325	FTG 256	SBG SBV 484	FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RB484 RS484	RB676
XC7A12T	User I/O	–	110	–	150	–	–	–	–	–	–	–	–	–
	Differential	–	108	–	144	–	–	–	–	–	–	–	–	–
XC7A15T	User I/O	106		210	150	170	–	250	–	–	–	–	–	–
	Differential	104		202	144	162	–	240	–	–	–	–	–	–
XC7A25T	User I/O	–	110	–	150	–	–	–	–	–	–	–	–	–
	Differential	–	108	–	144	–	–	–	–	–	–	–	–	–
XC7A35T	User I/O	106	–	210	150	170	–	250	–	–	–	–	–	–
	Differential	104	–	202	144	162	–	240	–	–	–	–	–	–
XC7A50T	User I/O	106	–	210	150	170	–	250	–	–	–	–	–	–
	Differential	104	–	202	144	162	–	240	–	–	–	–	–	–
XC7A75T	User I/O	–	–	210	–	170	–	285	300	–	–	–	–	–
	Differential	–	–	202	–	162	–	274	288	–	–	–	–	–
XC7A100T	User I/O	–	–	210	–	170	–	285	300	–	–	–	–	–
	Differential	–	–	202	–	162	–	274	288	–	–	–	–	–
XC7A200T	User I/O	–	–	–	–	–	285	–	–	285	400	500	–	–
	Differential	–	–	–	–	–	274	–	–	274	384	480	–	–
XA7A12T	User I/O	–	110	–	150	–	–	–	–	–	–	–	–	–
	Differential	–	108	–	144	–	–	–	–	–	–	–	–	–
XA7A15T	User I/O	106	–	210	150	–	–	–	–	–	–	–	–	–
	Differential	104	–	202	144	–	–	–	–	–	–	–	–	–
XA7A25T	User I/O	–	110	–	150	–	–	–	–	–	–	–	–	–
	Differential	–	108	–	144	–	–	–	–	–	–	–	–	–
XA7A35T	User I/O	106	–	210	150	–	–	–	–	–	–	–	–	–
	Differential	104	–	202	144	–	–	–	–	–	–	–	–	–
XA7A50T	User I/O	106	–	210	150	–	–	–	–	–	–	–	–	–
	Differential	104	–	202	144	–	–	–	–	–	–	–	–	–
XA7A75T	User I/O	–	–	210	–	–	–	285	–	–	–	–	–	–
	Differential	–	–	202	–	–	–	274	–	–	–	–	–	–
XA7A100T	User I/O	–	–	210	–	–	–	285	–	–	–	–	–	–
	Differential	–	–	202	–	–	–	274	–	–	–	–	–	–

Table 1-8: **Available I/O Pin/Device/Package Combinations for Artix-7 FPGAs *(Cont'd)***

Artix-7 Devices	User I/O Pins	Artix-7 FPGA Packages: HR I/O Banks Only												
		CPG 236	CPG 238	CSG 324	CSG 325	FTG 256	SBG SBV 484	FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RB484 RS484	RB676
XQ7A50T	User I/O	–	–	–	150	–	–	250	–	–	–	–	–	–
	Differential	–	–	–	144	–	–	240	–	–	–	–	–	–
XQ7A100T	User I/O	–	–	210	–	–	–	285	–	–	–	–	–	–
	Differential	–	–	202	–	–	–	274	–	–	–	–	–	–
XQ7A200T	User I/O	–	–	–	–	–	–	–	–	–	–	–	285	400
	Differential	–	–	–	–	–	–	–	–	–	–	–	274	384

Table 1-9 shows the number of available I/Os and the number of differential I/Os for each Kintex-7 device/package combination.

Table 1-9: **Available I/O Pin/Device/Package Combinations for Kintex-7 FPGAs**

Kintex-7 Devices	User I/O Pins	Kintex-7 FPGA Packages: HR and HP I/O Banks																	
		FBG484 FBV484		FBG676 FBV676		FBG900 FBV900		FFG676 FFV676		FFG900 FFV900		FFG901 FFV901		FFG1156 FFV1156		RF676		RF900	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7K70T	User I/O	100	185	100	200	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	Differential	96	176	96	192	–	–	–	–	–	–	–	–	–	–	–	–	–	–
XC7K160T	User I/O	100	185	150	250	–	–	150	250	–	–	–	–	–	–	–	–	–	–
	Differential	96	176	144	240	–	–	144	240	–	–	–	–	–	–	–	–	–	–
XC7K325T	User I/O	–	–	150	250	150	350	150	250	150	350	–	–	–	–	–	–	–	–
	Differential	–	–	144	240	144	336	144	240	144	336	–	–	–	–	–	–	–	–
XC7K355T	User I/O	–	–	–	–	–	–	–	–	–	–	0	300	–	–	–	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	0	288	–	–	–	–	–	–
XC7K410T	User I/O	–	–	150	250	150	350	150	250	150	350	–	–	–	–	–	–	–	–
	Differential	–	–	144	240	144	336	144	240	144	336	–	–	–	–	–	–	–	–
XC7K420T	User I/O	–	–	–	–	–	–	–	–	–	–	0	380	0	400	–	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	0	366	0	384	–	–	–	–
XC7K480T	User I/O	–	–	–	–	–	–	–	–	–	–	0	380	0	400	–	–	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	0	366	0	384	–	–	–	–
XQ7K325T	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	150	250	150	350
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	144	240	144	336
XQ7K410T	User I/O	–	–	–	–	–	–	–	–	–	–	–	–	–	–	150	250	150	350
	Differential	–	–	–	–	–	–	–	–	–	–	–	–	–	–	144	240	144	336

Table 1-10 and Table 1-11 show the number of available I/Os and the number of differential I/Os for each Virtex-7 device/package combination. When applicable, it also lists the number of user I/Os in the 3.3V-capable high-range (HR) banks and the number of 1.8V-capable high-performance (HP) banks.

Table 1-10: **Available I/O Pin/Device/Package Combinations for Virtex-7 T FPGAs**

Virtex-7 T Devices	User I/O Pins	Virtex-7 T FPGA Packages: HR and HP I/O Banks											
		FFG1157		FFG1761		FLG1925		FHG1761		RF1157		RF1761	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7V585T	User I/O	600	0	750	100	–		–		–		–	
	Differential	576	0	720	96	–		–		–		–	
XC7V2000T	User I/O	–		–		1200	0	850	0	–		–	
	Differential	–		–		1152	0	816	0	–		–	
XQ7V585T	User I/O	–		–		–		–		600	0	750	100
	Differential	–		–		–		–		576	0	720	96

Table 1-11: **Available I/O Pin/Device/Package Combinations for Virtex-7 XT FPGAs**

Virtex-7 XT Devices	User I/O Pins	Virtex-7 XT FPGA Packages: HR and HP I/O Banks																			
		FFG1157 FFV1157 RF1157		FFG1158 FFV1158 RF1158		FFG1761 FFV1761 RF1761		FFG 1926		FFG1927 FFV1927		FFG 1928		FFG1930 RF1930		FLG 1926		FLG 1928		FLG 1930	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7VX330T	User I/O	600	0	–		650	50	–		–		–		–		–		–		–	
	Differential	576	0	–		624	48	–		–		–		–		–		–		–	
XC7VX415T	User I/O	600	0	350	0	–		–		600	0	–		–		–		–		–	
	Differential	576	0	336	0	–		–		576	0	–		–		–		–		–	
XC7VX485T	User I/O	600	0	350	0	700	0	–		600	0	–		700	0	–		–		–	
	Differential	576	0	336	0	672	0	–		576	0	–		672	0	–		–		–	
XC7VX550T	User I/O	–		350	0	–		–		600	0	–		–		–		–		–	
	Differential	–		336	0	–		–		576	0	–		–		–		–		–	
XC7VX690T	User I/O	600	0	350	0	850	0	720	0	600	0	–		1000	0	–		–		–	
	Differential	576	0	336	0	816	0	690	0	576	0	–		960	0	–		–		–	
XC7VX980T	User I/O	–		–		–		720	0	–		480	0	900	0	–		–		–	
	Differential	–		–		–		690	0	–		460	0	864	0	–		–		–	
XC7VX1140T	User I/O	–		–		–		–		–		–		–		720	0	480	0	1100	0
	Differential	–		–		–		–		–		–		–		690	0	460	0	1056	0
XQ7VX330T	User I/O	600	0	–		650	50	–		–		–		–		–		–		–	
	Differential	576	0	–		624	48	–		–		–		–		–		–		–	
XQ7VX485T	User I/O	–		–		700	0	–		–		–		700	0	–		–		–	
	Differential	–		–		672	0	–		–		–		672	0	–		–		–	
XQ7VX690T	User I/O	600	0	350	0	850	0	–		–		–		1000	0	–		–		–	
	Differential	576	0	336	0	816	0	–		–		–		960	0	–		–		–	
XQ7VX980T	User I/O	–		–		–		–		–		–		900	0	–		–		–	
	Differential	–		–		–		–		–		–		864	0	–		–		–	

Pin Definitions

Table 1-12 lists the pin definitions used in 7 series FPGAs packages.

Note: There are dedicated general purpose user I/O pins listed separately in Table 1-12. There are also multi-function pins where the pin names start with either IO_LXXY_ZZZ_# or IO_XX_ZZZ_#, where ZZZ represents one or more functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.

Table 1-12: **7 Series FPGAs Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_LXXY_# IO_XX_#	Dedicated	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. The top and bottom I/O pins are always single ended. Each user I/O is labeled IO_LXXY_#, where: ◦ IO indicates a user I/O pin. ◦ L indicates a differential pair, with XX a unique pair in the bank and Y = [P|N] for the positive/negative sides of the differential pair. ◦ # indicates a bank number.
Configuration Pins			
For more information, see the *Configuration Pin Definitions* table in UG470, *7 Series FPGAs Configuration User Guide*.			
CCLK_0	Dedicated(1)	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
DONE_0	Dedicated(1)	Bidirectional	DONE indicates successful completion of configuration (active High).
INIT_B_0	Dedicated(1)	Bidirectional (open-drain)	Indicates initialization of configuration memory (active Low).
M0_0, M1_0, or M2_0	Dedicated(1)	Input	Configuration mode selection.
PROGRAM_B_0	Dedicated(1)	Input	Asynchronous reset to configuration logic (active Low).
TCK_0	Dedicated(1)	Input	JTAG clock.
TDI_0	Dedicated(1)	Input	JTAG data input.
TDO_0	Dedicated(1)	Output	JTAG data output.
TMS_0	Dedicated(1)	Input	JTAG mode select.

Table 1-12: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
CFGBVS_0	Dedicated(1)	Input	This pin selects the preconfiguration I/O standard type for the dedicated and multi-function configuration banks 0, 14, and 15. If the V_{CCO} for banks 0, 14, or 15 is 2.5V or 3.3V, then this pin must be connected to V_{CCO_0}. If the V_{CCO} for banks 0, 14, and 15 are less than or equal to 1.8V, then this pin should be connected to GND. ***Note:*** To avoid device damage, this pin must be connected correctly. See the *Configuration Banks Voltage Select* section in UG470, *7 Series FPGAs Configuration User Guide* for more information.
D00 through D31	Multi-function	Bidirectional	Configuration data pins.
ADV_B	Multi-function	Output	BPI Flash address valid output (active Low).
A00 through A28	Multi-function	Output	Address A00–A28 BPI address output.
RS0 or RS1	Multi-function	Output	RS0 and RS1 revision select output.
FCS_B	Multi-function	Output	BPI and SPI flash chip select (active Low).
FOE_B	Multi-function	Output	BPI flash output enable (active Low).
MOSI	Multi-function	Output	SPI flash command output. Also known as the SPI bus master output, slave input signal.
FWE_B	Multi-function	Output	BPI flash write enable (active Low).
DOUT	Multi-function	Output	Data output for serial daisy-chain configuration.
CSO_B	Multi-function	Output	Chip-select output for parallel daisy-chain (active Low).
CSI_B	Multi-function	Input	SelectMAP chip-select input (active Low).
PUDC_B	Multi-function	Input	Pull-Up During Configuration (bar) PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration (active Low). ◦ When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. ◦ When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. PUDC_B must be tied either directly (or through a 1KΩ or less resistor) to V_{CCO_14} or GND. Do not allow this pin to float before and during configuration.
RDWR_B	Multi-function	Input	SelectMAP data bus direction control signal for reading (active High) or writing (active Low) configuration data.
EMCCLK	Multi-function	Input	External master configuration clock.

Table 1-12: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
Power/Ground Pins			
GND	Dedicated	N/A	Ground.
VCCAUX	Dedicated	N/A	1.8V power-supply pins for auxiliary circuits.
VCCAUX_IO_G#[(2)]	Dedicated	N/A	1.8V/2.0V power-supply pins for auxiliary I/O circuits.
VCCINT	Dedicated	N/A	0.9V/1.0V power-supply pins for the internal core logic.
VCCO_#[(3)]	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VCCBRAM	Dedicated	N/A	1.0V power-supply pins for the FPGA logic block RAM.
VCCBATT_0	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used[(4)]. Specific Spartan-7 devices (XC7S6 and XC7S15) do not support AES encryption. In these devices, connect VCCBATT_0 to VCCAUX or GND.
VREF	Multi-function	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Analog to Digital Converter (XADC) Pins			
For more information, see the *XADC Package Pins* table in UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide*.			
VCCADC_0[(5)(6)]	Dedicated	N/A	XADC analog positive supply voltage. The XC7S6 and XC7S15 Spartan-7 devices do not support the XADC. In these devices, connect the VCCADC_0 pin to VCCAUX.
GNDADC_0[(5)(6)]	Dedicated	N/A	XADC analog ground reference. The XC7S6 and XC7S15 Spartan-7 devices do not support the XADC. In these devices, connect the GNDADC_0 pin to GND.
VP_0[(5)]	Dedicated	Input	XADC dedicated differential analog input (positive side).
VN_0[(5)]	Dedicated	Input	XADC dedicated differential analog input (negative side).
VREFP_0[(5)]	Dedicated	N/A	1.25V reference input.
VREFN_ 0[(5)]	Dedicated	N/A	1.25V reference GND reference.
AD0P through AD15P AD0N through AD15N	Multi-function	Input	XADC (analog-to-digital converter) differential auxiliary analog inputs 0–15. Auxiliary channels 6, 7, 13, 14, and 15 are not supported on Kintex-7 devices.
Multi-gigabit Serial Transceiver Pins (GTPE2, GTXE2, and GTHE2)			
For more information on the GTPE2 pins see the *Pin Description and Design Guidelines* section in UG482, *7 Series FPGAs GTP Transceivers User Guide*. For more information on the on the GTXE2 and GTHE2 pins see the *Pin Description and Design Guidelines* section in UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*.			
MGTPRXP[0:3]	Dedicated	Input	Positive differential receive port GTP Quad.
MGTPRXN[0:3]	Dedicated	Input	Negative differential receive port GTP Quad.

Table 1-12: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
MGTPTXP[0:3]	Dedicated	Output	Positive differential transmit port GTP Quad.
MGTPTXN[0:3]	Dedicated	Output	Negative differential transmit port GTP Quad.
MGTXRXP[0:3]	Dedicated	Input	Positive differential receive port GTX Quad.
MGTXRXN[0:3]	Dedicated	Input	Negative differential receive port GTX Quad.
MGTXTXP[0:3]	Dedicated	Output	Positive differential transmit port GTX Quad.
MGTXTXN[0:3]	Dedicated	Output	Negative differential transmit port GTX Quad.
MGTHRXP[0:3]	Dedicated	Input	Positive differential receive port GTH Quad.
MGTHRXN[0:3]	Dedicated	Input	Negative differential receive port GTH Quad.
MGTHTXP[0:3]	Dedicated	Output	Positive differential transmit port GTH Quad.
MGTHTXN[0:3]	Dedicated	Output	Negative differential transmit port GTH Quad.
MGTAVCC_G#(7)	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_G#(7)	Dedicated	Input	1.2V analog power-supply pin for the transmit driver.
MGTVCCAUX_G#(7)	Dedicated	Input	1.8V auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.
MGTREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTAVTTRCAL	Dedicated	N/A	Precision reference resistor pin for internal calibration termination. Not used for Artix-7 devices.
MGTRREF	Dedicated	Input	Precision reference resistor pin for internal calibration termination.
Other Pins			
MRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. In addition, these pins can drive the BUFMR for multi-region BUFIO and BUFR support. These pins become regular user I/Os when not needed as a clock. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins, when used as single region resource, can drive four BUFIOs and four BUFR in a single bank.
SRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. These pins become regular user I/Os when not needed for clocks. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single region) pins can drive four BUFIOs and four BUFRs in a single bank.
VRN(8)	Multi-function	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).

Table 1-12: **7 Series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
VRP[8]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
DXP_0, DXN_0	Dedicated	N/A	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines. The recommended temperature monitoring solution for 7 series FPGAs uses the temperature sensor in the XADC block.
T0, T1, T2, or T3	Multi-function	N/A	This pin belongs to the memory byte group 0-3.
T0_DQS, T1_DQS, T2_DQS, or T3_DQS	Multi-function	Bidirectional	The DDR DQS strobe pin that belongs to the memory byte group T0–T3.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCO_0}.
2. For devices that do not include VCCAUX_IO_G# pins, auxiliary I/O circuits are powered by VCCAUX pins. As indicated in Chapter 2, 7 Series FPGAs Package Files, some packages include VCCAUX_IO_G# pins but also have auxiliary I/O circuits powered by VCCAUX pins. In this case, the VCCAUX_IO_G# pins exist for migration purposes only and will not connect to any internal circuitry. When planning to migrate to a device that utilizes VCCAUX_IO_G#, these pins must be connected to the desired voltage (1.8V/2.0V). Otherwise, they can be tied to V_{CCAUX} or left unconnected.
3. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or ground).
4. Refer to the data sheet for V_{CCBATT_0} specifications.
5. See UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* for the default connections required to support on-chip monitoring.
6. In SSI technology devices, GNDADC and VCCADC do not have an _0 in the pin name.
7. In packages with only one MGT power group, the MGTAVCC_G#, MGTAVTT_G#, and MGTVCCAUX_G# pins are labeled without the _G#. These pins also appear without a number in the power and GND placement diagrams in Chapter 3, Device Diagrams.
8. The DCI guidelines in the 7 series FPGAs are different from previous Virtex device DCI guidelines. See the DCI sections in UG471, *7 Series FPGAs SelectIO Resources User Guide* for more information on the VRN/VRP pins.

Pin Compatibility between Packages

7 series FPGA devices are pin compatible only with other 7 series FPGA devices of the same family (Spartan-7, Artix-7, Kintex-7, and Virtex-7) in the same package. In addition, FB/FBG/FBV, FF/FFG/FFV, FH/FHG, FL/FLG, RB, RF, and RS packages of the same pin-count designator are pin compatible. Also, in Artix-7 devices the FGG and FBG packages are pin compatible.

Note: Pin compatible packages can have substantially different decoupling capacitor recommendations.

Some FB/FBG and RB packages include V_{CCAUX_IO} pins that are not utilized by the I/O. These pins are placeholders to ensure pin compatibility with FF/FFG/FFV and RF packages. In the FF/FFG/FFV and RF packages, when the high-performance option is chosen for the HP I/O banks, the V_{CCAUX_IO} pins must be connected to a separate power supply from V_{CCAUX}. Therefore, to allow for migration to the FF/FFG/FFV and RF packages, V_{CCAUX_IO} must be connected to the appropriate voltage/regulator.

Migrating between Devices

When migrating between devices using the same package, any differences between the devices must be taken into consideration. Examples include the following.

- Package pins that are routed from a specific bank in one device can be routed from a different bank in another device. Migration between the two devices can be affected when interfaces span multiple banks.
- Package pins routed to pins of a certain pin type in one device can be routed to a different pin type in another device. Migration differences can include clock-capable pins or differential signal capable pins in the first device with non-clock capable pins or single-ended pins in the second device.
- Package pins routed from a single bank on one device can be routed from multiple banks on another device. To prevent multiple voltage levels between the devices, the V_{CCO} voltage level of the multiple banks on the second device must be the same as the voltage level of the single bank on the first device.
- The auxiliary analog input pins AD[15:00] for the XADC in some devices are not always routed to the same pins in other devices. Each device can have available a different number of auxiliary analog input pins. Prior to designing with XADCs, the compatibility between pins in each device should be thoroughly analyzed.

Die Level Bank Numbering Overview

Banking and Clocking Summary

- The center clocking backbone contains all vertical clock tracks and clock buffer connectivity.
- The CMT backbone contains all vertical CMT connectivity and is located in the CMT column.
- Not all banks are bonded out in every part/package combination.
- GTP/GTX/GTH columns summary
  - One GT Quad = Four transceivers = Four GTPE2 or GTXE2 or GTHE2 primitives.
  - Not all GT Quads are bonded out in every package.
- I/O banks summary
  - Each bank has four pairs of clock capable (CC) inputs for four differential or four single ended clock inputs.
    - Can connect to the CMT in the same region and the region above and below (with restrictions).
    - Two MRCC pairs can connect to the BUFRs and BUFIOs in the same region/banks and the regions/banks above and below.
    - Two SRCC pairs can only connect to the BUFRs and BUFIOs in the same region/bank.
    - There are no global clock pins (GC pins) in the 7 series FPGAs.
  - Each user I/O bank has 50 single-ended I/Os or 24 differential pairs (48 differential I/Os). The top and bottom I/O pin are always single ended. All 50 pads of a bank are not always bonded out to pins.
- Bank locations of dedicated and dual-purpose pins
  - In most devices, banks 14 and 15 always contain the dual-purpose configuration pins. Bank 15 and 35 contains the XADC auxiliary inputs; however, in Kintex-7 devices, the auxiliary inputs are only in bank 15. Bank 0 contains the dedicated configuration pins.
  - All dedicated configuration I/Os (bank 0) are 3.3V capable.
  - The multi-function configuration banks 14 and 15 are restricted during configuration. The SSI technology devices (XC7VX1140T and XC7V2000T) pins in banks 11, 12, 17, 18, 20, and 21 are restricted, similar to multi-function pins. Pins in these banks do not have configuration functions. Because there are architectural differences between these and other banks, special consideration must be taken. For more information, see the *State of I/Os During and After Configuration* and the

Special DCI Requirements for Some Banks sections of UG471, *7 Series FPGAs SelectIO Resources User Guide*.

- The physical XY locations for each IDELAYCTRL start at X0Y0 in the bottom left-most bank. The locations then increment by one starting with the lowest bank number in each column in the vertical Y direction and by one for each column in the horizontal X direction. IDELAYCTRLs are located in each of the HROWs.

This section visually describes the die level bank numbering.

- Spartan-7 devices on page 34 through page 37.
- Artix-7 devices on page 38 through page 43.
- Kintex-7 devices on page 44 through page 50.
- Virtex-7 T devices (XC7V585T and XC7V2000T) on page 51 through page 53.
- Virtex-7 XT devices (XC7VX330T, XC7VX415T, XC7VX485T, XC7VX550T, XC7VX690T, XC7VX980T, and XC7VX1140T) on page 54 through page 64.

XC7S6 and XC7S15 Banks

Figure 1-1 shows the I/O and transceiver banks.

FTGB196 Package

All HR I/O banks are fully bonded out in this package.

CPGA196 Package

All HR I/O banks are fully bonded out in this package.

CSGA225 Package

All HR I/O banks are fully bonded out in this package.

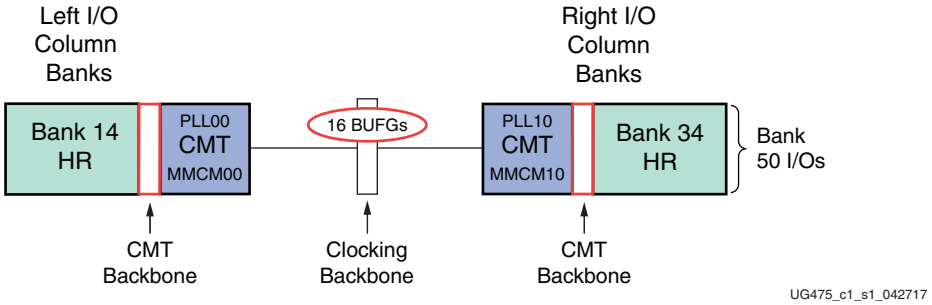


Figure 1-1: **XC7S6 and XC7S15 Banks**

XC7S25 Banks

Figure 1-2 shows the I/O and transceiver banks.

FTGB196 Package

HR I/O bank 15 is not bonded out.

CSGA225 Package

All HR I/O banks are fully bonded out in this package.

CSGA324 Package

All HR I/O banks are fully bonded out in this package.

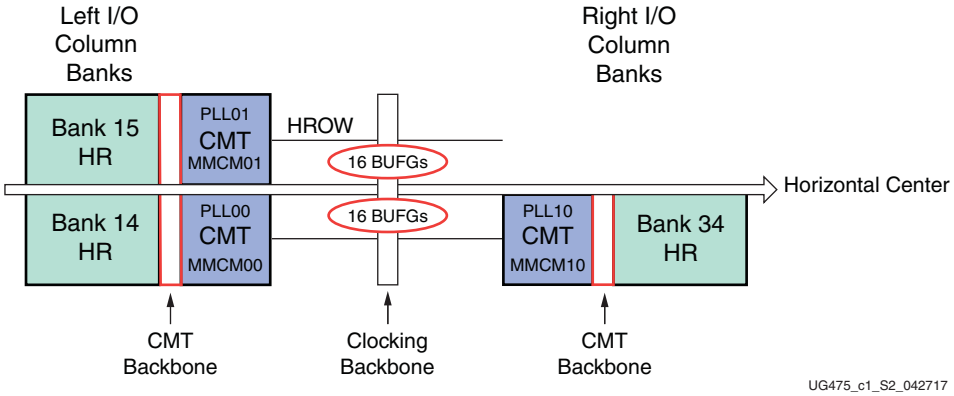


Figure 1-2: **XC7S25 Banks**

XC7S50 Banks

Figure 1-3 shows the I/O and transceiver banks.

FTGB196 Package

HR I/O banks 15, 16, and 35 are not bonded out.

CSGA324 Package

HR I/O bank 16 is partially bonded out.

FGGA484 Package

All HR I/O banks are fully bonded out in this package.

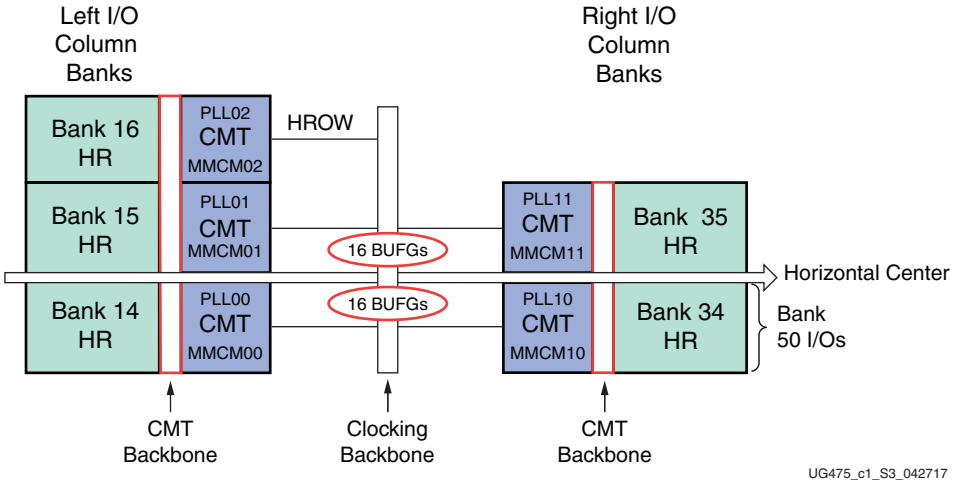


Figure 1-3: **XC7S50 Banks**

XC7S75 and XC7S100 Banks

Figure 1-4 shows the I/O and transceiver banks.

FGGA484 Package

- HR I/O bank 13 is partially bonded out.
- HR I/O bank 33 is not bonded out.

FGGA676 Package

All HR I/O banks are fully bonded out in this package.

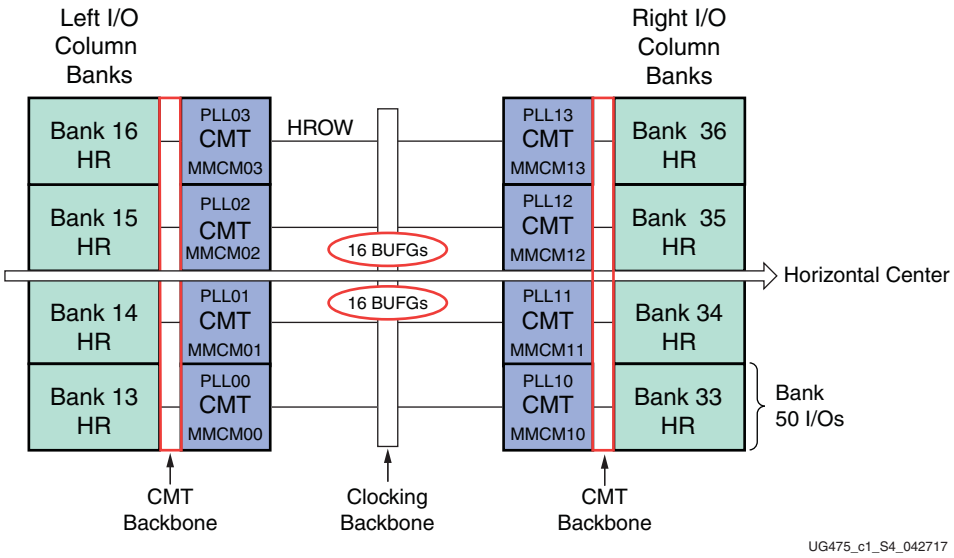


Figure 1-4: **XC7S75 and XC7S100 Banks**

XA7A12T and XC7A25T Banks

Figure 1-5 shows the I/O and transceiver banks.

CPG238 Package

- HR I/O banks 15 and 34 are partially bonded out.
- The GTP Quad 215 is partially bonded out.

CSG325 Package

- All HR I/O banks are fully bonded out in this package.
- All GTP Quads are fully bonded out.

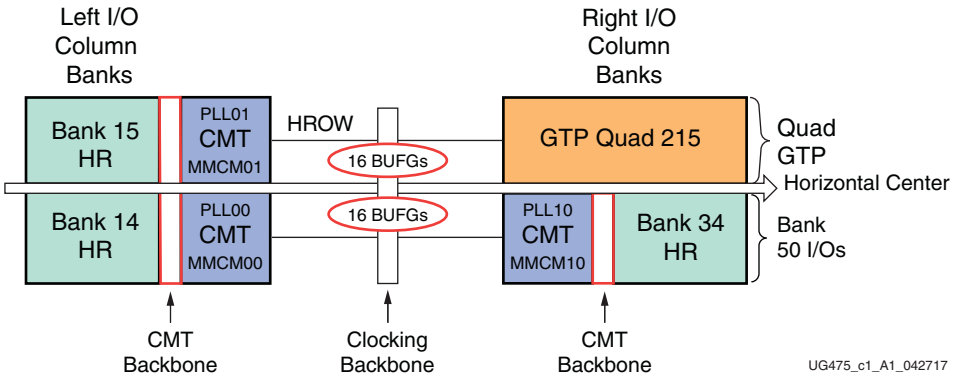


Figure 1-5: **XA7A12T and XC7A25T Banks**

XC7A15T, XC7A35T, XA7A15T, and XA7A35T Banks

Figure 1-6 shows the I/O and transceiver banks.

CPG236 Package

- HR I/O bank 15 is not bonded out.
- HR I/O banks 16, 34, and 35 are partially bonded out.
- The GTP Quad 216 is partially bonded out.

FTG256 Package (XC7A15T and XC7A35T only)

- HR I/O bank 16 is not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG324 Package

- HR I/O bank 16 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG325 Package

- HR I/O banks 16 and 35 are not bonded out.
- All GTP Quads are fully bonded out in this package.

FGG484 Package (XC7A15T and XC7A35T only)

All HR I/O banks and the GTP Quads are fully bonded out in this package.

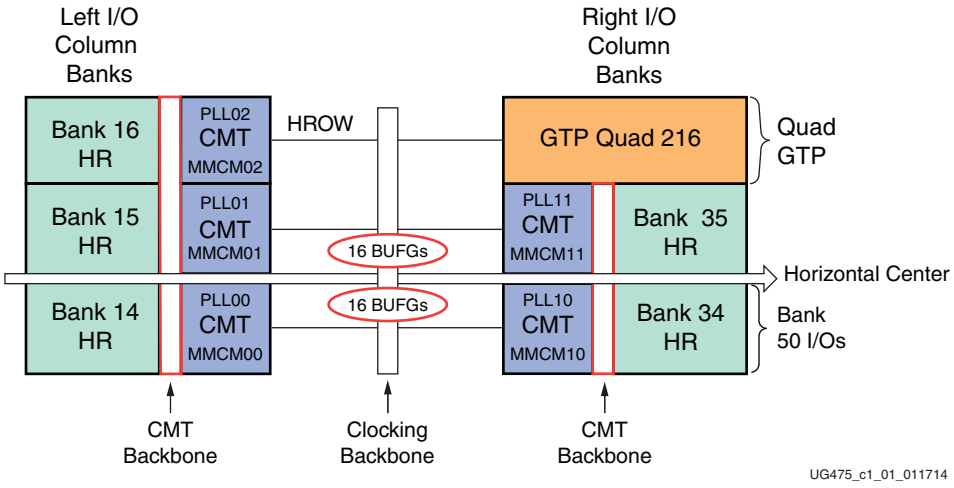


Figure 1-6: **XC7A15T, XC7A35T, XA7A15T, and XA7A35T Banks**

XC7A50T, XA7A50T, and XQ7A50T Banks

Figure 1-7 shows the I/O and transceiver banks.

CPG236 Package

- HR I/O bank 15 is not bonded out.
- HR I/O banks 16, 34, and 35 are partially bonded out.

FTG256 Package (XC7A50T only)

- HR I/O bank 16 is not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG324 Package

- HR I/O bank 16 is partially bonded out.
- The GTP Quad 216 is not bonded out.

CSG325 Package

- HR I/O banks 16 and 35 are not bonded out.
- All GTP Quads are fully bonded out in this package.

FGG484 Package (XC7A50T and XQ7A50T only)

All HR I/O banks and the GTP Quads are fully bonded out in this package.

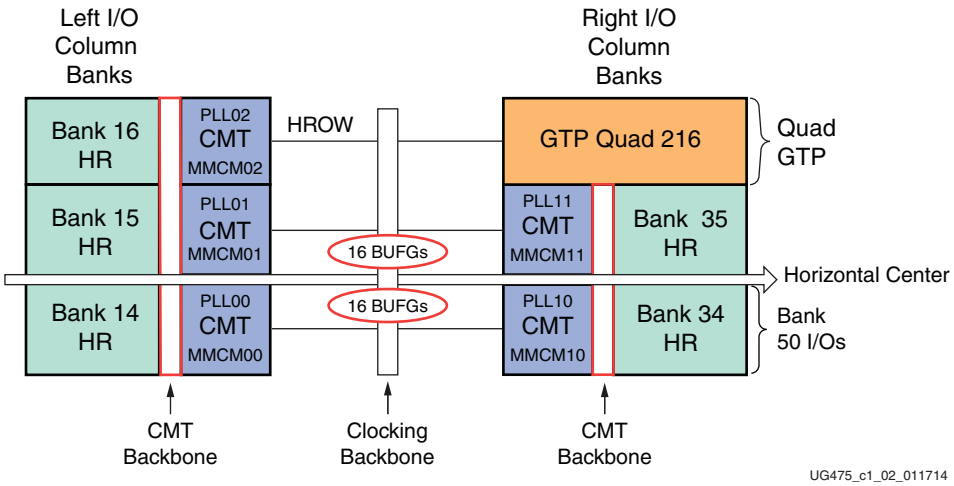


Figure 1-7: **XC7A50T, XA7A50T, and XQ7A50T Banks**

XC7A75T and XA7A75T Banks

Figure 1-8 shows the I/O and transceiver banks.

FTG256 Package (XC7A75T only)

- HR I/O banks 13 and 16 are not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

CSG324 Package

- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

FGG484 Package

- HR I/O bank 13 is partially bonded out.
- The GTP Quad 213 is not bonded out.

FGG676 Package (XC7A75T only)

All HR I/O banks and the GTP Quads are fully bonded out in this package.

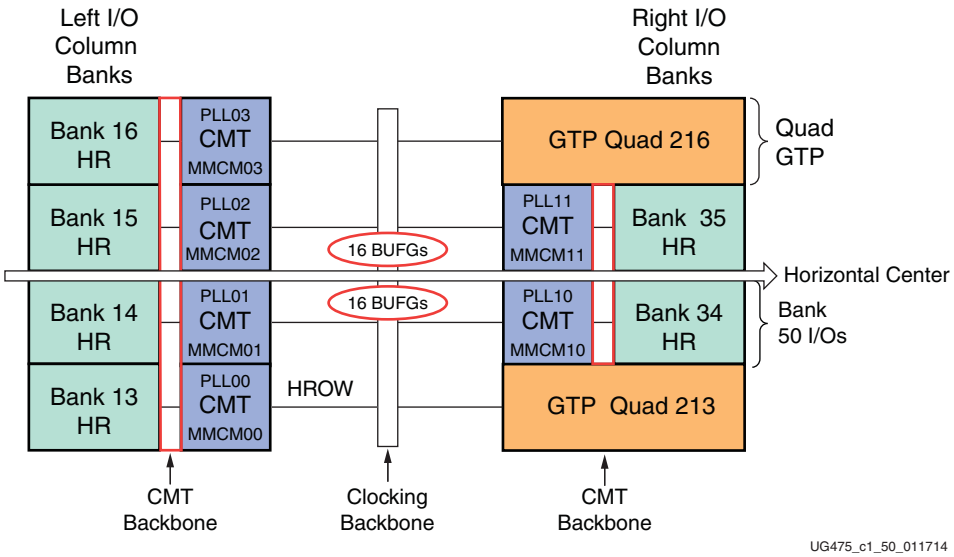


Figure 1-8: **XC7A75T and XA7A75T Banks**

XC7A100T, XQ7A100T, and XA7A100T Banks

Figure 1-9 shows the I/O and transceiver banks.

FTG256 Package (XC7A100T only)

- HR I/O banks 13 and 16 are not bonded out.
- HR I/O bank 34 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

CSG324 Package

- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

FGG484 Package

- HR I/O bank 13 is partially bonded out.
- The GTP Quad 213 is not bonded out.

FGG676 Package (XC7A100T only)

All HR I/O banks and the GTP Quads are fully bonded out in this package.

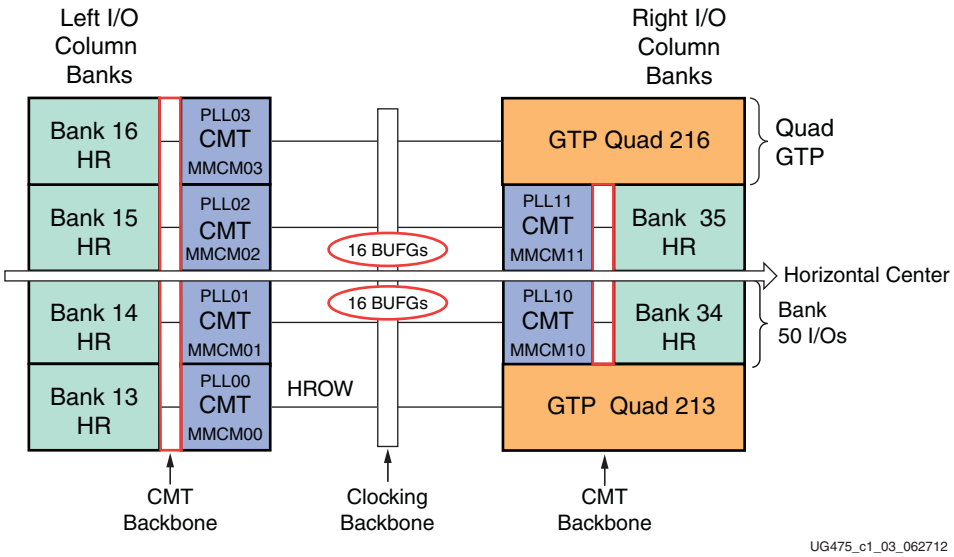


Figure 1-9: **XC7A100T, XQ7A100T, and XA7A100T Banks**

XC7A200T and XQ7A200T Banks

Figure 1-10 shows the I/O and transceiver banks.

SBG484, SBV484, and RS484 Packages

- HR I/O bank 13 is partially bonded out.
- HR I/O banks 12, 32, 33, and 36 are not bonded out.
- The GTP Quads 113, 116, and 213 are not bonded out.

FBG484, FBV484, and RB484 Packages

- HR I/O bank 13 is partially bonded out.
- HR I/O banks 12, 32, 33, and 36 are not bonded out.
- The GTP Quads 113, 116, and 213 are not bonded out.

FBG676, FBV676, and RB676 Packages

- HR I/O banks 32 and 36 are not bonded out.
- The GTP Quads 113 and 116 are not bonded out.

FFG1156 and FFV1156 Package (XC7A200T only)

All HR I/O banks and the GTP Quads are fully bonded out in this package.

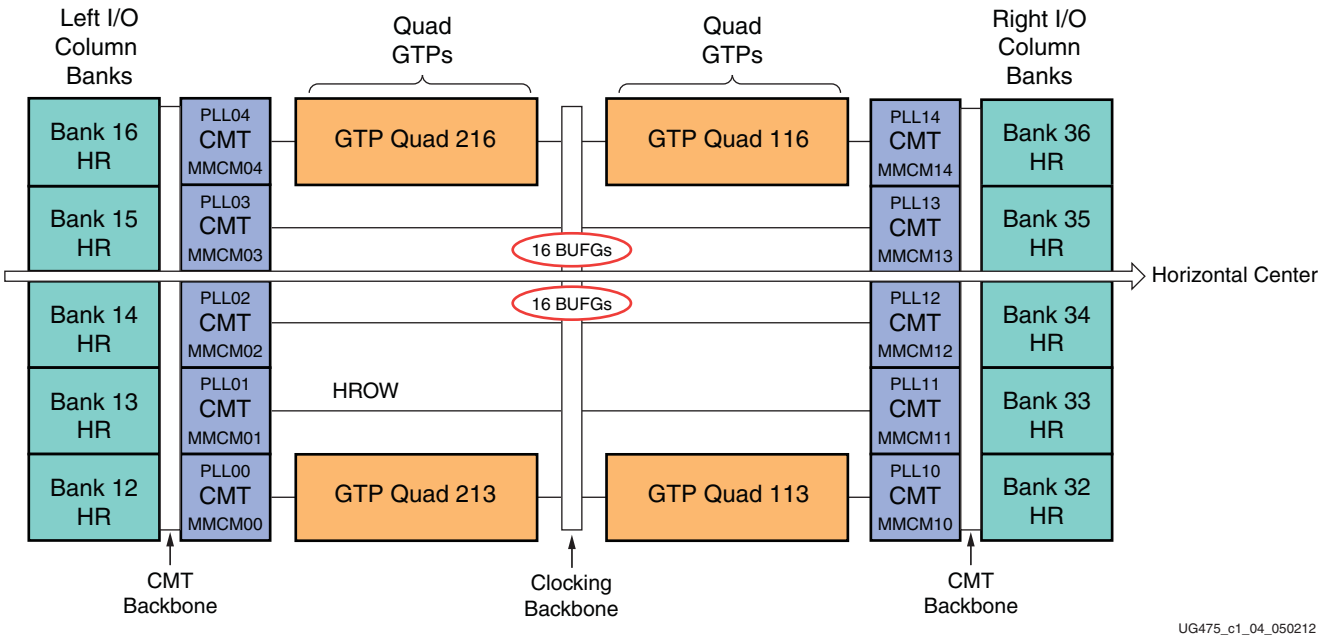


Figure 1-10: **XC7A200T and XQ7A200T Banks**

XC7K70T Banks

Figure 1-11 shows the I/O and transceiver banks for the XC7K70T.

FBG484 and FBV484 Package

- HR I/O bank 16 is partially bonded out.
- All HP I/O banks are fully bonded out.
- The GTX Quad 116 is not bonded out.

FBG676 and FBV676 Package

All HR and HP I/O banks and the GTX Quads are fully bonded out in this package.

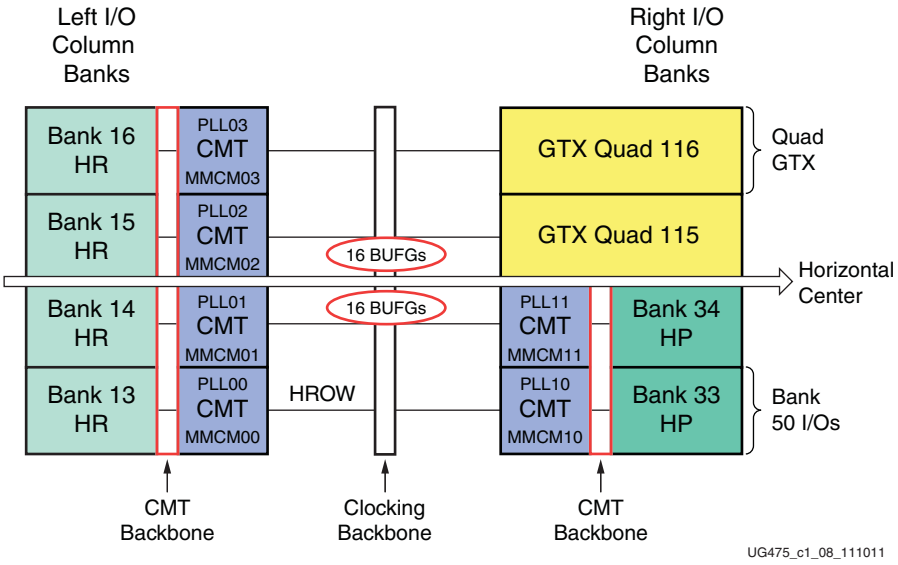


Figure 1-11: **XC7K70T Banks**

XC7K160T Banks

Figure 1-12 shows the I/O and transceiver banks for the XC7K160T.

FBG484 and FBV484 Package

- HR I/O bank 12 is not bonded out and bank 16 is partially bonded out.
- HP I/O bank 32 is not bonded out.
- The GTX Quad 116 is not bonded out.

FBG676, FBV676, FFG676, and FFV676 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

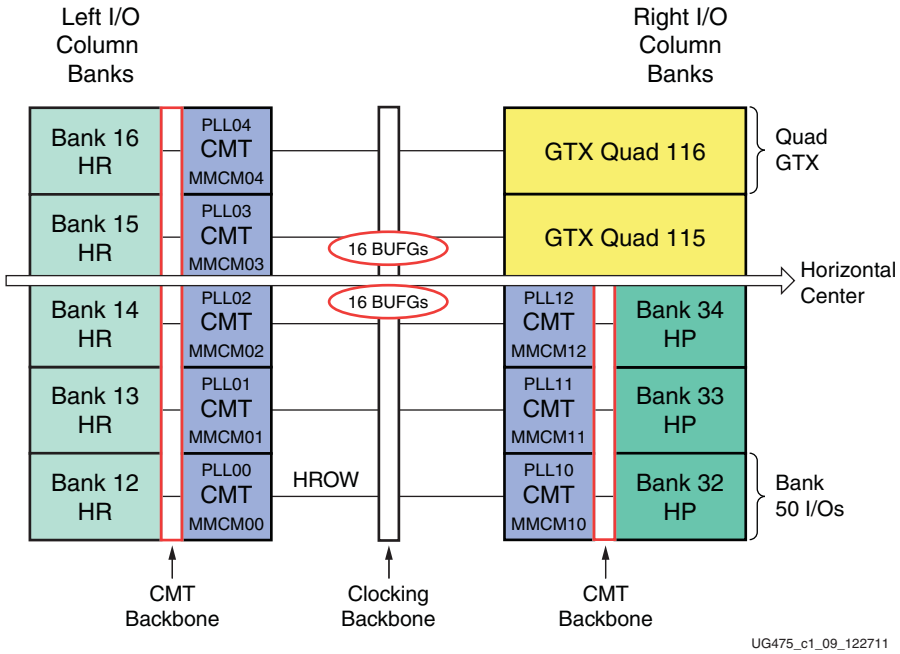


Figure 1-12: **XC7K160T Banks**

XC7K325T and XQ7K325T Banks

Figure 1-13 shows the I/O and transceiver banks for the XC7K325T and XQ7K325T.

FBG676, FBV676, FFG676, FFV676, and RF676 Packages

- HR I/O banks 17 and 18 are not bonded out.
- All HP I/O banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900, FBV900, FFG900, FFV900, and RF900 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

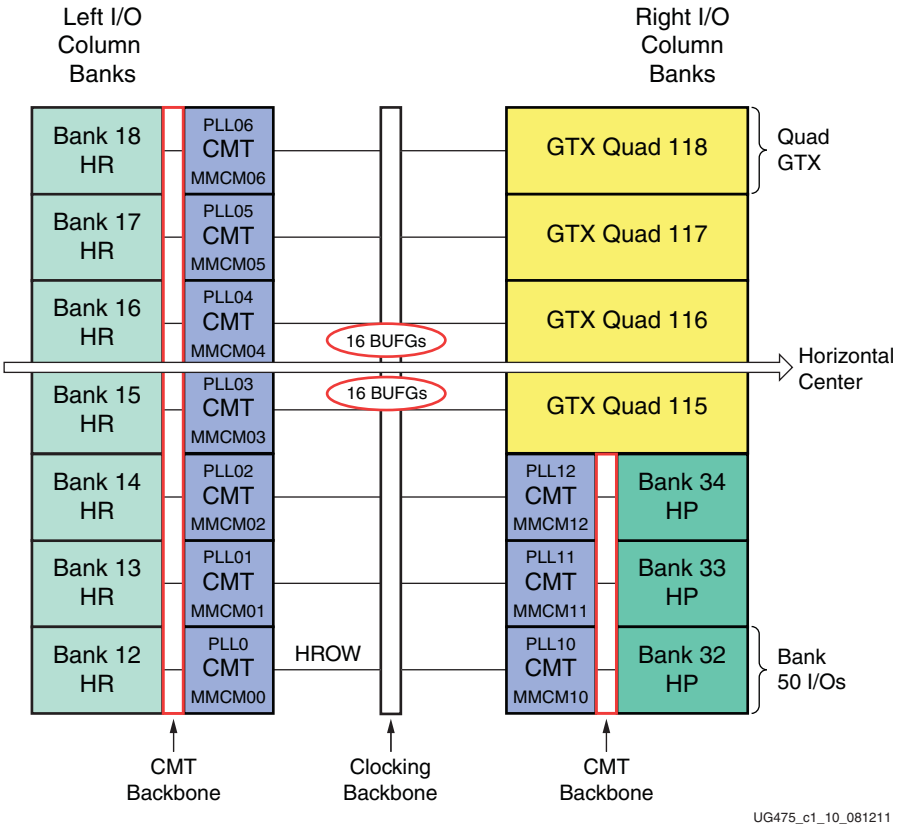


Figure 1-13: **XC7K325T and XQ7K325T Banks**

XC7K355T Banks

Figure 1-14 shows the I/O and transceiver banks for the XC7K355T.

FFG901 and FFV901 Package

All HR I/O banks and the GTX Quads are fully bonded out in this package.

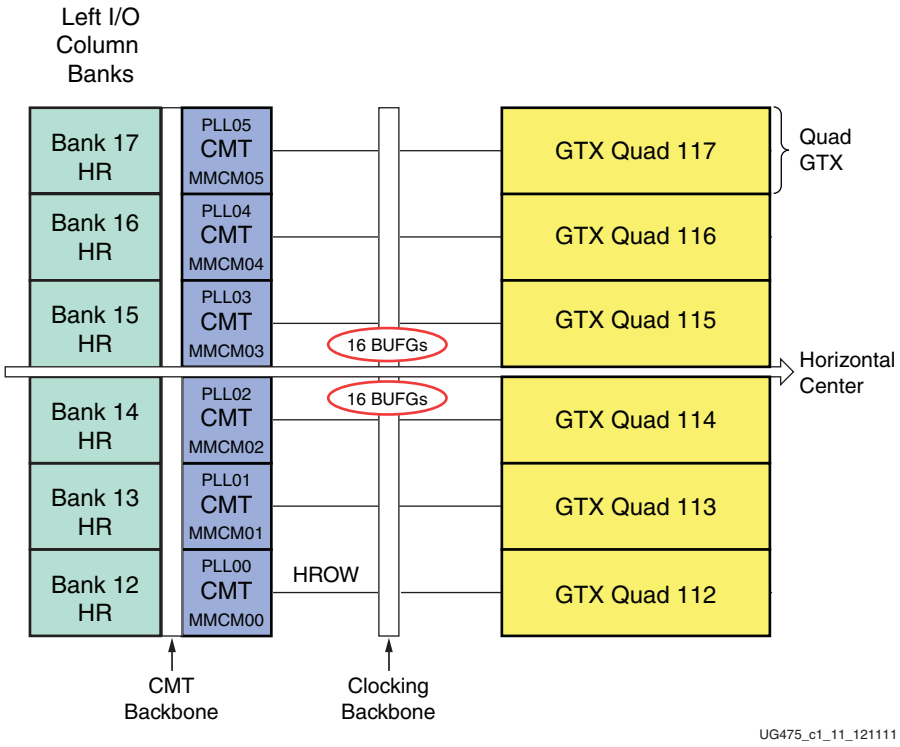


Figure 1-14: **XC7K355T Banks**

XC7K410T and XQ7K410T Banks

Figure 1-15 shows the I/O and transceiver banks for the XC7K410T and XQ7K410T.

FBG676, FBV676, FFG676, FFV676, and RF676 Packages

- HR I/O banks 17 and 18 are not bonded out.
- All HP I/O banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900, FBV900, FFG900, FFV900, and RF900 Packages

All HR and HP I/O banks and the GTX Quads are fully bonded out in these packages.

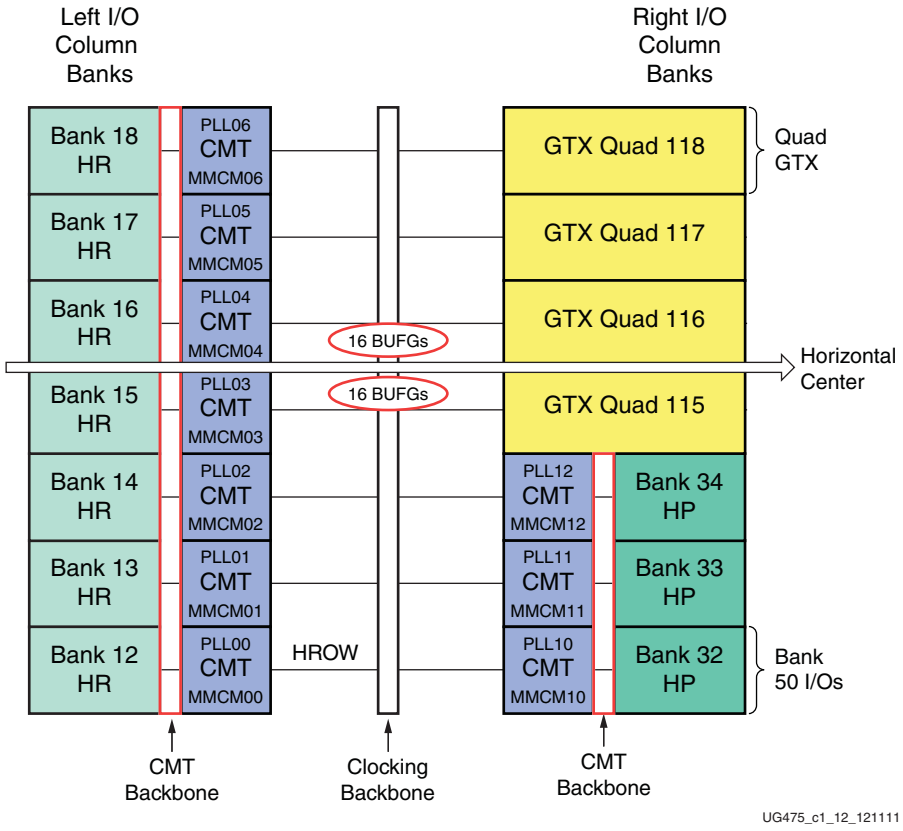


Figure 1-15: **XC7K410T and XQ7K410T Banks**

XC7K420T Banks

Figure 1-16 shows the I/O and transceiver banks for the XC7K420T.

FFG901 and FFV901 Package

- HR I/O bank 18 is not fully bonded out.
- GTX Quad 118 is not bonded out.

FFG1156 and FFV1156 Package

All HR I/O banks and the GTX Quads are fully bonded out in this package.

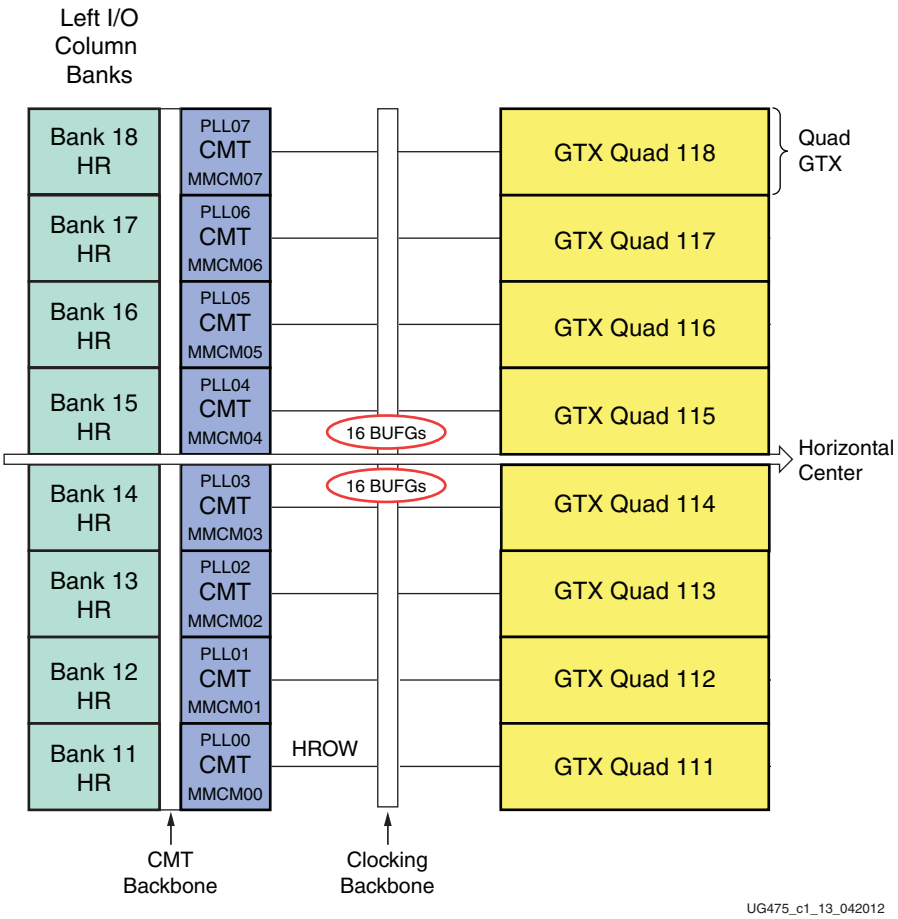


Figure 1-16: **XC7K420T Banks**

XC7K480T Banks

Figure 1-17 shows the I/O and transceiver banks for the XC7K480T.

FFG901 and FFV901 Package

- HR I/O bank 18 is not fully bonded out.
- GTX Quad 118 is not bonded out.

FFG1156 and FFV1156 Package

All HR I/O banks and the GTX Quads are fully bonded out in this package.

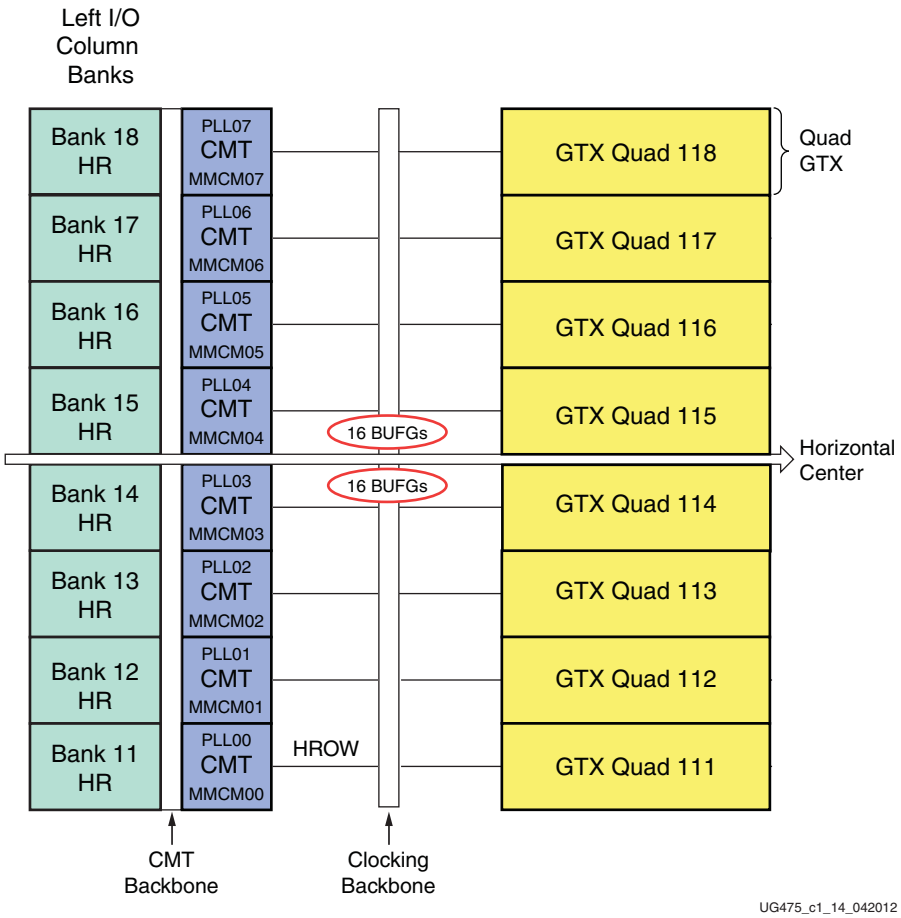


Figure 1-17: **XC7K480T Banks**

XC7V585T and XQ7V585T Banks

Figure 1-18 shows the I/O and transceiver banks for the XC7V585T and XQ7V585T.

FFG1157 and RF1157 Packages

- All HR I/O banks (11, 12, and 13) are not bonded out.
- HP I/O banks 31, 32, and 33 are not bonded out.
- GTX Quads 111, 112, 113, and 119 are not bonded out.

FFG1761 and RF1761 Packages

- HR I/O bank 11 is not bonded out.
- All HP I/O banks and the GTX Quads are fully bonded out in these packages.

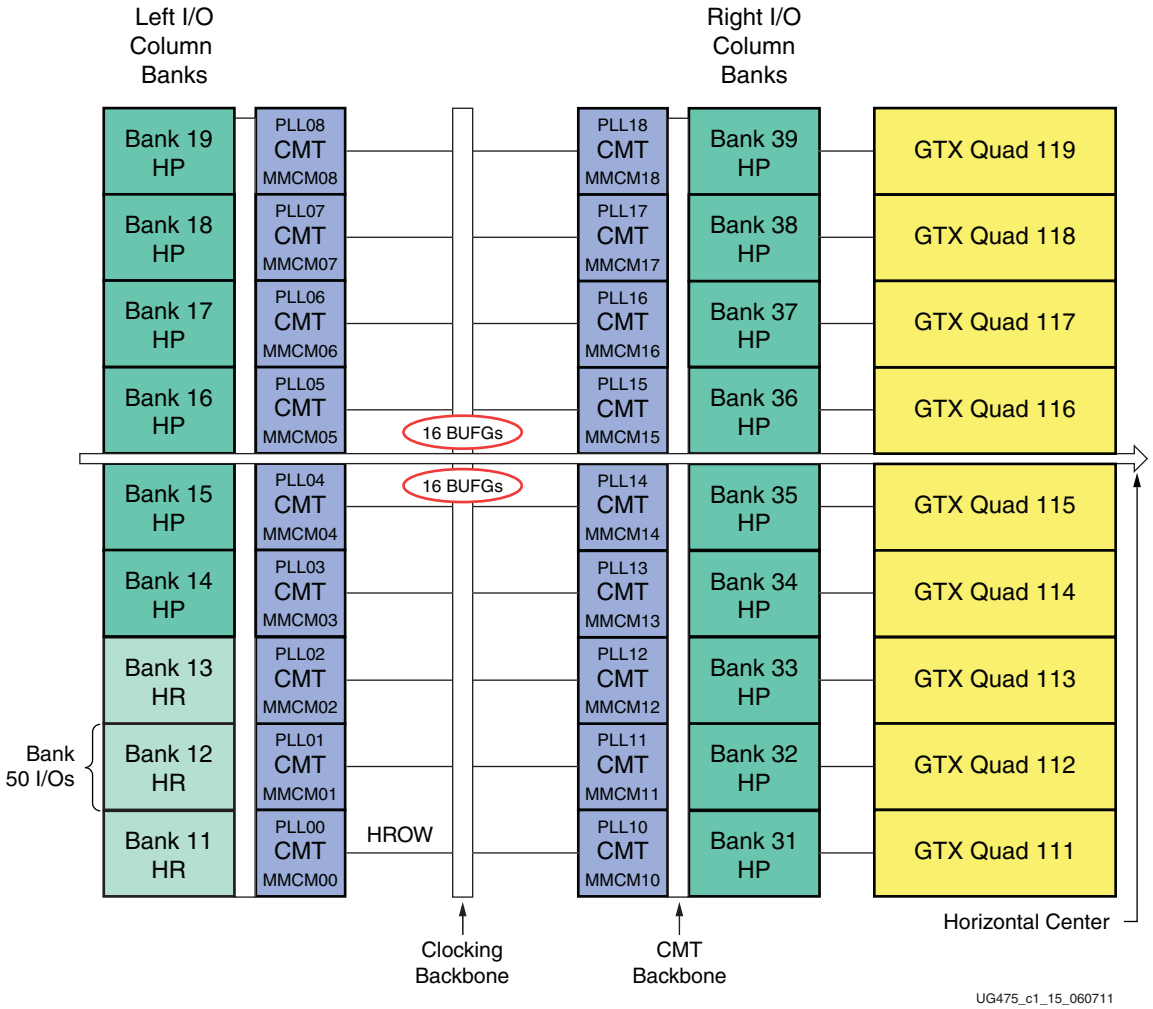


Figure 1-18: **XC7V585T and XQ7V585T Banks**

XC7V2000T Banks

Figure 1-19 shows the I/O and transceiver banks for the XC7V2000T.

FHG1761 Package

- HP I/O banks 11, 20, 21, 22, 40, 41, and 42 are not bonded out.
- GTX Quads 120, 121, and 122 are not bonded out.

FLG1925 Package

- All HP I/O banks are fully bonded out in this package.
- GTX Quads 111, 116, 117, 118, 119, 120, 121, and 122 are not bonded out.

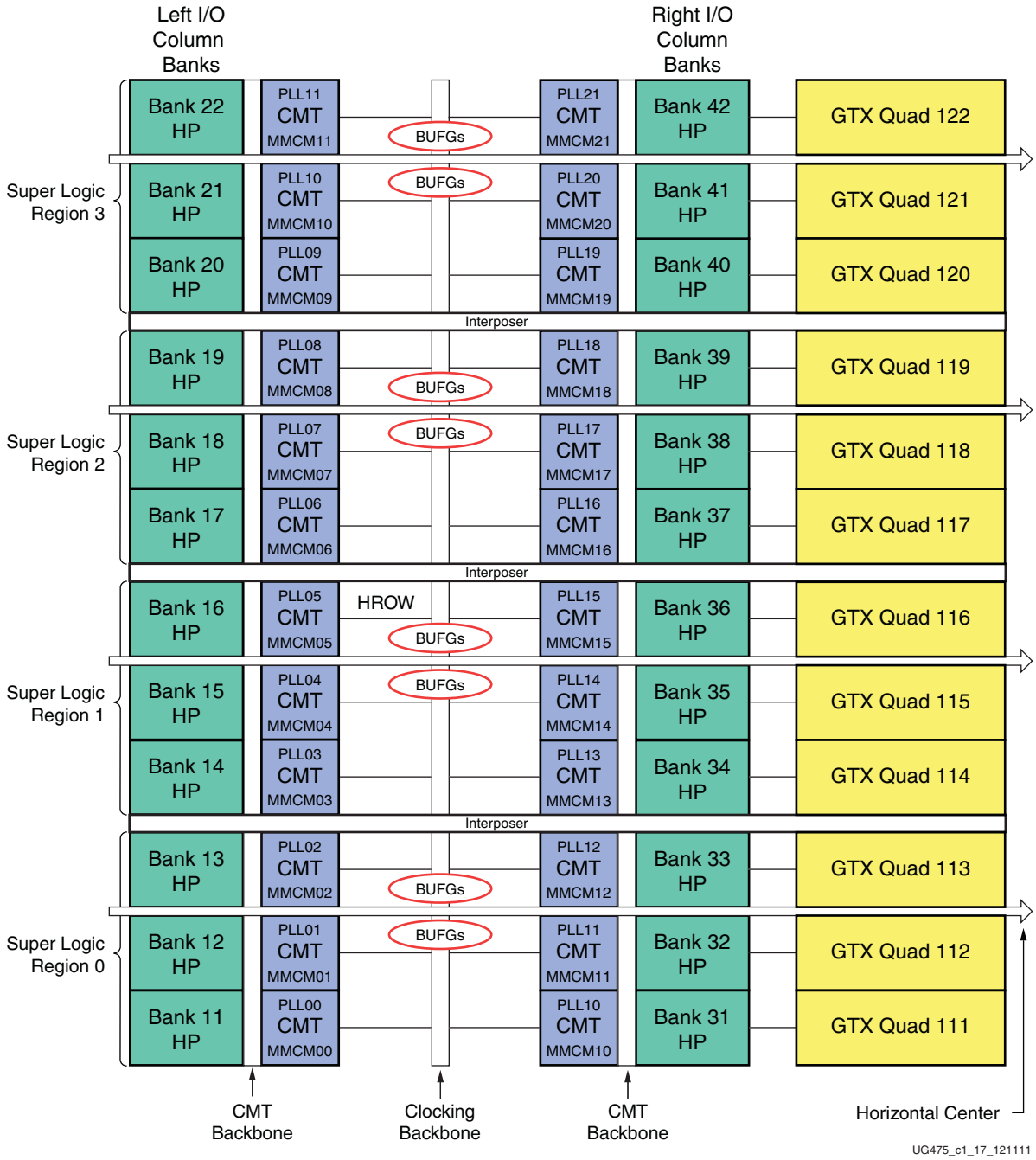


Figure 1-19: **XC7V2000T Banks**

XC7VX330T and XQ7VX330T Banks

Figure 1-20 shows the I/O and transceiver banks for the XC7VX330T and XQ7VX330T.

FFG1157, FFV1157, and RF1157 Packages

- HR I/O bank 13 is not bonded out.
- HP I/O bank 33 is not bonded out.
- GTH Quads 113 and 119 are not bonded out.

FFG1761, FFV1761, and RF1761 Packages

All HR and HP I/O banks and the GTH Quads are fully bonded out in these packages.

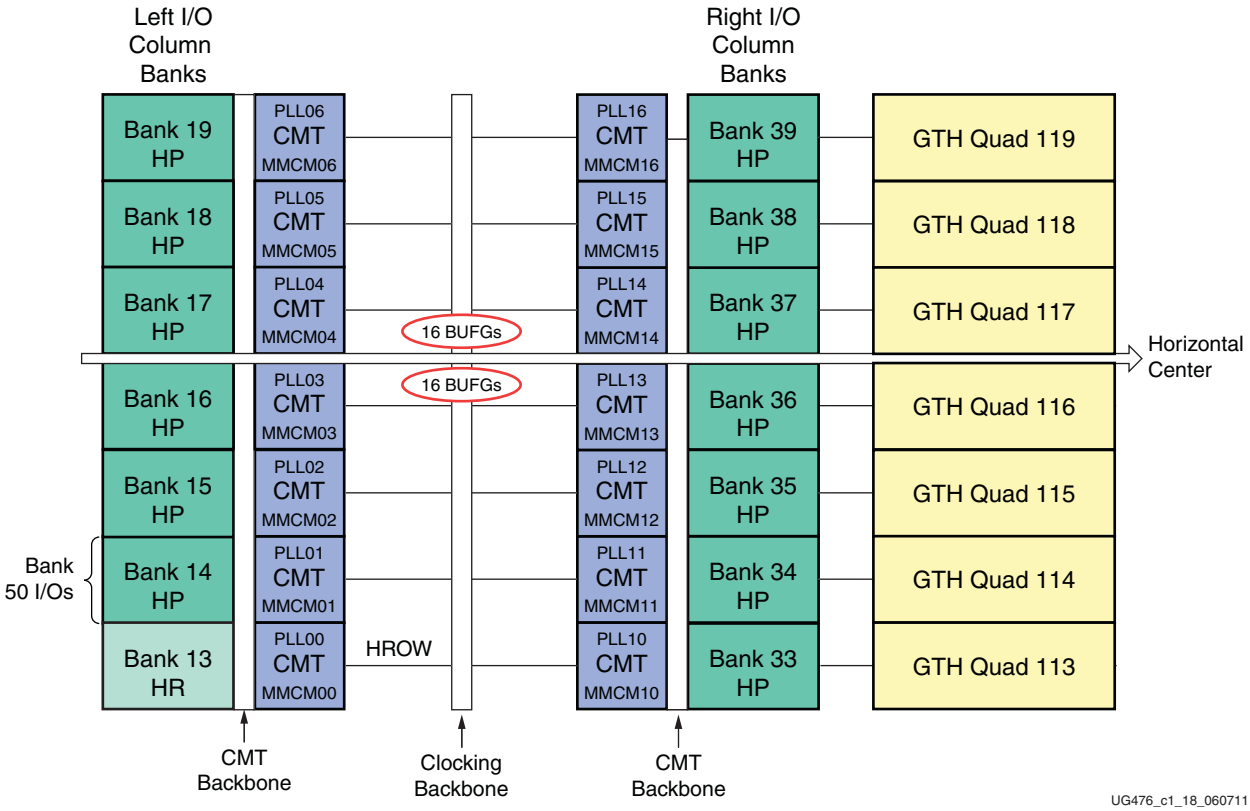


Figure 1-20: **XC7VX330T and XQ7VX330T Banks**

XC7VX415T Banks

Figure 1-21 shows the I/O and transceiver banks for the XC7VX415T.

FFG1157 and FFV1157 Package

- All HP I/O banks are fully bonded out.
- GTH Quads 119, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 and FFV1158 Package

- HP I/O banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads are fully bonded out in this package.

FFG1927 and FFV1927 Package

All HP I/O banks and the GTH Quads are fully bonded out in this package.

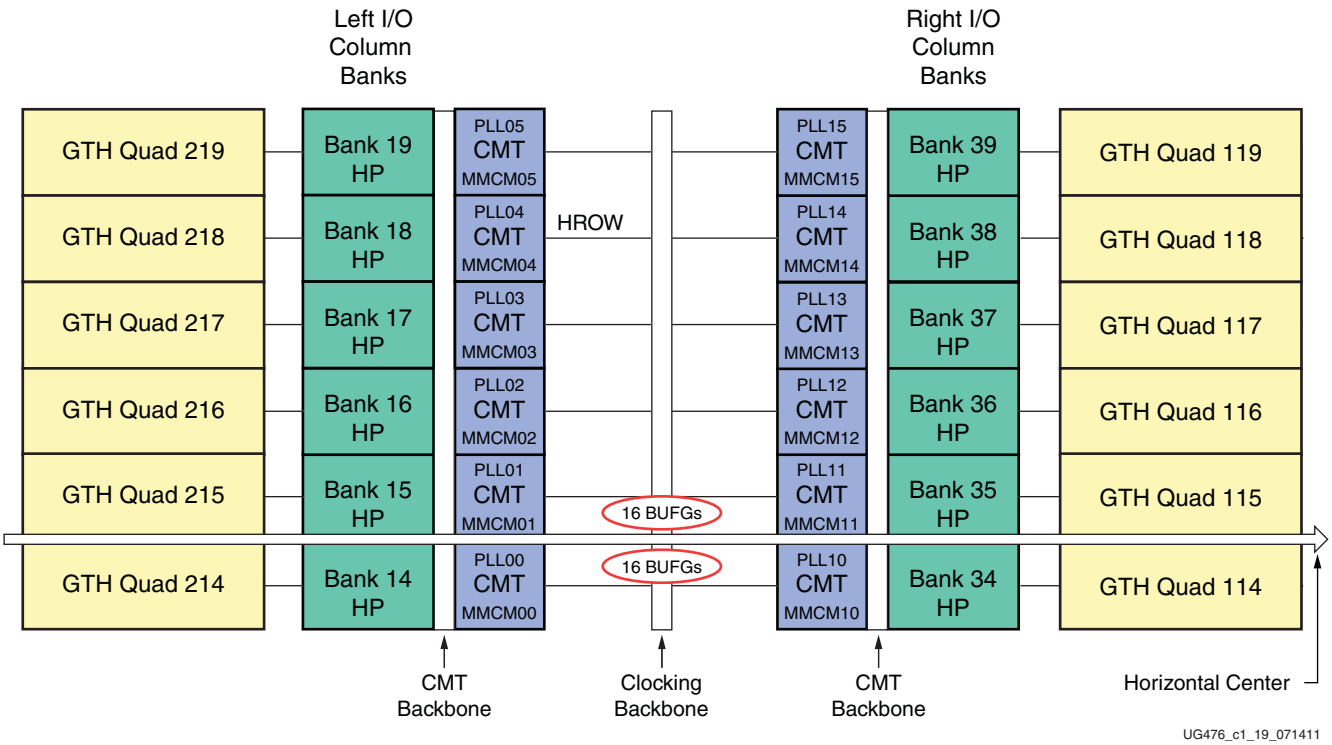


Figure 1-21: **XC7VX415T Banks**

XC7VX485T and XQ7VX485T Banks

Figure 1-22 shows the I/O and transceiver banks for the XC7VX485T and XQ7VX485T.

FFG1157 Package

- HP I/O banks 13 and 33 are not bonded out.
- GTX Quads 113, 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Packages

- HP I/O banks 13, 18, 19, 33, 37, 38, and 39 are not bonded out.
- GTX Quads 113 and 213 are not bonded out.

FFG1761 and RF1761 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTX Quads 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1927 Package

- HP I/O banks 13 and 33 are not bonded out.
- All the GTX Quads are fully bonded out in this package.

FFG1930 and RF1930 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTX Quads 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

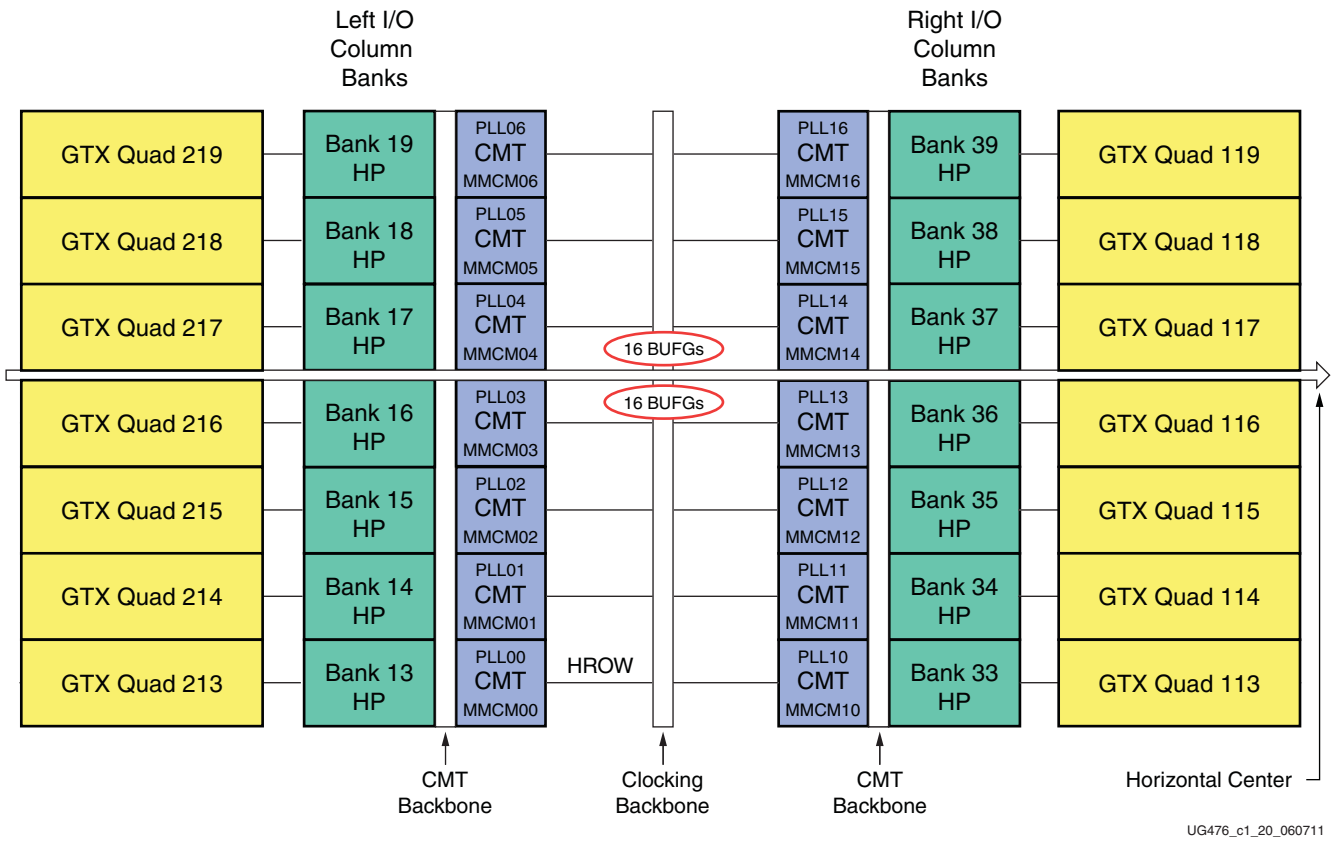


Figure 1-22: **XC7VX485T and XQ7VX485T Banks**

XC7VX550T Banks

Figure 1-23 shows the I/O and transceiver banks for the XC7VX550T.

FFG1158 Package

- HP I/O banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1927 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

Figure 1-23: **XC7VX550T Banks**

XC7VX690T and XQ7VX690T Banks

Figure 1-24 shows the I/O and transceiver banks for the XC7VX690T and XQ7VX690T.

FFG1157 and RF1157 Packages

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- GTH Quads 110, 111, 112, 113, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 and RF1158 Packages

- HP I/O banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1761 and RF1761 Packages

- HP I/O banks 10, 11, and 30 are not bonded out.
- GTH Quads 110, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 119, 210, and 219 are not bonded out.

FFG1927 Package

- HP I/O banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 and RF1930 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTH Quads 110, 111, 112, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

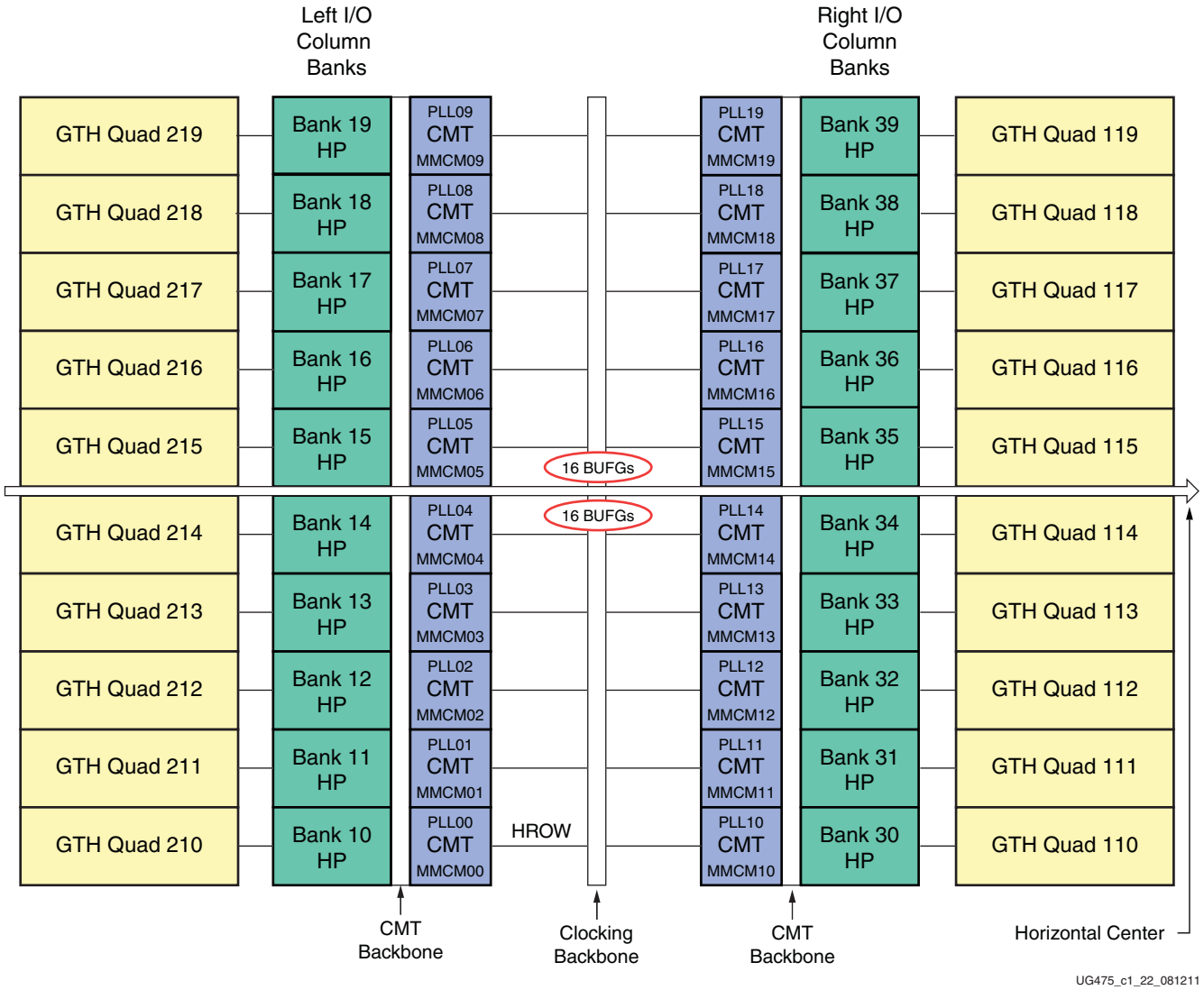


Figure 1-24: **XC7VX690T and XQ7VX690T Banks**

XC7VX980T and XQ7VX980T Banks

Figure 1-25 shows the I/O and transceiver banks for the XC7VX980T and XQ7VX980T.

FFG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 37, and 38 are not bonded out.
- GTH Quads 110 and 210 are not bonded out.

FFG1928 Package

- HP I/O bank 16 is partially bonded out.
- HP I/O banks 10, 11, 12, 17, 18, 30, 31, and 32 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 and RF1930 Packages

- All HP I/O banks are fully bonded out in these packages.
- GTH Quads 110, 111, 112, 210, 211, 212, 213, 214, 215, 216, 217, and 218 are not bonded out.

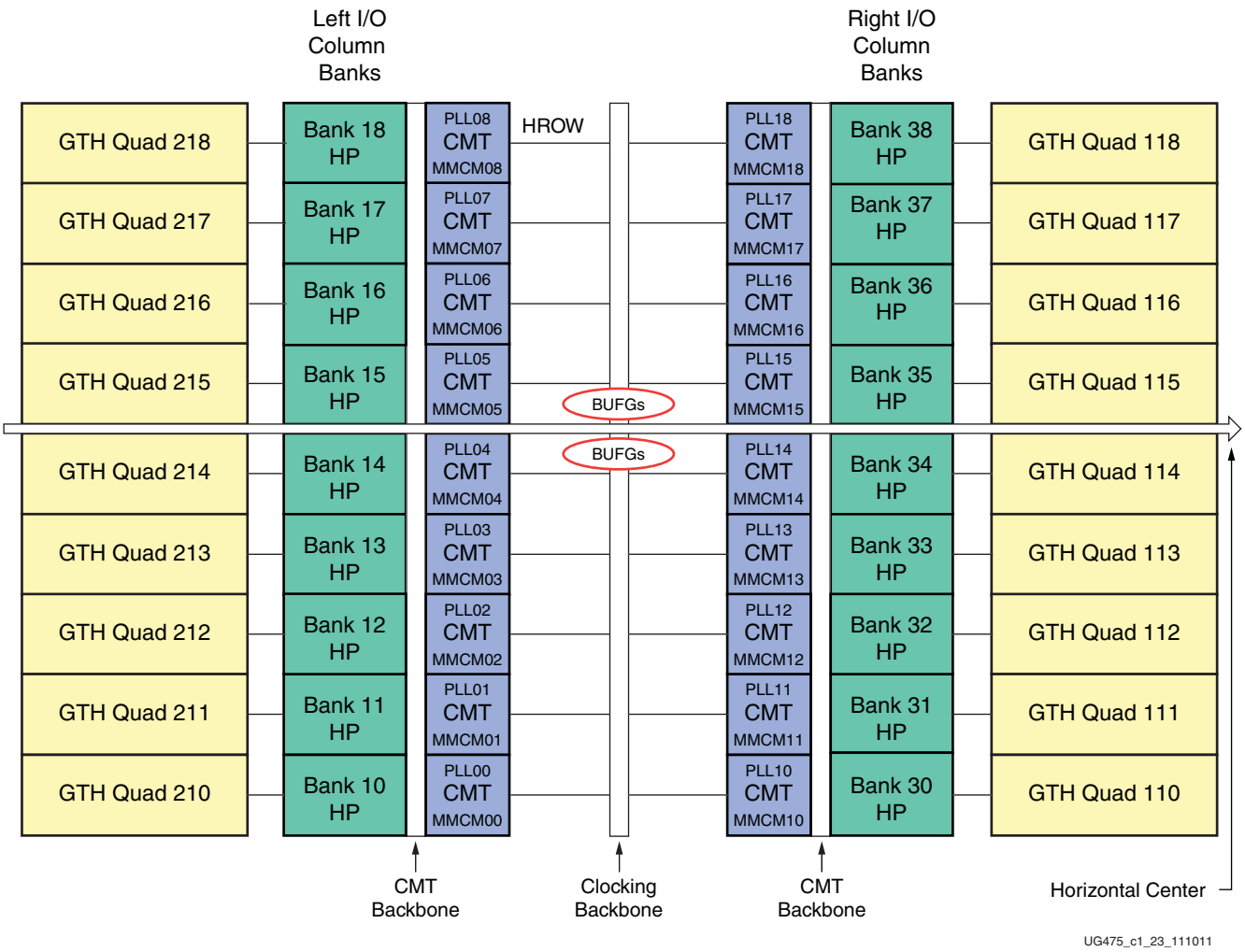


Figure 1-25: **XC7VX980T and XQ7VX980T Banks**

XC7VX1140T Banks

Figure 1-26 shows the I/O and transceiver banks for the XC7VX1140T.

FLG1926 Package

- HP I/O bank 17 is partially bonded out.
- HP I/O banks 18, 19, 20, 21, 37, 38, 39, 40, and 41 are not bonded out.
- GTH Quads 110, 119, 120, 121, 210, 219, 220, and 221 are not bonded out.

FLG1928 Package

- HP I/O bank 16 is partially bonded out.
- HP I/O banks 10, 11, 12, 17, 18, 19, 20, 21, 30, 31, 32, 39, 40, and 41 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FLG1930 Package

- HP I/O banks 40 and 41 are not bonded out.
- GTH Quads 110, 111, 112, 119, 120, 121, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, and 221 are not bonded out.

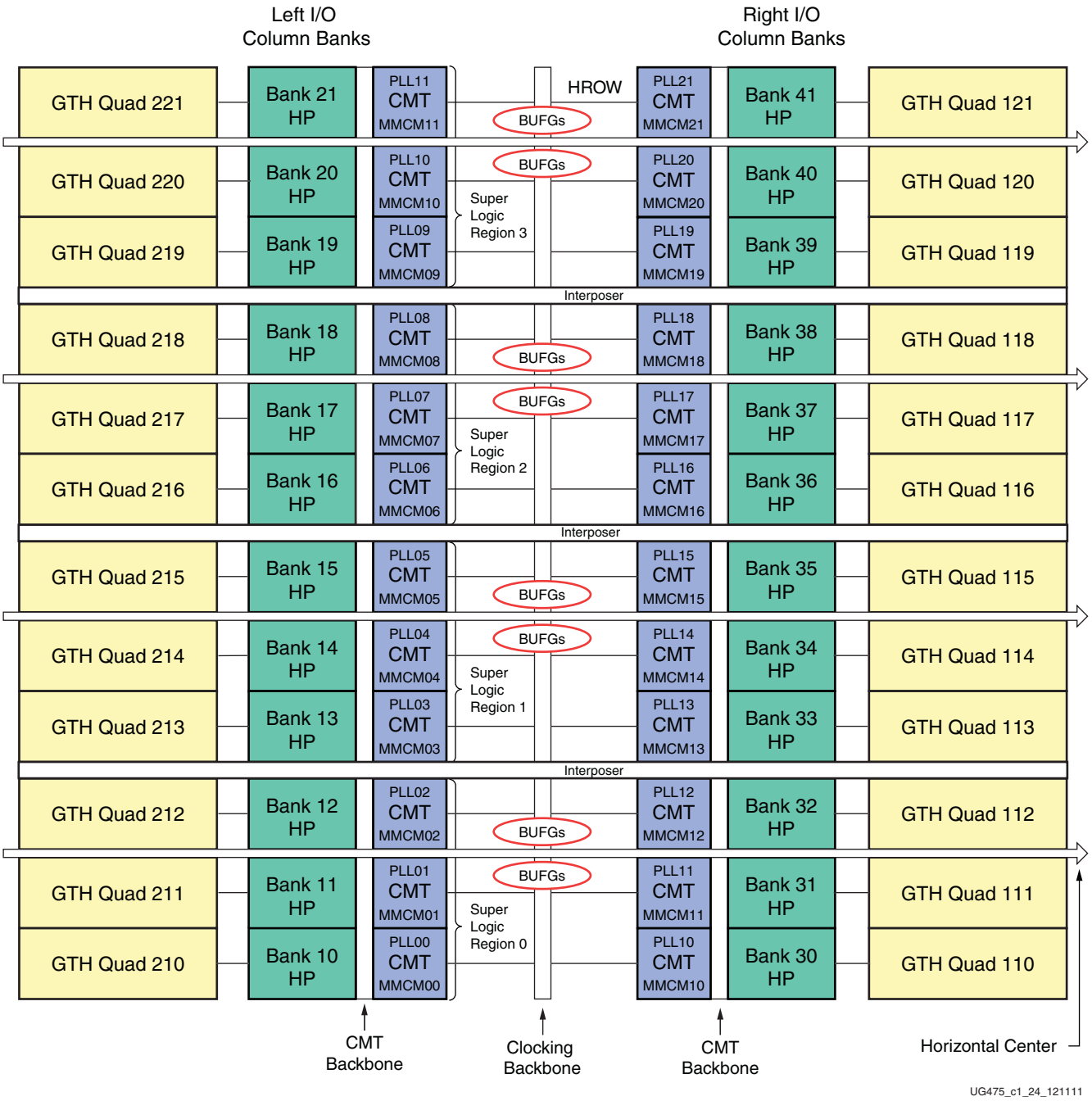


Figure 1-26: **XC7VX1140T Banks**

7 Series FPGAs Package Files

About ASCII Package Files

The ASCII files for each package include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor. Each of the files consists of the following:

- Device/Package name (*FPGA Family—Device—Package*), date and time of creation
- Eight columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3. For more information on the memory byte group, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
  - Bank—Bank number.
  - V_{CCAUX} Group—Number corresponding to the V_{CCAUX_IO} power supply for the given pin. V_{CCAUX} is shown for packages with only one V_{CCAUX} group.
  - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
  - I/O Type—CONFIG, HR, HP, or GT (GTP, GTX, GTH) depending on the I/O type. For more information on the I/O type, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).
  - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.
- The package file links for the ruggedized packages have the same pinouts are as the equivalent BGA packages.
  - RS pinouts use the SBG/SBV files (Artix®-7 devices)
  - RB pinouts use the FBG/FBV files (Artix-7 devices)
  - RF pinouts use the FFG/FFV files (Kintex®-7 and Virtex®-7 devices)

Package Specifications Designations

Package specifications are designated as evaluation only, engineering sample, or production. Each designation is defined as follows.

Evaluation Only

These package specifications are based on initial device specifications, package routability analysis and mechanical package construction. Package specifications with this designation are not stable and package pinouts are likely to change and these specifications should only be used for initial system level design feasibility.

Engineering Sample

These package specifications are based on a released package design and validated with ES engineering sample (ES) devices. Package specifications with this designation are considered stable, however some pinout and mechanical specifications might change prior to the production release of the particular device. Package pinouts with this designation are to be used for PCB and Vivado designs using ES devices.

Production

These package specifications are released coincident with production release of a particular device. Customers receive formal notification of any subsequent changes.

IMPORTANT: *When a package specification designation is not in the packages file, the device/package combination is already production released.*

ASCII Pinout Files

This chapter includes the pinout information tables for the following device/packages. For brevity, all the package selections are not listed in the link ZIP file names. For more information on available device and package choices, consult the device/package ordering information tables in the *7 Series FPGAs Overview* (DS180), or the *7 Series Product Selection Guide*. The XA devices are further outlined in the *XA* Artix®-7 *FPGAs Data Sheet Overview* (DS197) and *XA* Spartan®-7 *Automotive FPGA Data Sheet: Overview* (DS171). The XQ devices are outlined in the *Defense-Grade 7 Series FPGAs Overview* (DS185).

Note: All package files are ASCII files in TXT and CSV file format.

To download all available Spartan-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/spartan-7-pkgs.html

Table 2-1: **Spartan-7 FPGAs Package/Device Pinout Files**

Device	CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
XC7S6	CPGA196 Engineering Sample	CSGA225 Engineering Sample		FTGB196 Engineering Sample		
XC7S15	CPGA196 Engineering Sample	CSGA225 Engineering Sample		FTGB196 Engineering Sample		
XC7S25		CSGA225 Production	CSGA324 Production	FTGB196 Production		
XC7S50			CSGA324 Production	FTGB196 Production	FGGA484 Production	
XC7S75					FGGA484 Production	FGGA676 Production
XC7S100					FGGA484 Production	FGGA676 Production

To download all available Artix-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/artix-7-pkgs.html

Table 2-2: **Artix-7 FPGAs Package/Device Pinout Files**

Device	CPG 236	CPG 238	CS CSG 324	CS CSG 325	FTG 256	SBG SBV 484	FG FGG 484	FGG 676	FBG FBV 484	FBG FBV 676	FFG FFV 1156	RB 484	RS 484	RB 676
XC7A12T		CPG238		CSG325										
XC7A15T	CPG236		CSG324	CSG325	FTG256		FGG484							
XC7A25T		CPG238		CSG325										
XC7A35T	CPG236		CSG324	CSG325	FTG256		FGG484							
XC7A50T	CPG236		CSG324	CSG325	FTG256		FGG484							
XC7A75T			CSG324		FTG256		FGG484	FGG676						
XC7A100T			CSG324		FTG256		FGG484	FGG676						
XC7A200T						SBG484			FBG484	FBG676	FFG1156			
XA7A12T		CPG238		CSG325										
XA7A15T	CPG236		CSG324	CSG325										
XA7A25T		CPG238		CSG325										
XA7A35T	CPG236		CSG324	CSG325										
XA7A50T	CPG236		CSG324	CSG325										
XA7A75T			CSG324				FGG484							
XA7A100T			CSG324				FGG484							
XQ7A50T				CS325			FG484							
XQ7A100T			CS324				FG484							
XQ7A200T												RB484	RS484	RB676

To download all available Kintex-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/kintex-7-pkgs.html

Note: Only the available files listed in Table 2-3 are linked and consolidated in the above ZIP file.

Table 2-3: **Kintex-7 FPGAs Package/Device Pinout Files**

Device	FB484 FBG484 FBV484	FB676 FBG676 FBV676	FB900 FBG900 FBV900	FF676 FFG676 FFV676	FF900 FFG900 FFV900	FF901 FFG901 FFV901	FF1156 FFG1156 FFV1156	RF676	RF900
XC7K70T	FBG484	FBG676							
XC7K160T	FBG484	FBG676		FFG676					
XC7K325T		FBG676	FBG900	FFG676	FFG900				
XC7K355T						FF901/ FFG901			
XC7K410T		FBG676	FBG900	FFG676	FFG900				
XC7K420T						FFG901	FFG1156		
XC7K480T						FFG901	FFG1156		
XQ7K325T								RF676	RF900
XQ7K410T								RF676	RF900

To download all available Virtex-7 FPGAs package/device/pinout files click here:

www.xilinx.com/support/package-pinout-files/virtex-7-pkgs.html

Note: Only the available files listed in Table 2-4 and Table 2-5 are linked and consolidated in the above ZIP file.

Table 2-4: **Virtex-7 T FPGAs Package/Device Pinout Files**

Device	FF1157/FFG1157	FF1761/FFG1761	FL1925/FLG1925	FH1761/FHG1761	RF1157	RF1761
XC7V585T	FFG1157	FFG1761				
XC7V2000T			FLG1925	FHG1761		
XQ7V585T					RF1157	RF1761

Table 2-5: **Virtex-7 XT FPGAs Package/Device Pinout Files**

Device	FF1157 FFG1157 FFV1157 RF1157	FF1158 FFG1158 FFV1158 RF1158	FF1761 FFG1761 FFV1761 RF1761	FF1926 FFG1926	FF1927 FFG1927 FFV1927	FF1928 FFG1928	FF1930 FFG1930 RF1930	FL1926 FLG1926	FL1928 FLG1928	FL1930 FLG1930
XC7VX330T	FFG1157		FFG1761							
XC7VX415T	FFG1157	FFG1158			FFG1927					
XC7VX485T	FFG1157	FFG1158	FFG1761		FFG1927		FFG1930			
XC7VX550T		FFG1158			FFG1927					
XC7VX690T	FFG1157	FFG1158	FFG1761	FFG1926	FFG1927		FFG1930			
XC7VX980T				FFG1926		FFG1928	FFG1930			
XC7VX1140T								FLG1926	FLG1928	FLG1930
XQ7VX330T	RF1157		RF1761							
XQ7VX485T			RF1761				RF1930			
XQ7VX690T	RF1157	RF1158	RF1761				RF1930			
XQ7VX980T							RF1930			

Device Diagrams

Summary

This chapter provides pinout, high-performance and high-range I/O bank, memory groupings, and power and ground placement diagrams for each 7 series (Artix®-7, Kintex®-7, Spartan®-7, and Virtex®-7) FPGA package/device combination.

- Spartan-7 FPGAs Device Diagrams, page 72
- Artix-7 FPGAs Device Diagrams, page 95
- Kintex-7 FPGAs Device Diagrams, page 132
- Virtex-7 FPGAs Device Diagrams, page 166

The figures provide a top-view perspective.

The symbols for the multi-function I/O pins are represented by only one of the available pin functions; with precedence (by functionality) in this order:

- ADV_B, FCS_B, FOE_B, MOSI, FWE_B, DOUT_CSO_B, CSI_B, PUDC_B, or RDWR_B
- RS0–RS1
- AD0P, AD0N–AD15P, AD15N
- EMCCLK
- VRN, VRP, or VREF
- D00–D31
- A00–A28
- DQS, MRCC, or SRCC

For example, a pin description such as IO_L8P_SRCC_12 is represented with a SRCC symbol, a pin description such as IO_L19N_T3_A09_D25_VREF_14 is represented with a VREF symbol, and a pin description such as IO_L21N_T3_DQS_A06_D22_14 is represented with a D0–D31 symbol.

Note: For brevity, the prefixes for Xilinx commercial (XC) devices are used when the defense-grade (XQ) or the automotive (XA) could also be available.

Spartan-7 FPGAs Device Diagrams

Table 3-1: **Spartan-7 FPGAs Device Diagrams Cross-Reference**

Device	CPGA196	CSGA225	CSGA324	FTGB196	FGGA484	FGGA676
XC7S6	page 73	page 79		page 75		
XC7S15	page 73	page 79		page 75		
XC7S25		page 81	page 83	page 77		
XC7S50			page 85	page 77	page 87	
XC7S75					page 89	page 92
XC7S100					page 89	page 92

CPGA196 Package—XC7S6 and XC7S15

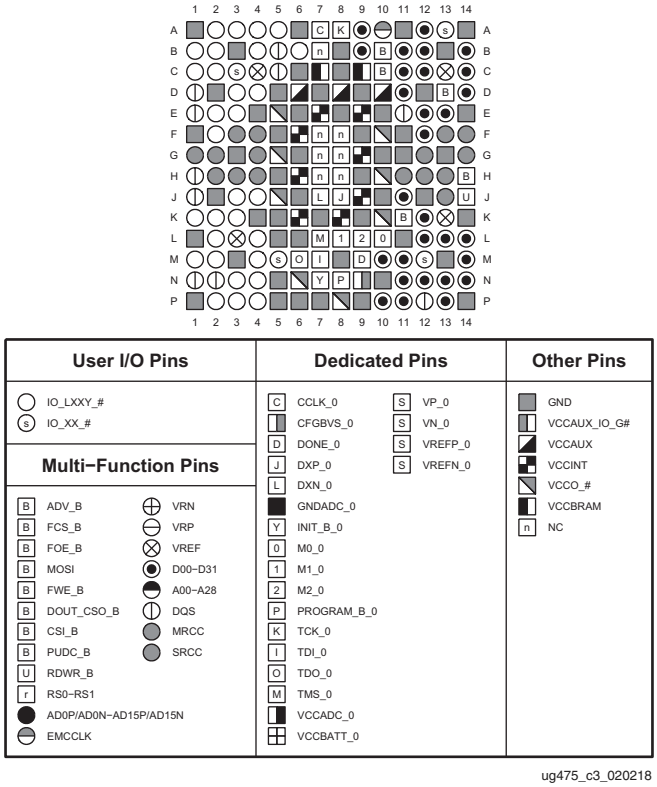


Figure 3-1: **CPGA196 Package—XC7S6 and XC7S15 Pinout Diagram**

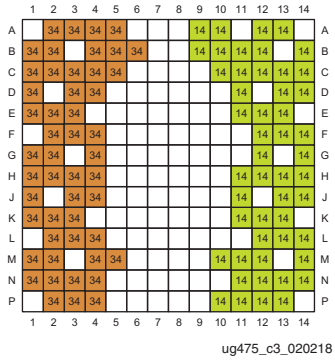


Figure 3-2: **CPGA196 Package—XC7S6 and XC7S15 I/O Banks**

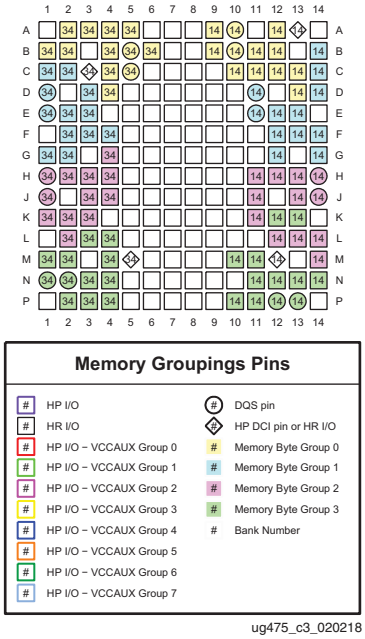


Figure 3-3: **CPGA196 Package—XC7S6 and XC7S15 Memory Groupings**

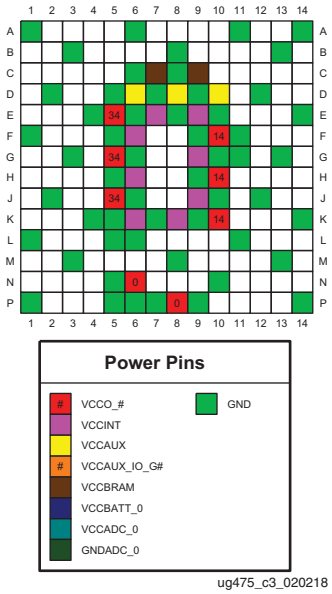


Figure 3-4: **CPGA196 Package—XC7S6 and XC7S15 Power and GND Placement**

FTGB196 Package—XC7S6 and XC7S15

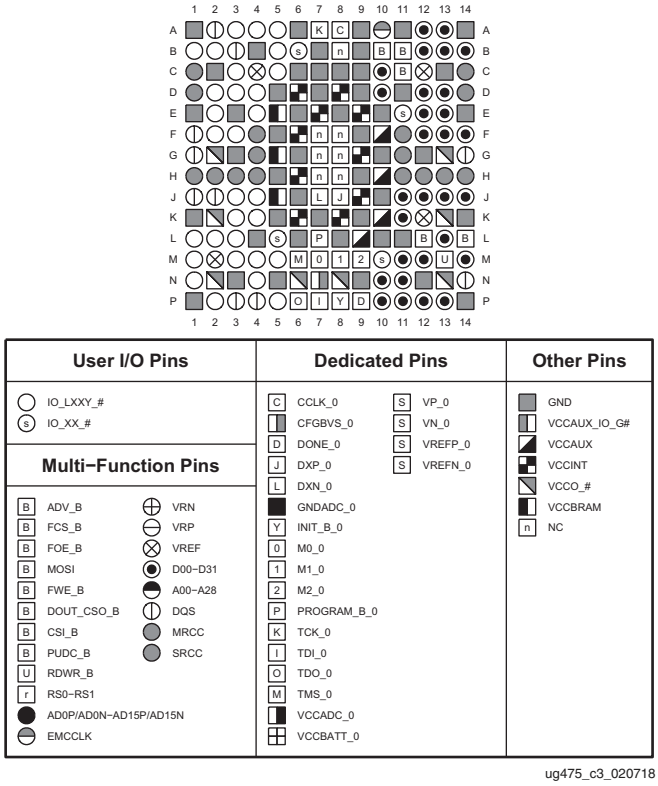


Figure 3-5: **FTGB196 Package—XC7S6 and XC7S15 Pinout Diagram**

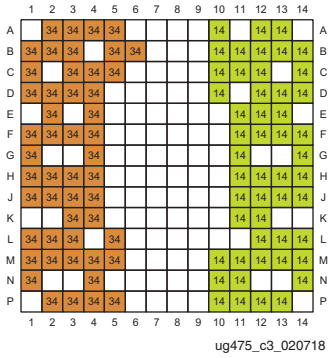


Figure 3-6: **FTGB196 Package—XC7S6 and XC7S15 I/O Banks**

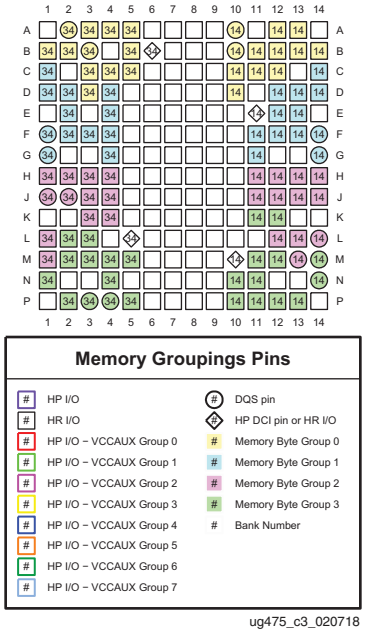


Figure 3-7: **FTGB196 Package—XC7S6 and XC7S15 Memory Groupings**

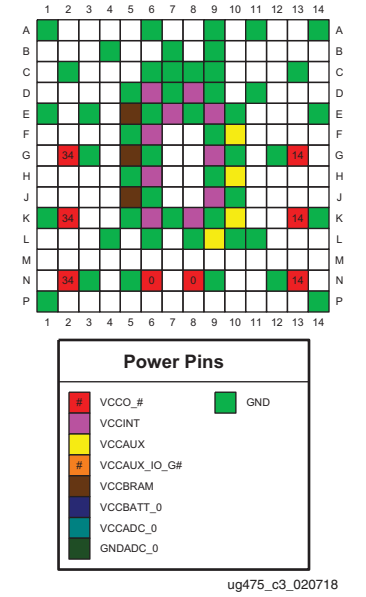


Figure 3-8: **FTGB196 Package—XC7S6 and XC7S15 Power and GND Placement**

FTGB196 Package—XC7S25 and XC7S50

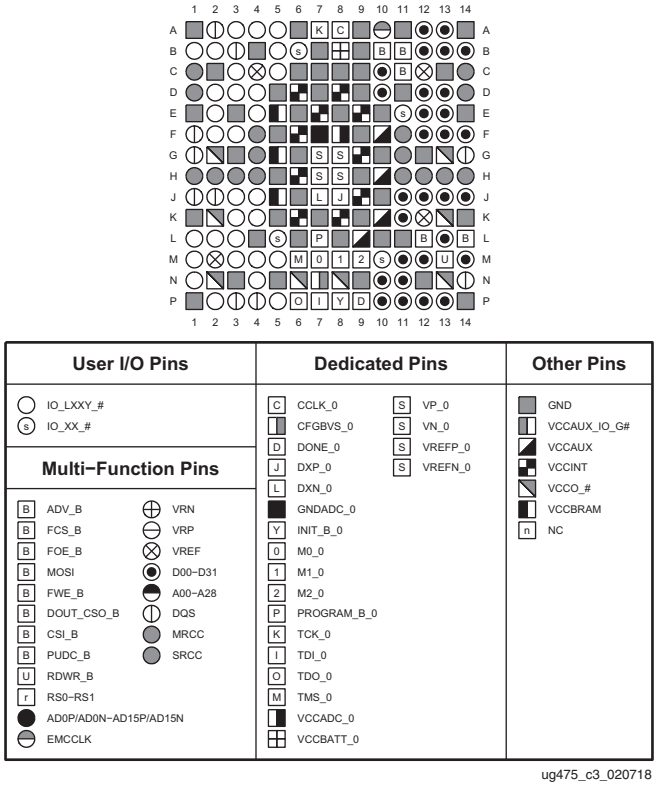


Figure 3-9: **FTGB196 Package—XC7S25 and XC7S50 Pinout Diagram**

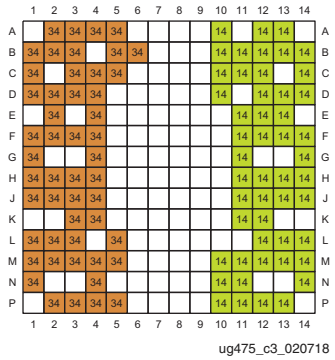


Figure 3-10: **FTGB196 Package—XC7S25 and XC7S50 I/O Banks**

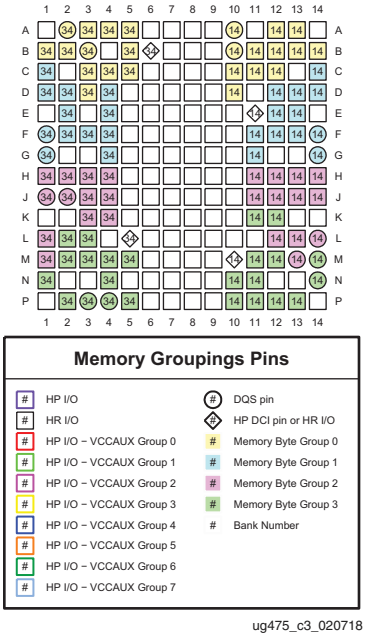


Figure 3-11: **FTGB196 Package—XC7S25 and XC7S50 Memory Groupings**

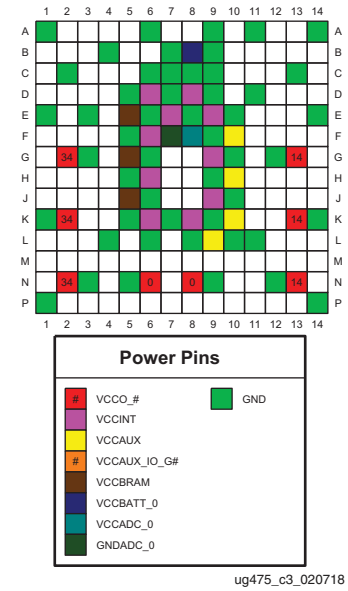


Figure 3-12: **FTGB196 Package—XC7S25 and XC7S50 Power and GND Placement**

CSGA225 Package—XC7S6 and XC7S15

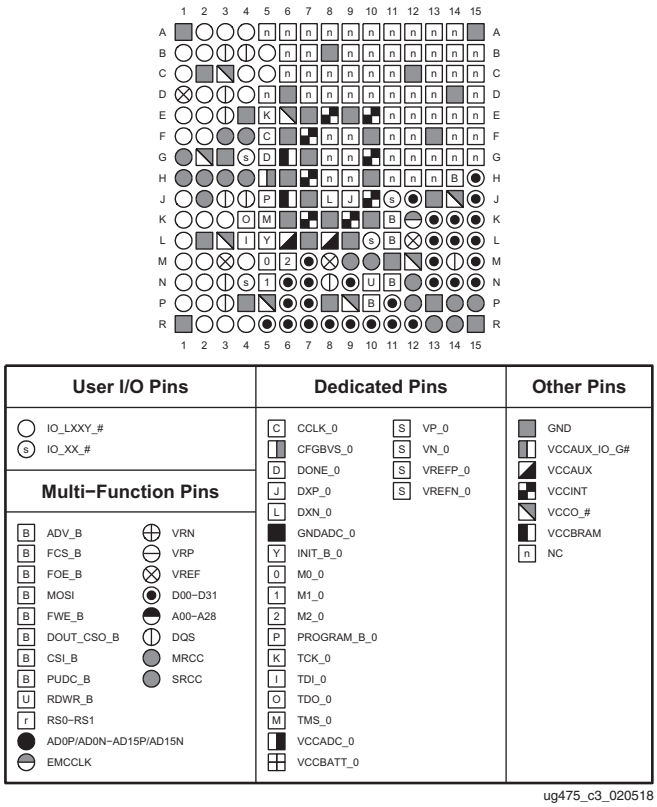


Figure 3-13: **CSGA225 Package—XC7S6 and XC7S15 Pinout Diagram**

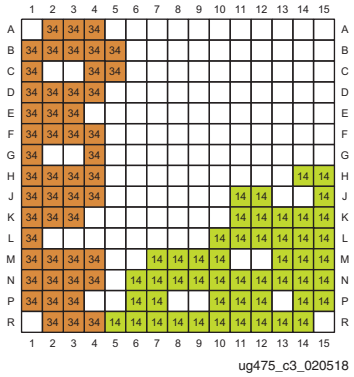


Figure 3-14: **CSGA225 Package—XC7S6 and XC7S15 I/O Banks**

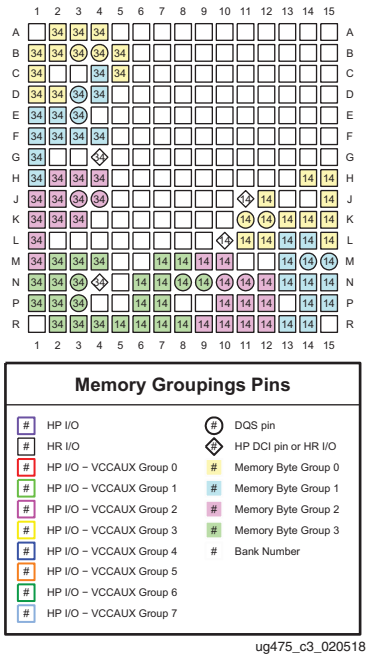


Figure 3-15: **CSGA225 Package—XC7S6 and XC7S15 Memory Groupings**

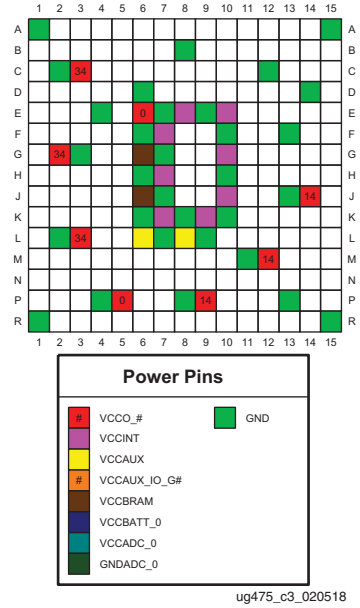


Figure 3-16: **CSGA225 Package—XC7S6 and XC7S15 Power and GND Placement**

CSGA225 Package—XC7S25

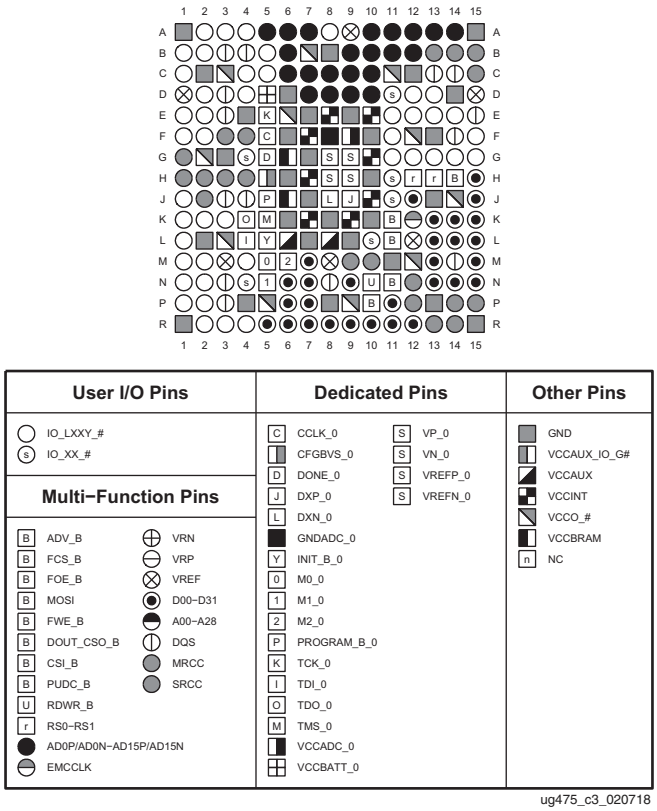


Figure 3-17: **CSGA225 Package—XC7S25 Pinout Diagram**

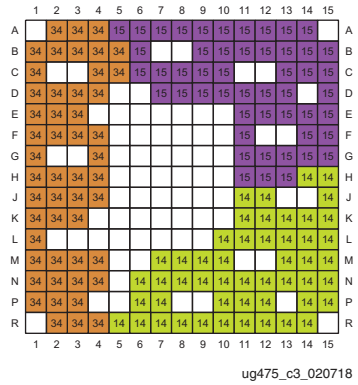


Figure 3-18: **CSGA225 Package—XC7S25 I/O Banks**

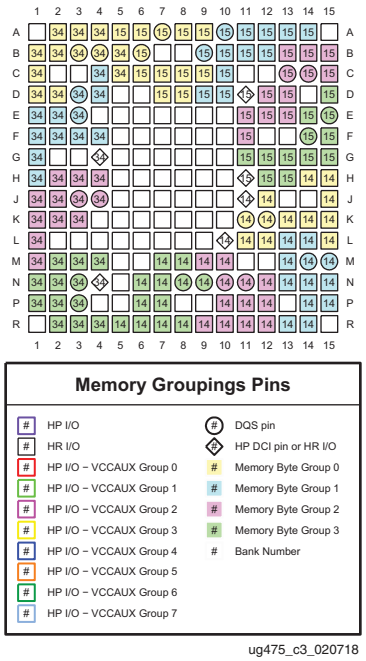


Figure 3-19: **CSGA225 Package—XC7S25 Memory Groupings**

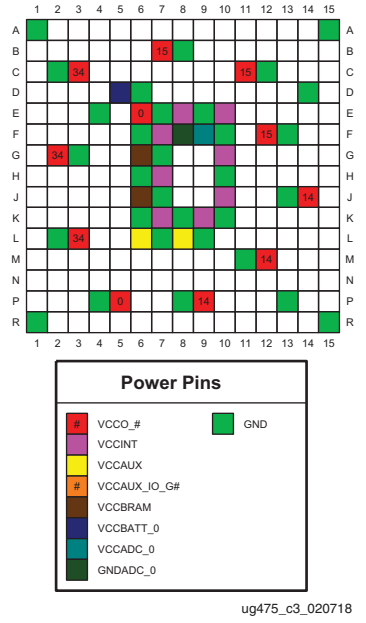


Figure 3-20: **CSGA225 Package—XC7S25 Power and GND Placement**

CSGA324 Package—XC7S25

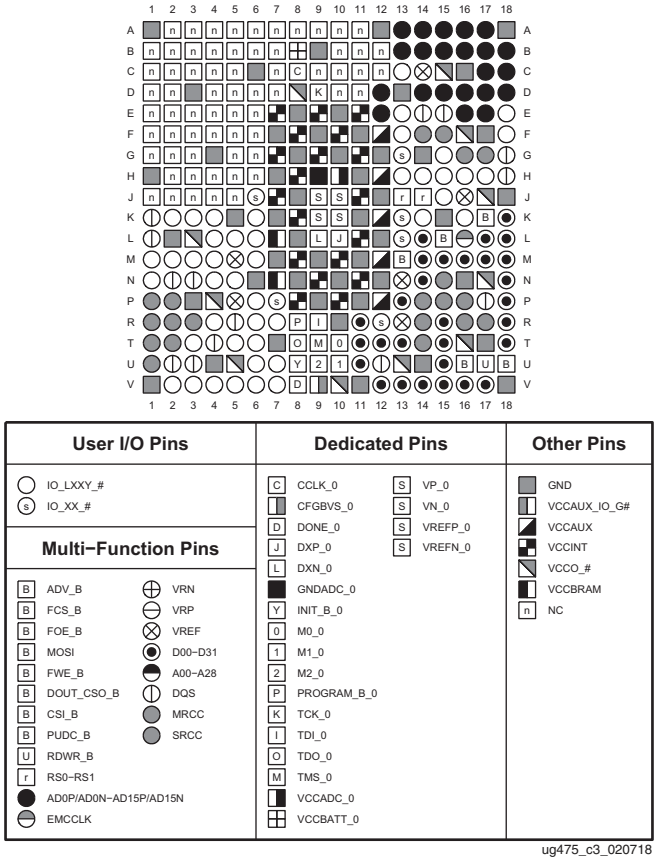


Figure 3-21: **CSGA324 Package—XC7S25 Pinout Diagram**

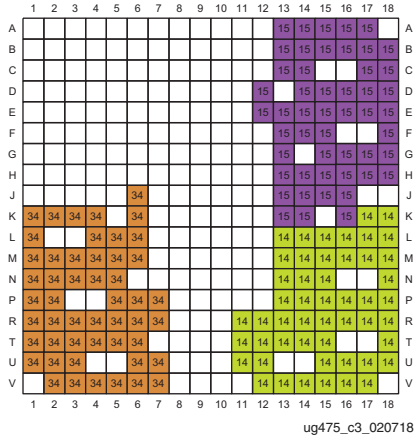


Figure 3-22: **CSGA324 Package—XC7S25 I/O Banks**

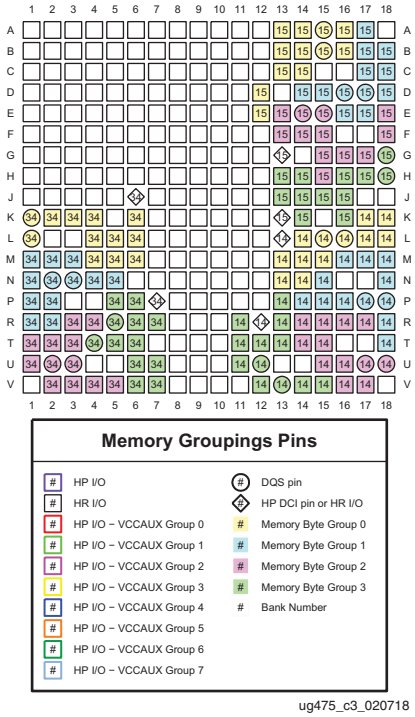


Figure 3-23: **CSGA324 Package—XC7S25 Memory Groupings**

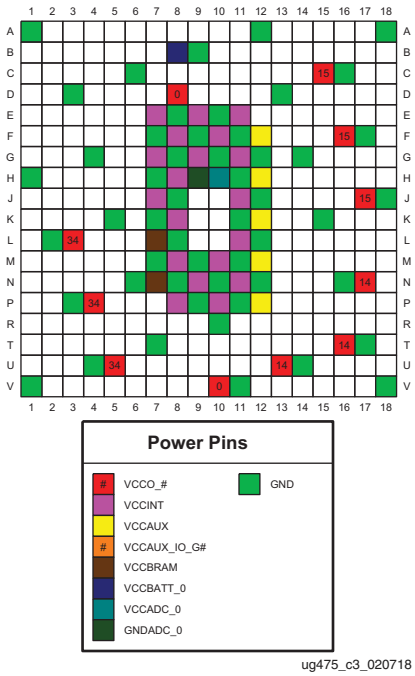


Figure 3-24: **CSGA324 Package—XC7S25 Power and GND Placement**

CSGA324 Package—XC7S50

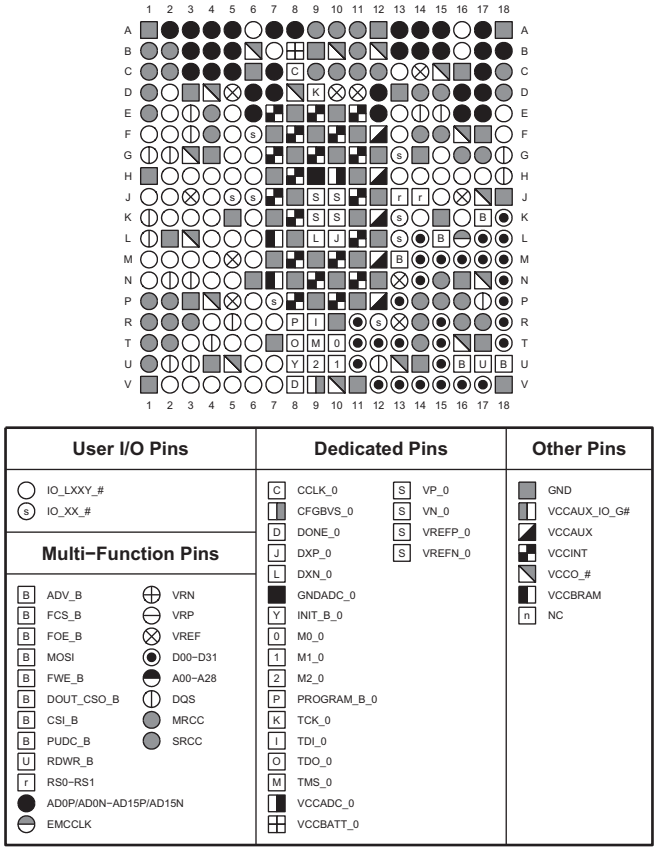


Figure 3-25: **CSGA324 Package—XC7S50 Pinout Diagram**

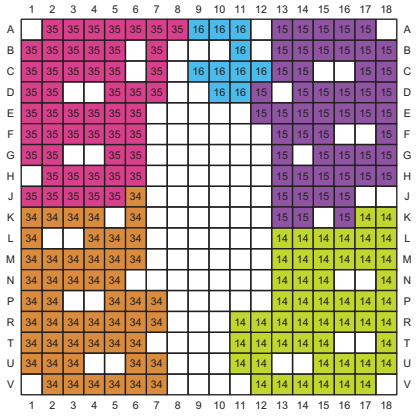


Figure 3-26: **CSGA324 Package—XC7S50 I/O Banks**

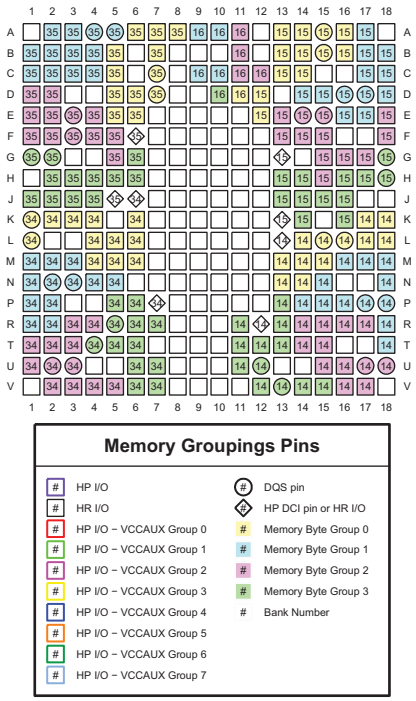


Figure 3-27: **CSGA324 Package—XC7S50 Memory Groupings**

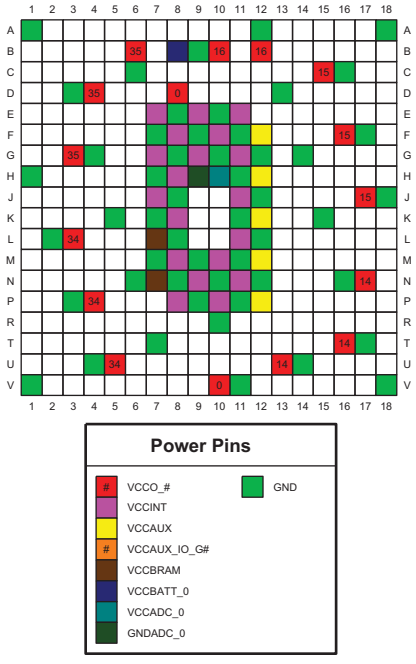


Figure 3-28: **CSGA324 Package—XC7S50 Power and GND Placement**

FGGA484 Package—XC7S50

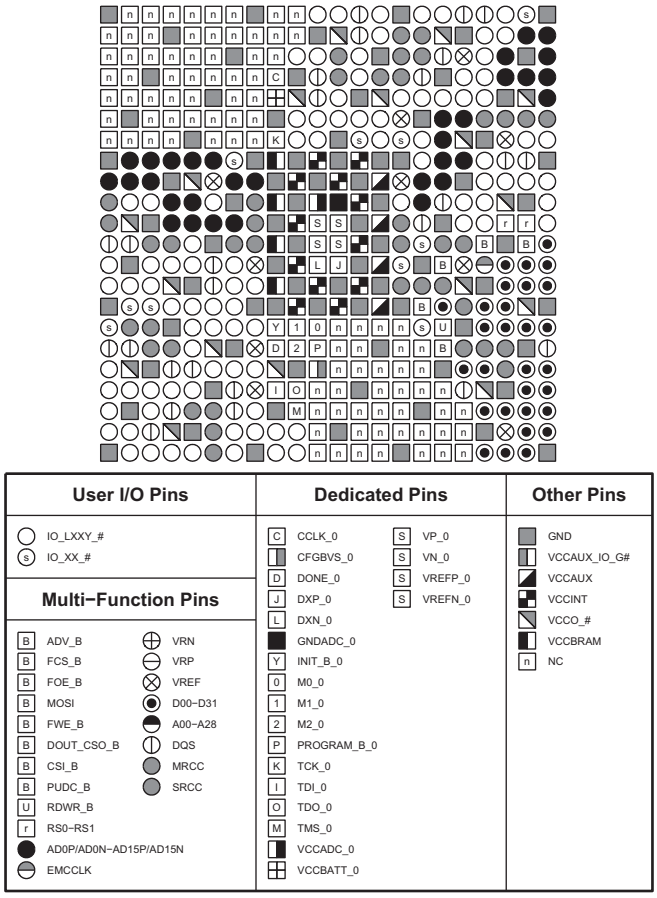


Figure 3-29: **FGGA484 Package—XC7S50 Pinout Diagram**

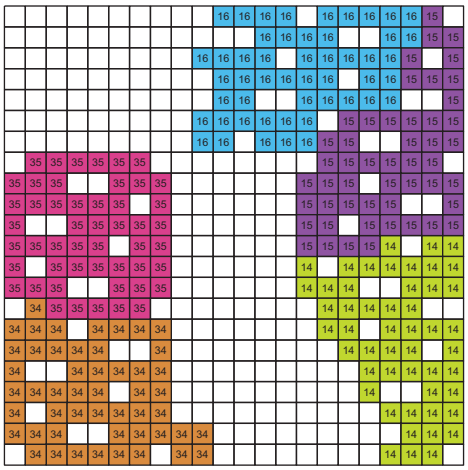


Figure 3-30: **FGGA484 Package—XC7S50 I/O Banks**

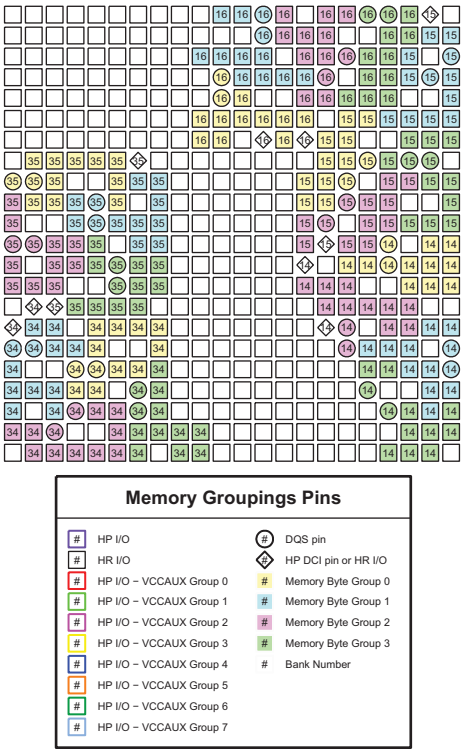


Figure 3-31: **FGGA484 Package—XC7S50 Memory Groupings**

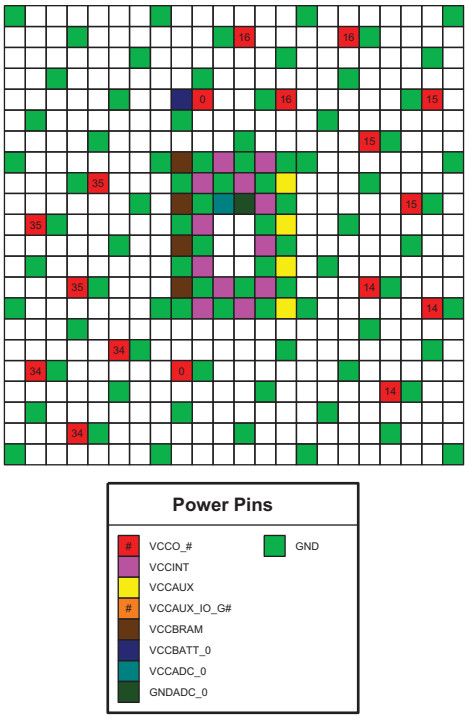


Figure 3-32: **FGGA484 Package—XC7S50 Power and GND Placement**

FGGA484 Package—XC7S75 and XC7S100

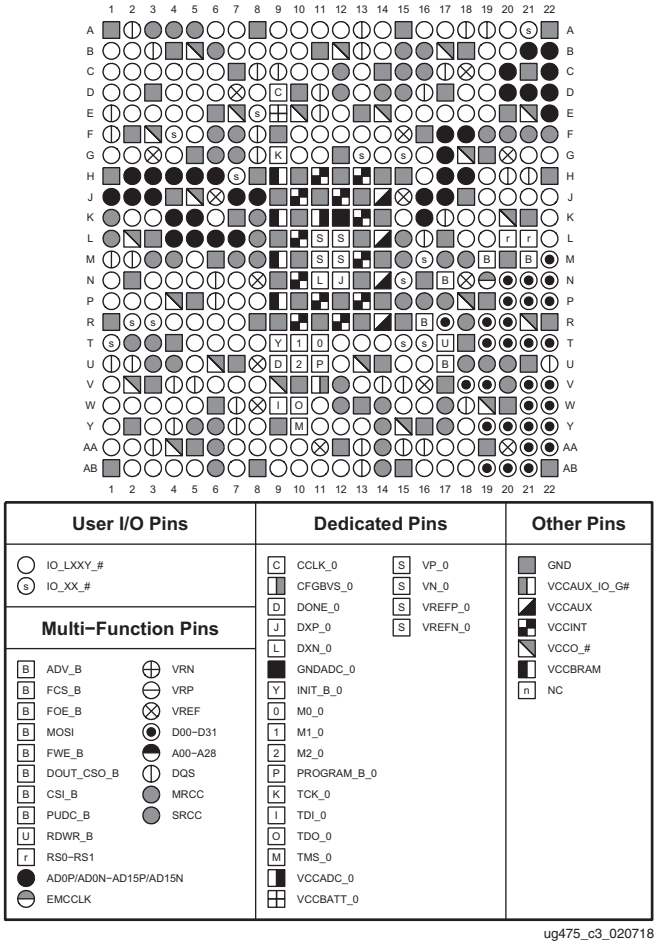


Figure 3-33: **FGGA484 Package—XC7S75 and XC7S100 Pinout Diagram**

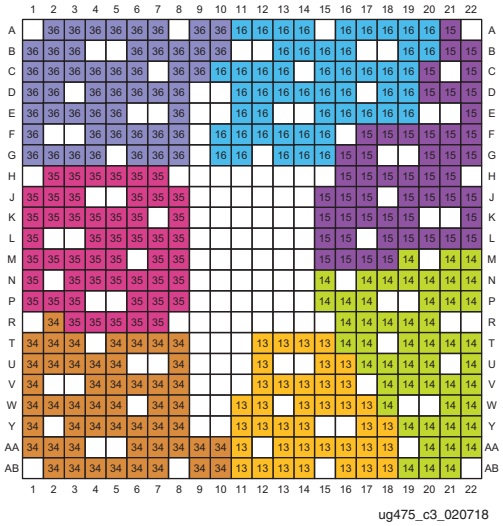


Figure 3-34: **FGGA484 Package—XC7S75 and XC7S100 I/O Banks**

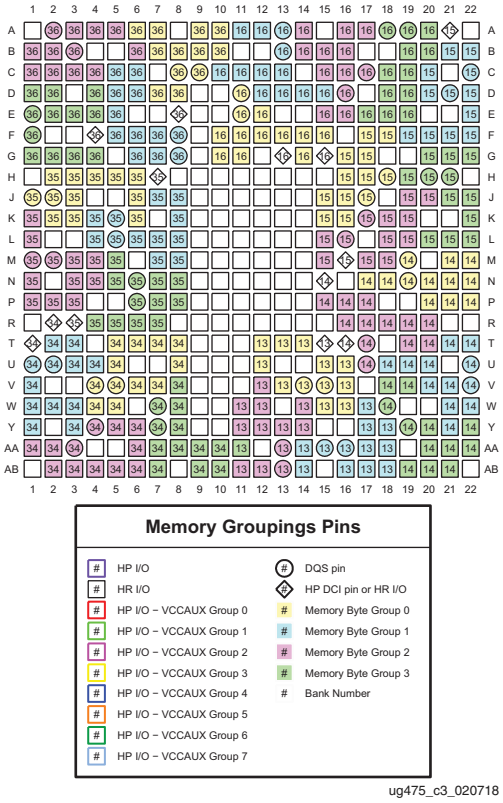


Figure 3-35: **FGGA484 Package—XC7S75 and XC7S100 Memory Groupings**

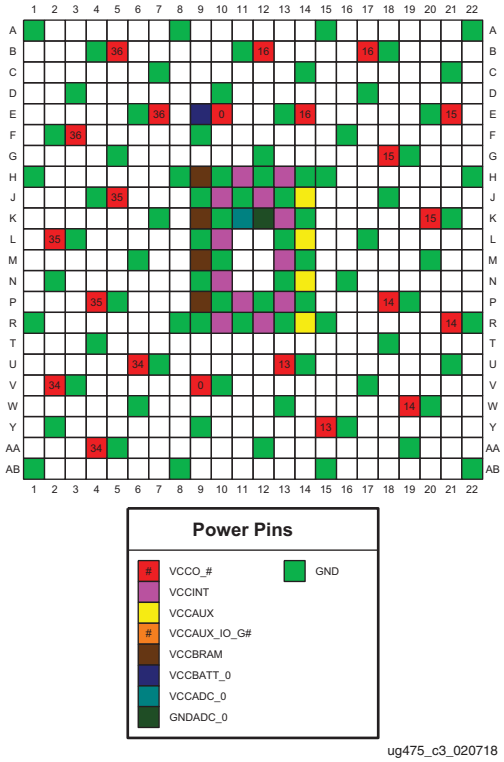


Figure 3-36: **FGGA484 Package—XC7S75 and XC7S100 Power and GND Placement**

FGGA676 Package—XC7S75 and XC7S100

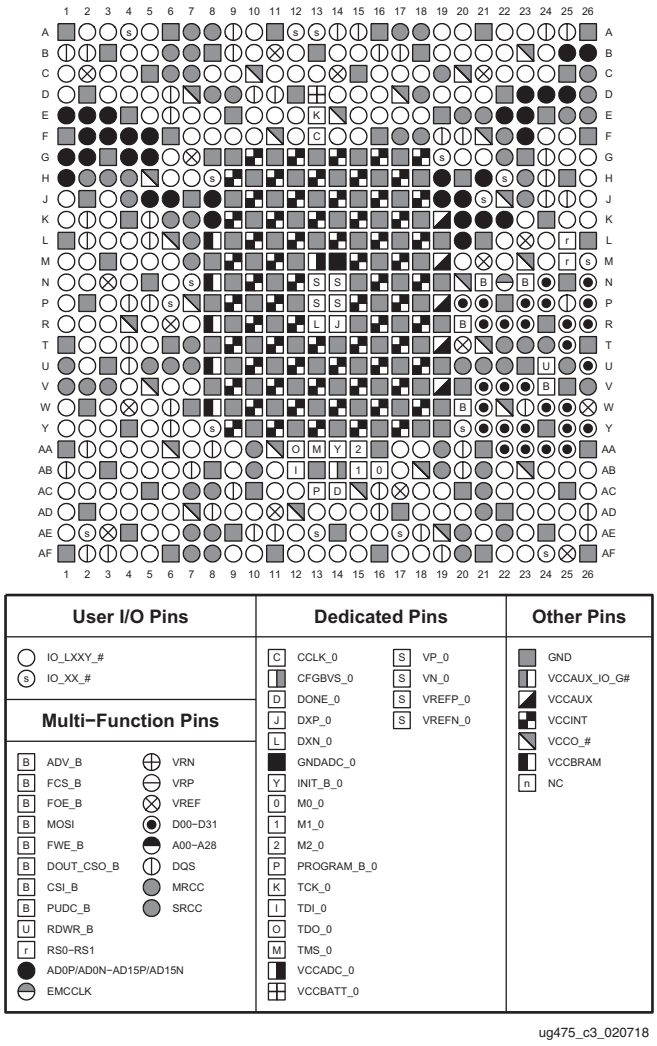


Figure 3-37: **FGGA676 Package—XC7S75 and XC7S100 Pinout Diagram**

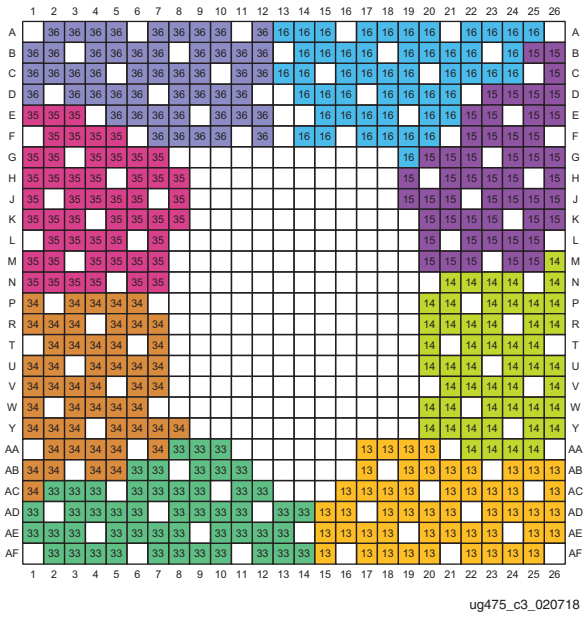


Figure 3-38: **FGGA676 Package—XC7S75 and XC7S100 I/O Banks**

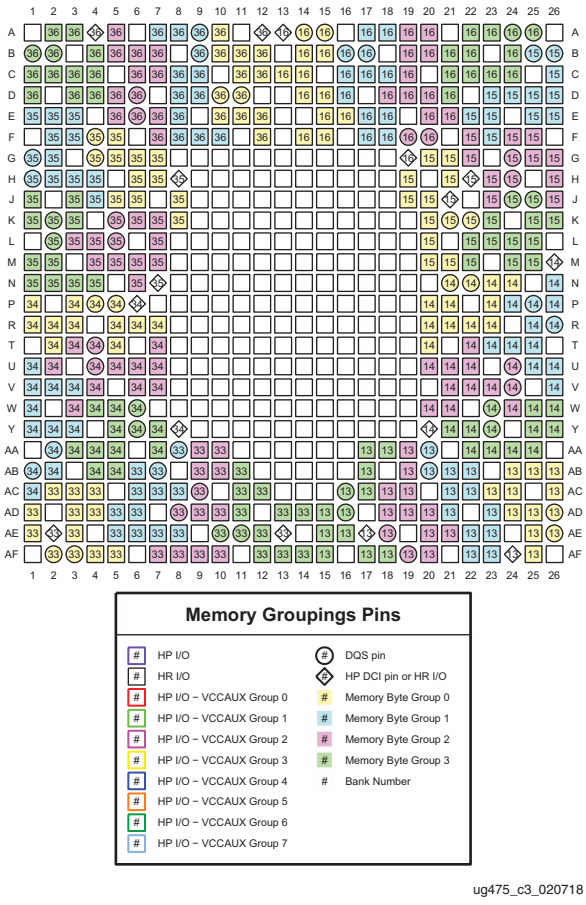


Figure 3-39: **FGGA676 Package—XC7S75 and XC7S100 Memory Groupings**

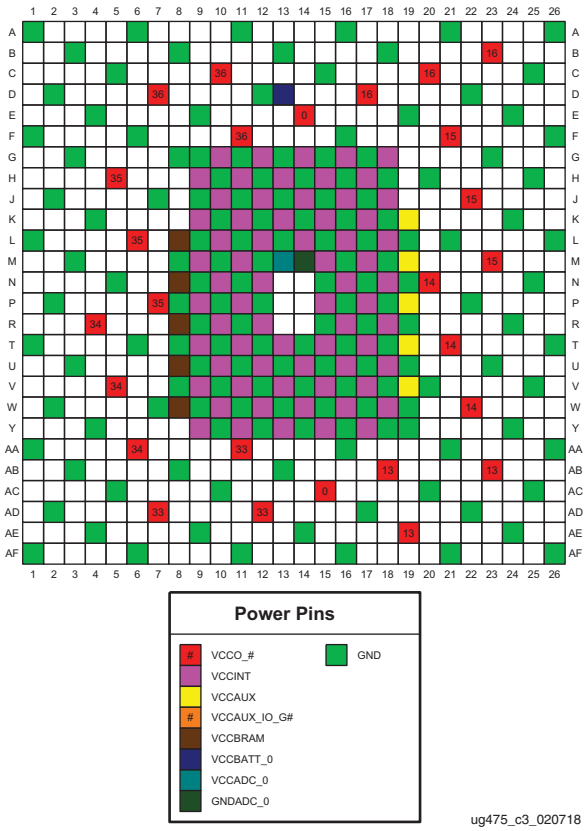


Figure 3-40: **FGGA676 Package—XC7S75 and XC7S100 Power and GND Placement**

Artix-7 FPGAs Device Diagrams

Table 3-2: **Artix-7 FPGAs Device Diagrams Cross-Reference**(1)

Device	CP236 CPG236	CPG238	CS324 CSG324	CS325 CSG325	FT256 FTG256	SB484 SBG484 SBV484 RS484	FG484 FGG484	FG676 FGG676	FB484 FBG484 RB484	FB676 FBG676 RB676	FF1156 FFG1156
XC7A12T		page 98		page 102							
XC7A15T	page 96		page 100	page 106	page 108		page 110				
XC7A25T		page 98		page 104							
XC7A35T	page 96		page 100	page 106	page 108		page 110				
XC7A50T	page 96		page 100	page 106	page 108		page 110				
XC7A75T			page 100		page 108		page 113	page 116			
XC7A100T			page 100		page 108		page 113	page 116			
XC7A200T						page 119			page 122	page 125	page 128

Notes:

1. FGG676, FBG676 and FGG484, FBG484 packages are pin compatible.

CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T

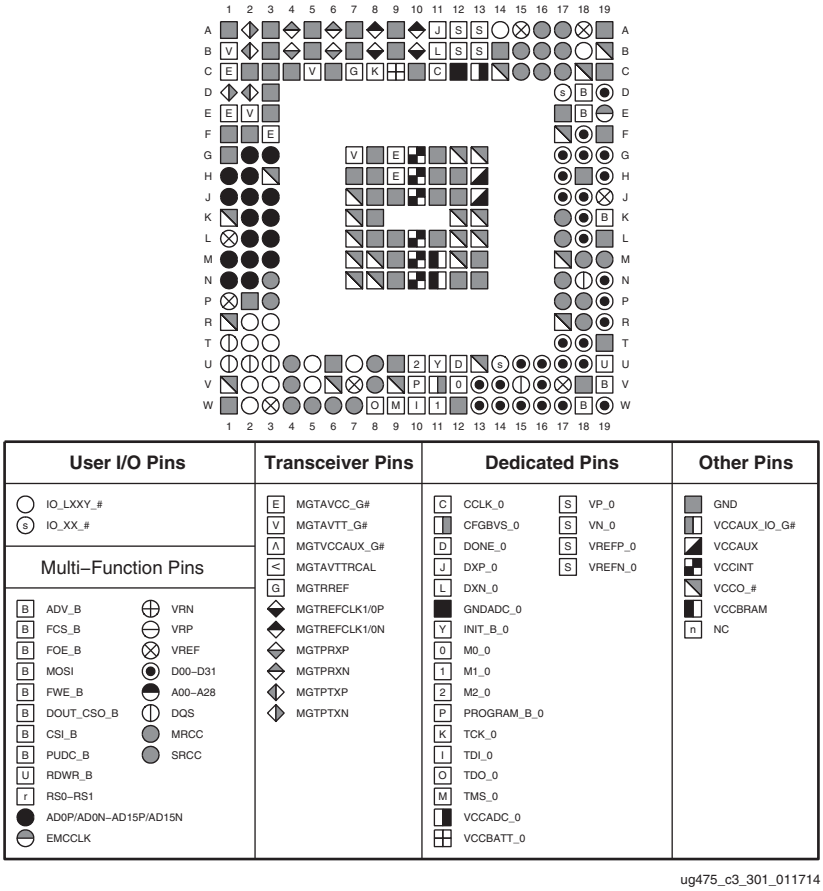


Figure 3-41: **CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T Pinout Diagram**

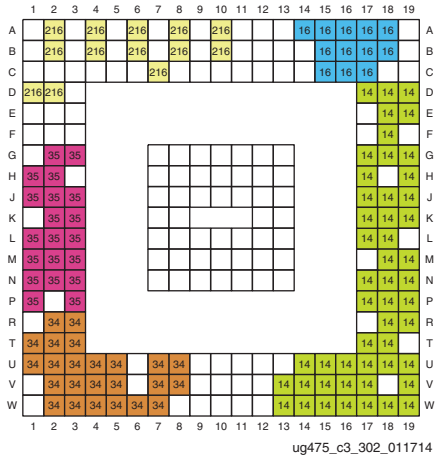


Figure 3-42: **CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T I/O Banks**

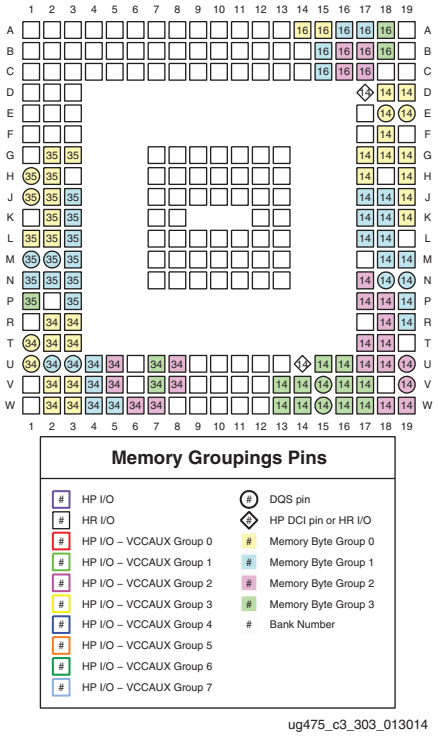


Figure 3-43: **CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T Memory Groupings**

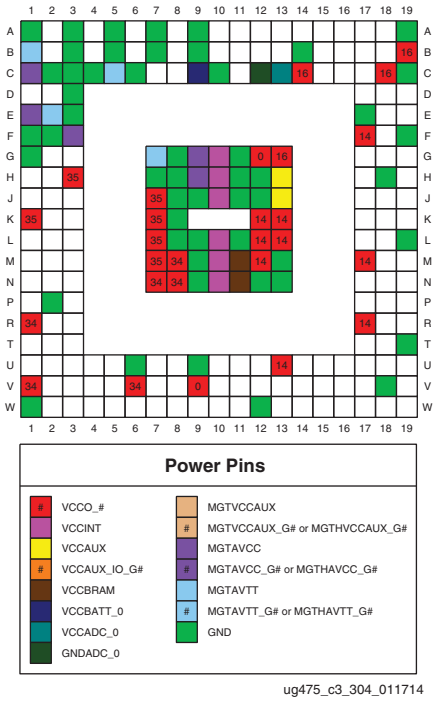


Figure 3-44: **CP236 and CPG236 Packages—XC7A15T, XC7A35T, and XC7A50T Power and GND Placement**

CPG238 Package—XC7A12T and XC7A25T

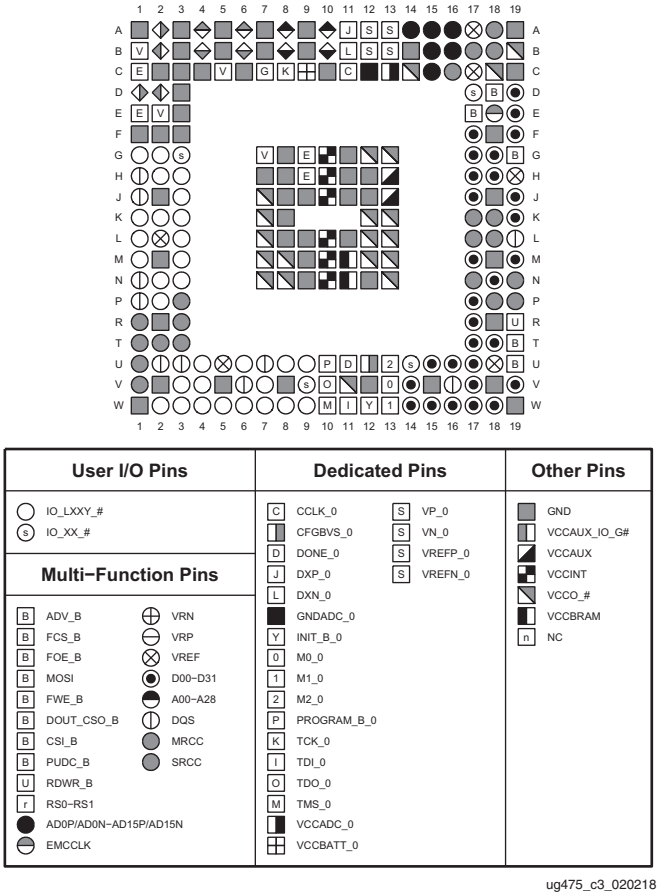


Figure 3-45: **CPG238 Package—XC7A12T and XC7A25T Pinout Diagram**

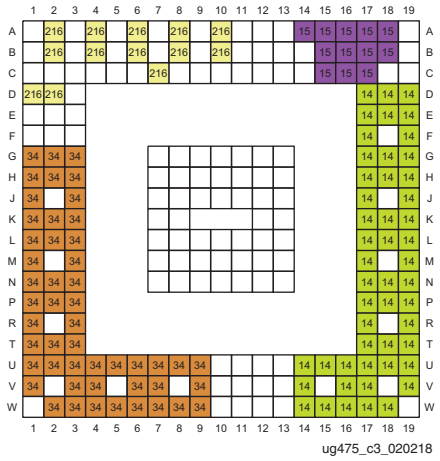


Figure 3-46: **CPG238 Package—XC7A12T and XC7A25T I/O Banks**

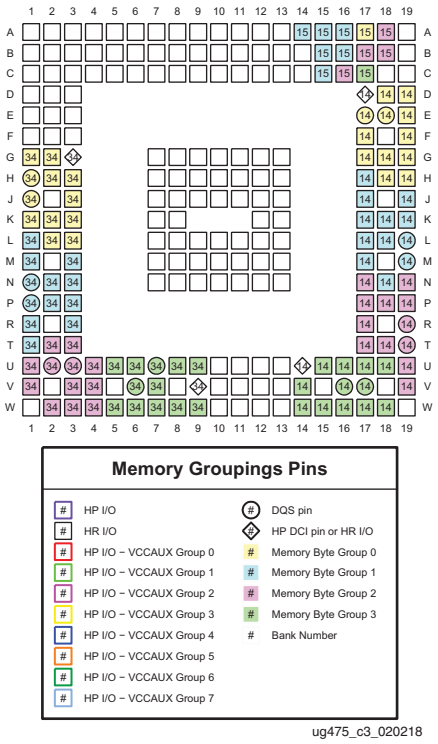


Figure 3-47: **CPG238 Package—XC7A12T and XC7A25T Memory Groupings**

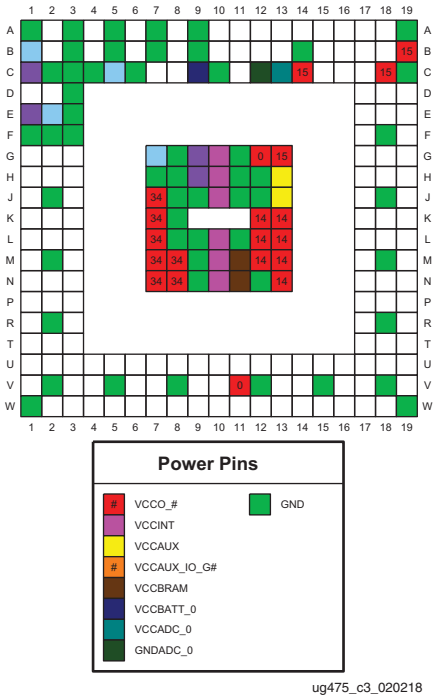


Figure 3-48: **CPG238 Package—XC7A12T and XC7A25T Power and GND Placement**

CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T

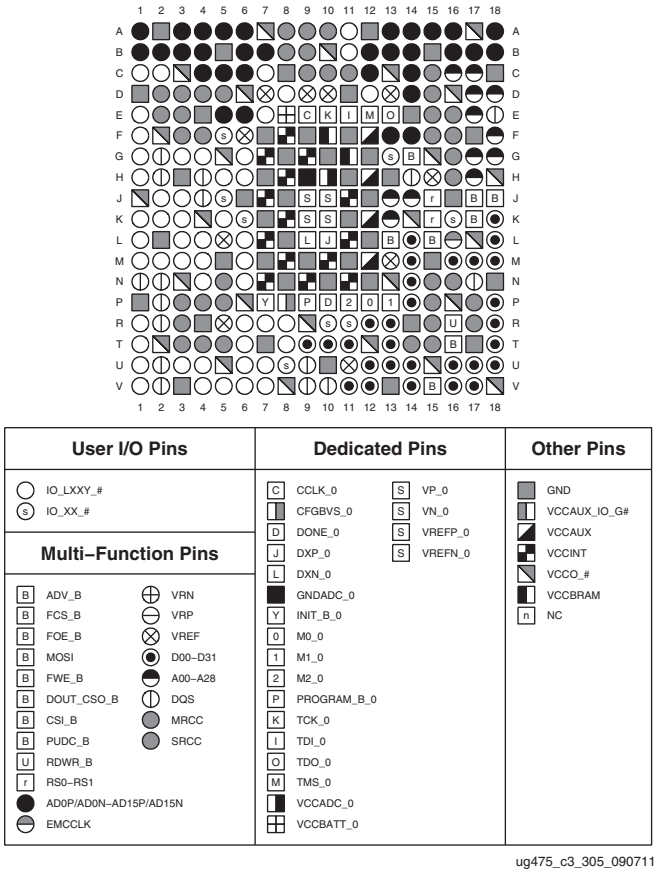


Figure 3-49: **CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Pinout Diagram**

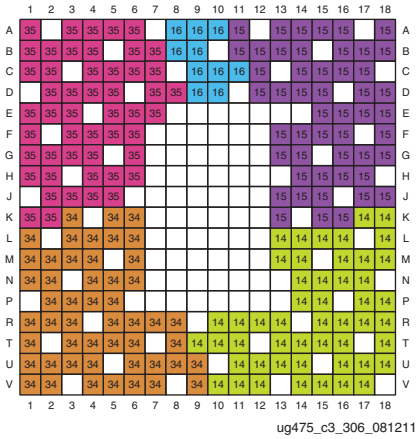


Figure 3-50: **CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T I/O Banks**

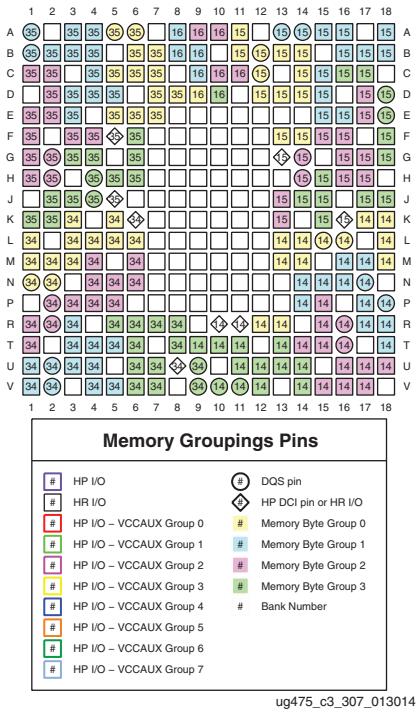


Figure 3-51: **CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Memory Groupings**

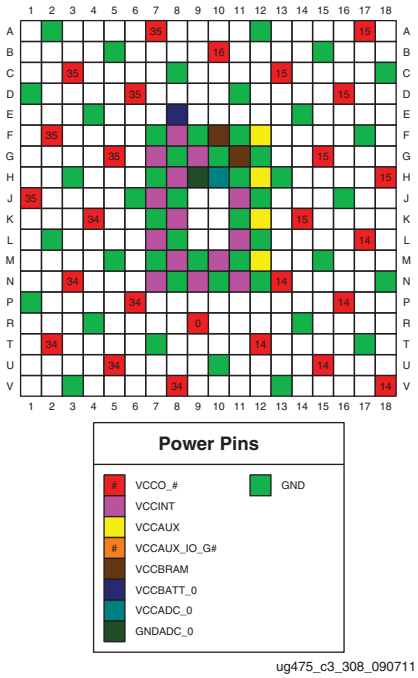


Figure 3-52: **CS324 and CSG324 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Power and GND Placement**

CSG325 Package—XC7A12T

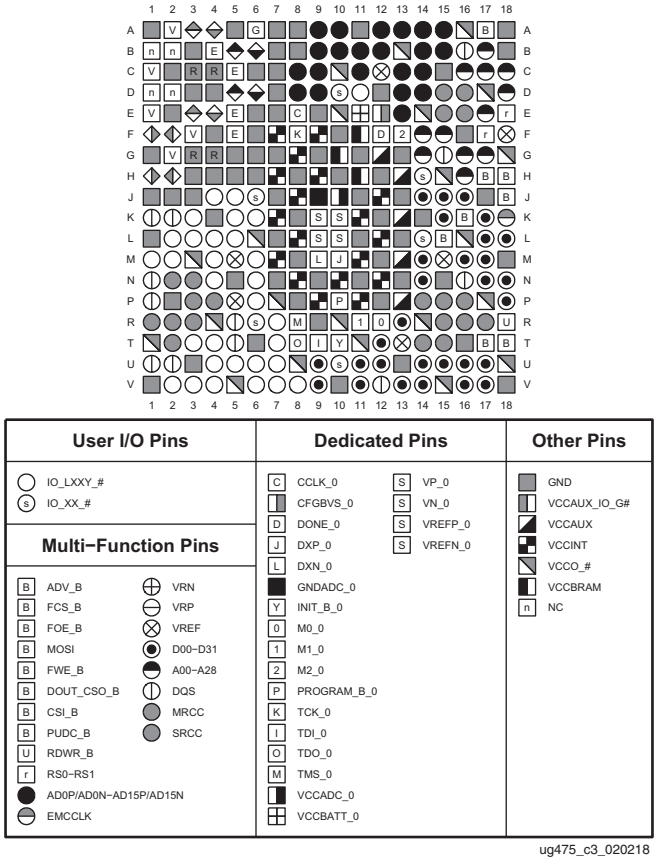


Figure 3-53: **CSG325 Package—XC7A12T Pinout Diagram**

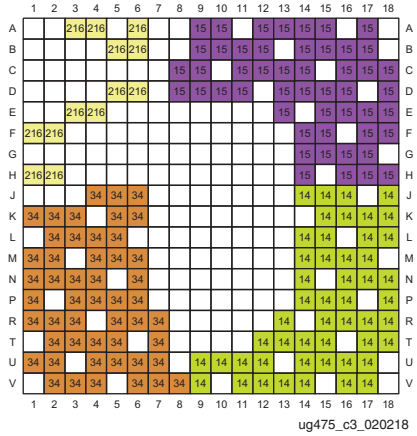


Figure 3-54: **CSG325 Package—XC7A12T I/O Banks**

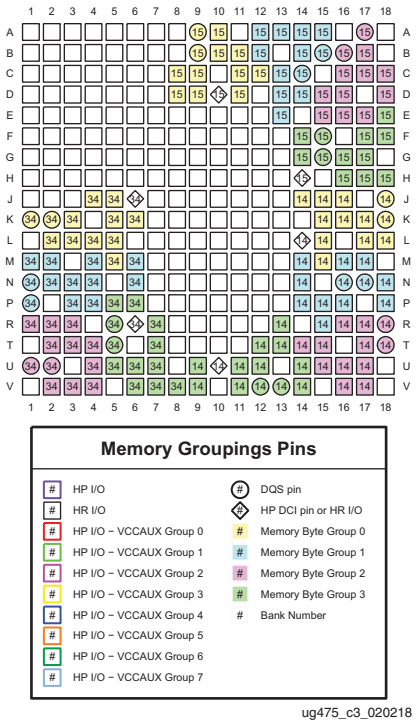


Figure 3-55: **CSG325 Package—XC7A12T Memory Groupings**

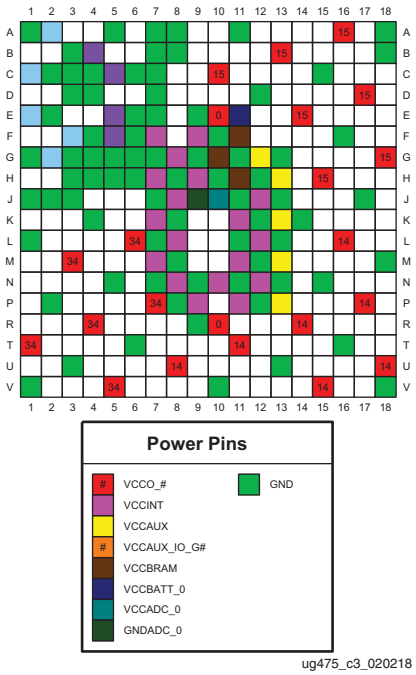


Figure 3-56: **CSG325 Package—XC7A12T Power and GND Placement**

CSG325 Package—XC7A25T

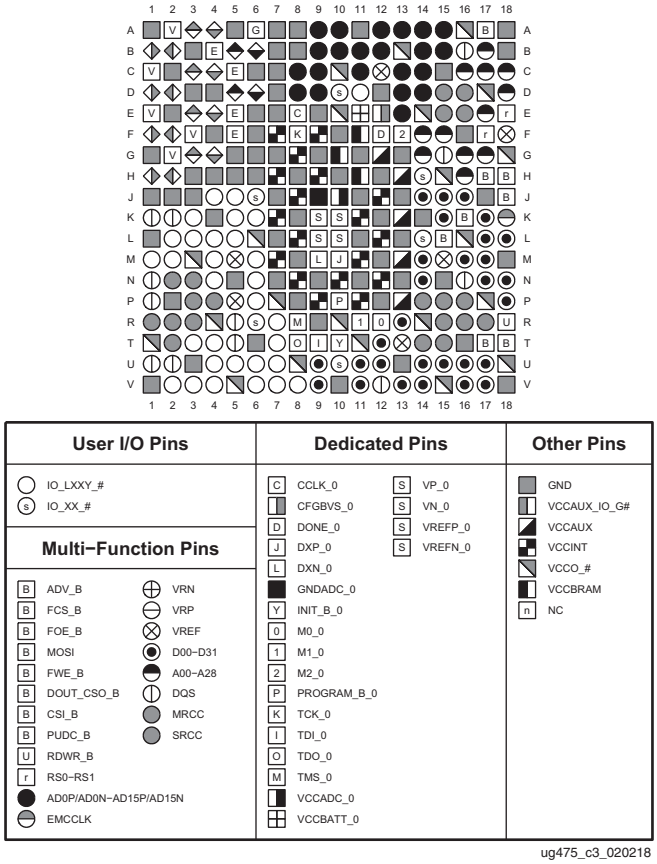


Figure 3-57: **CSG325 Package—XC7A25T Pinout Diagram**

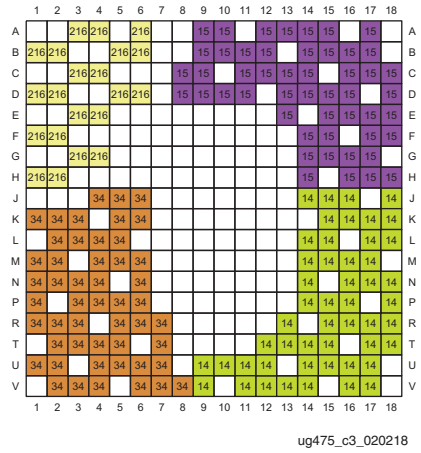


Figure 3-58: **CSG325 Package—XC7A25T I/O Banks**

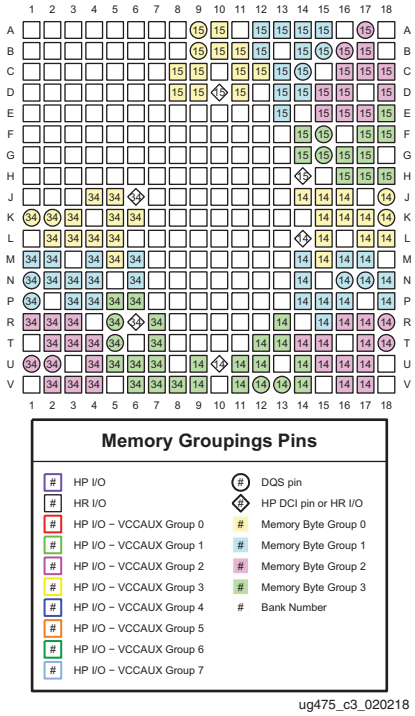


Figure 3-59: **CSG325 Package—XC7A25T Memory Groupings**

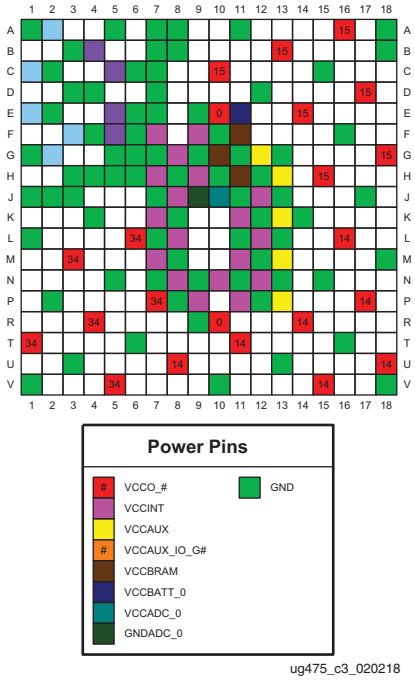


Figure 3-60: **CSG325 Package—XC7A25T Power and GND Placement**

CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T

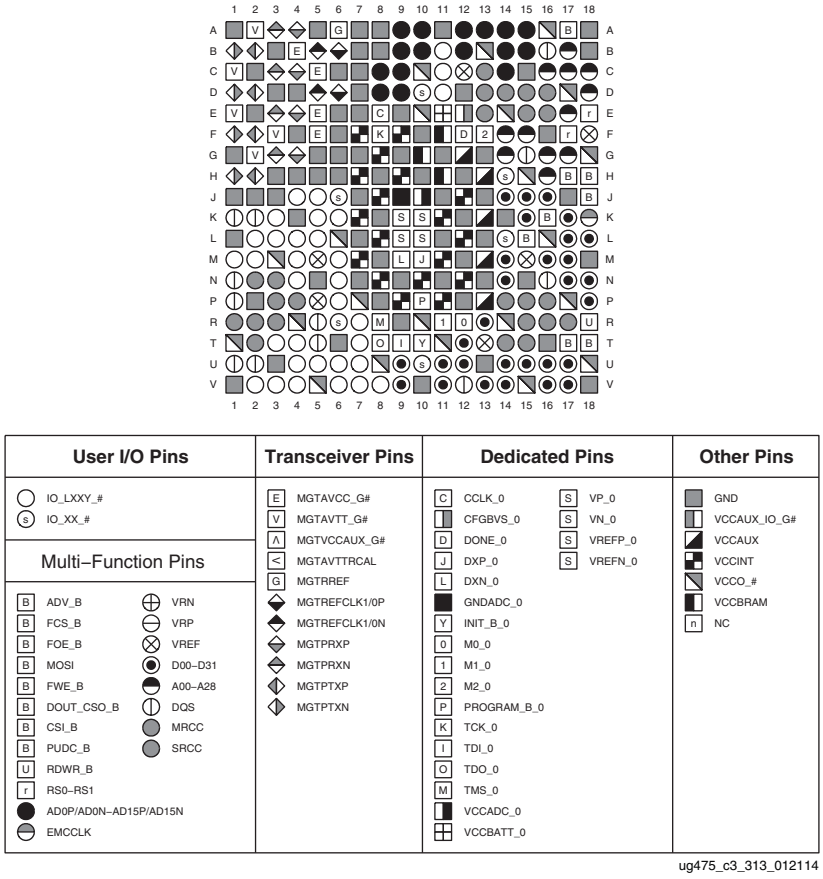


Figure 3-61: **CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T Pinout Diagram**

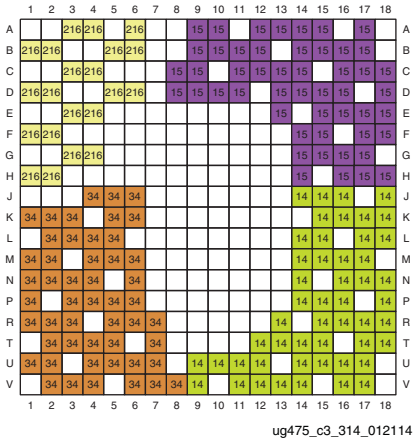


Figure 3-62: **CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T I/O Banks**

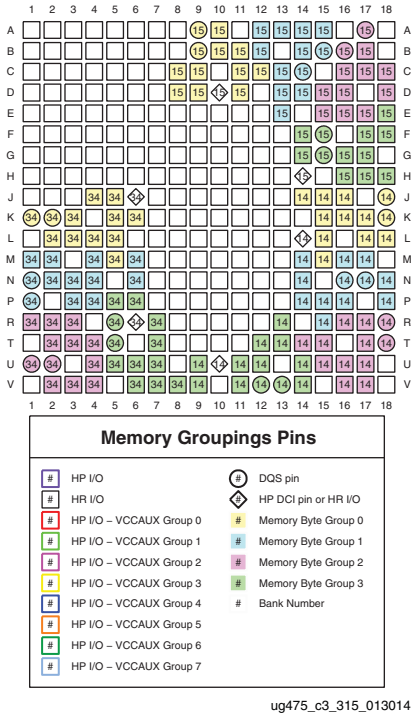


Figure 3-63: **CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T Memory Groupings**

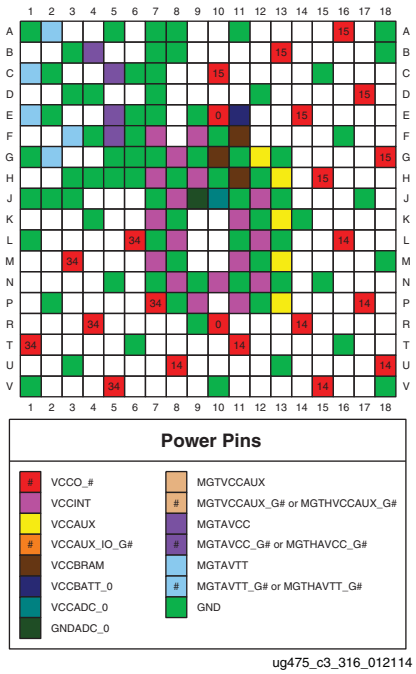


Figure 3-64: **CS325 and CSG325 Packages—XC7A15T, XC7A35T, and XC7A50T Power and GND Placement**

FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T

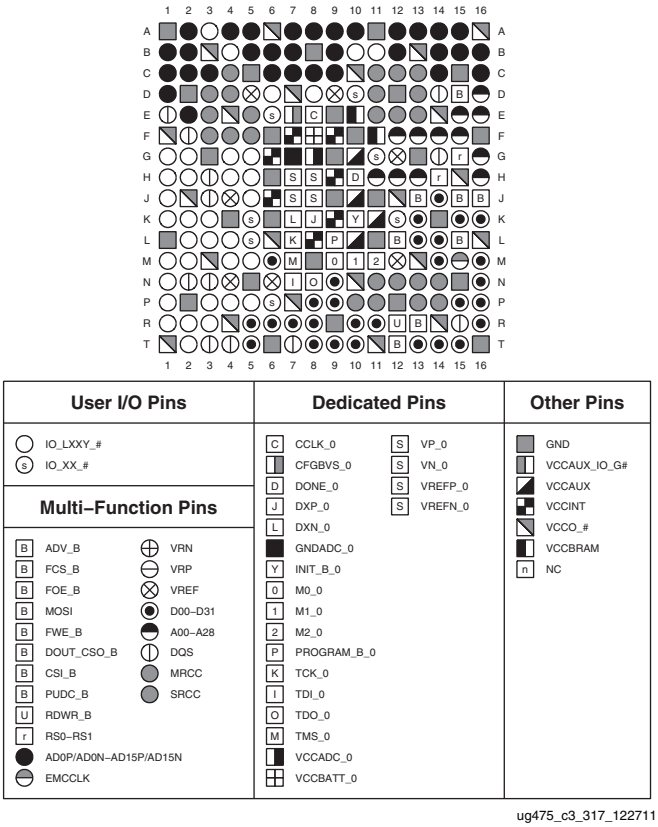


Figure 3-65: **FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Pinout Diagram**

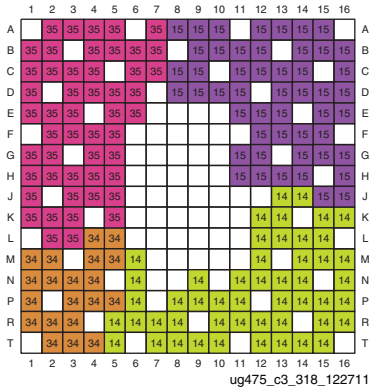


Figure 3-66: **FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T I/O Banks**

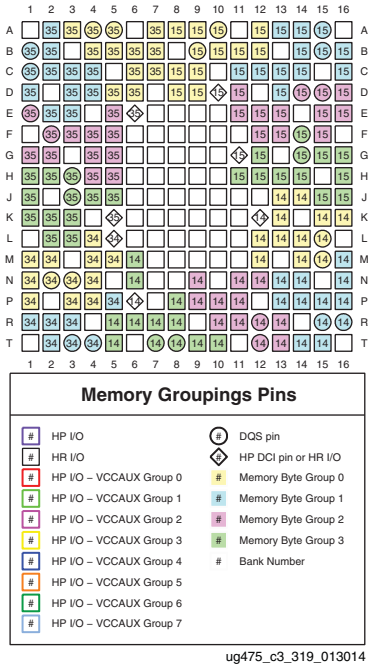


Figure 3-67: **FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Memory Groupings**

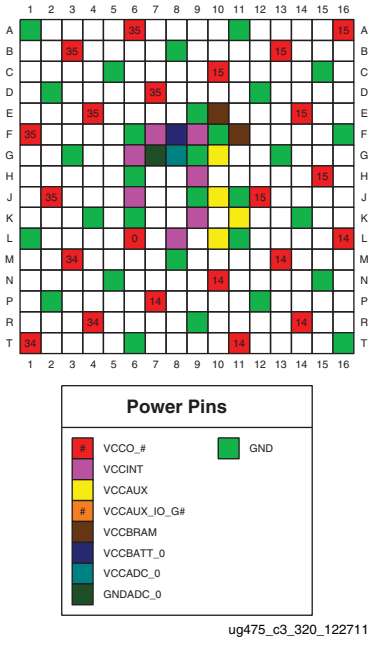


Figure 3-68: **FT256 and FTG256 Packages—XC7A15T, XC7A35T, XC7A50T, XC7A75T, and XC7A100T Power and GND Placement**

FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T

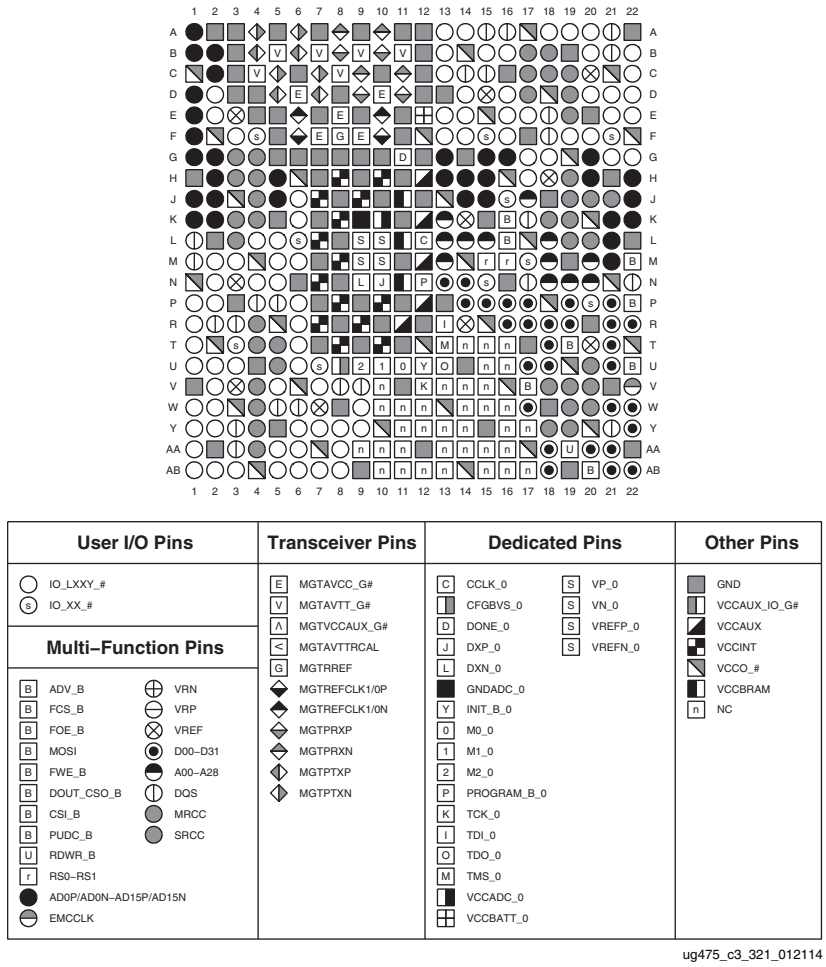


Figure 3-69: **FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T Pinout Diagram**

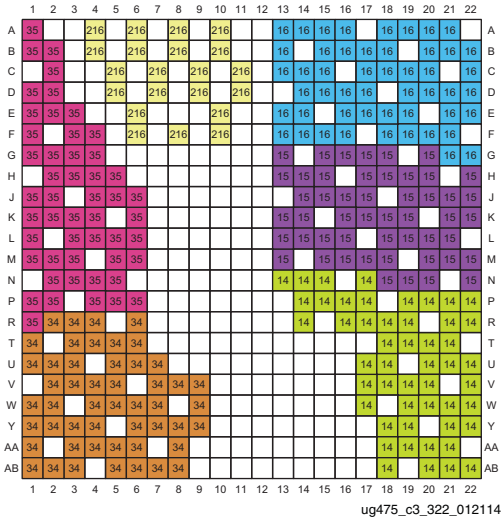


Figure 3-70: **FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T I/O Banks**

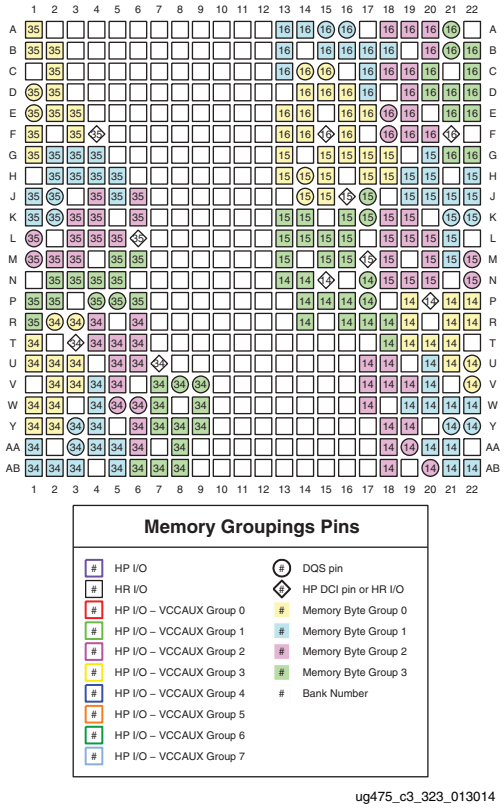


Figure 3-71: **FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T Memory Groupings**

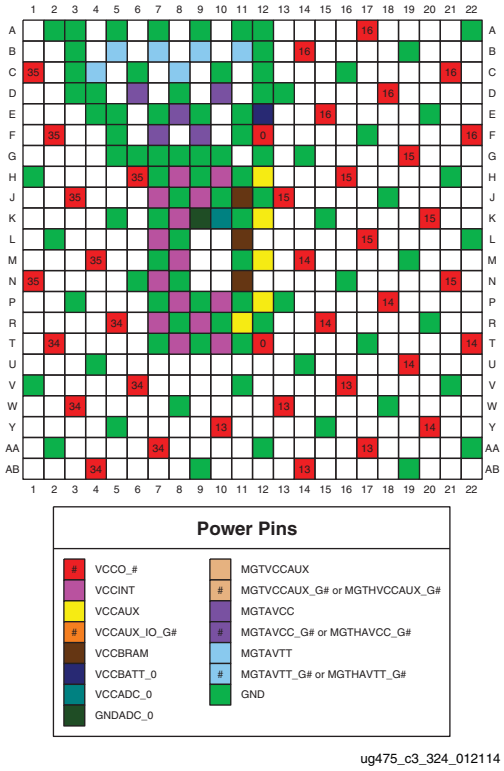


Figure 3-72: **FG484 and FGG484 Packages—XC7A15T, XC7A35T, and XC7A50T Power and GND Placement**

FG484 and FGG484 Packages—XC7A75T and XC7A100T

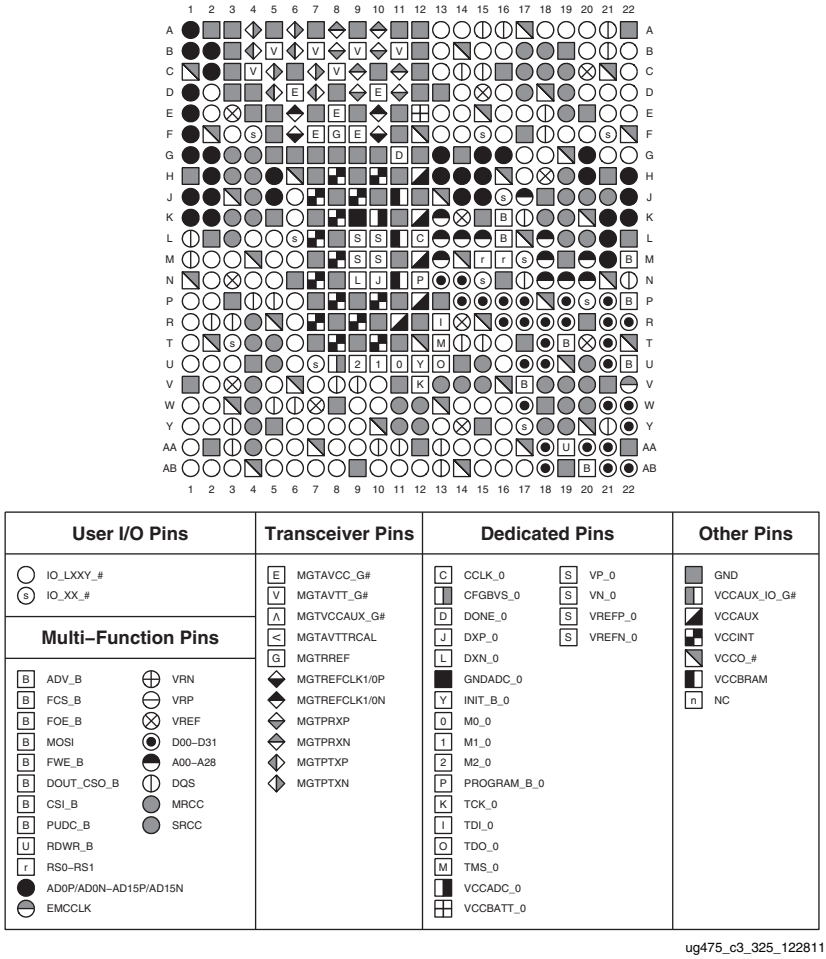


Figure 3-73: **FG484 and FGG484 Packages—XC7A75T and XC7A100T Pinout Diagram**

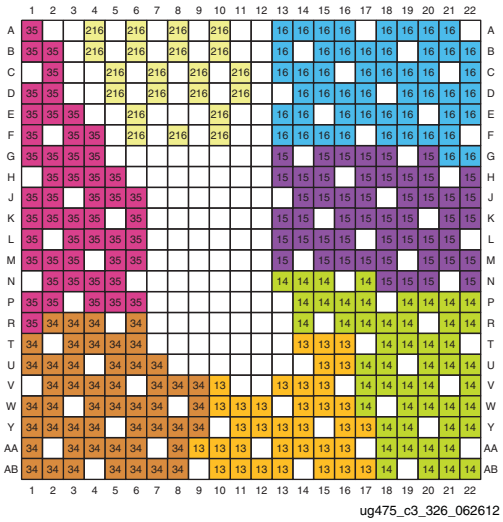


Figure 3-74: **FG484 and FGG484 Packages—XC7A75T and XC7A100T I/O Banks**

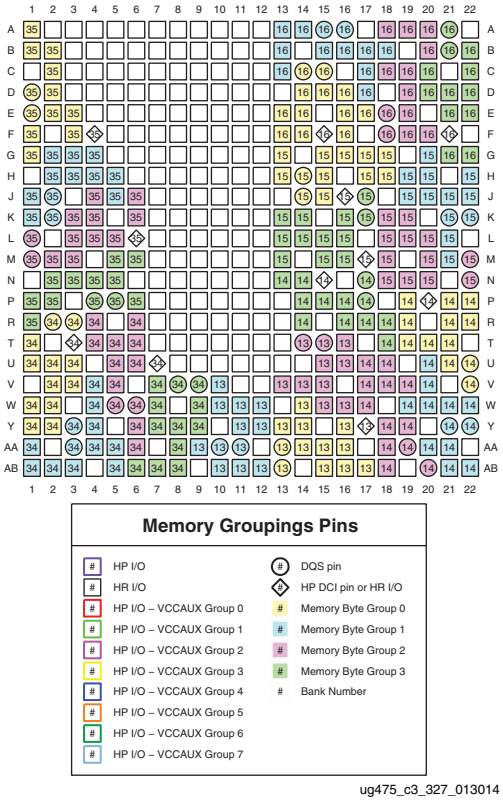


Figure 3-75: **FG484 and FGG484 Packages—XC7A75T and XC7A100T Memory Groupings**

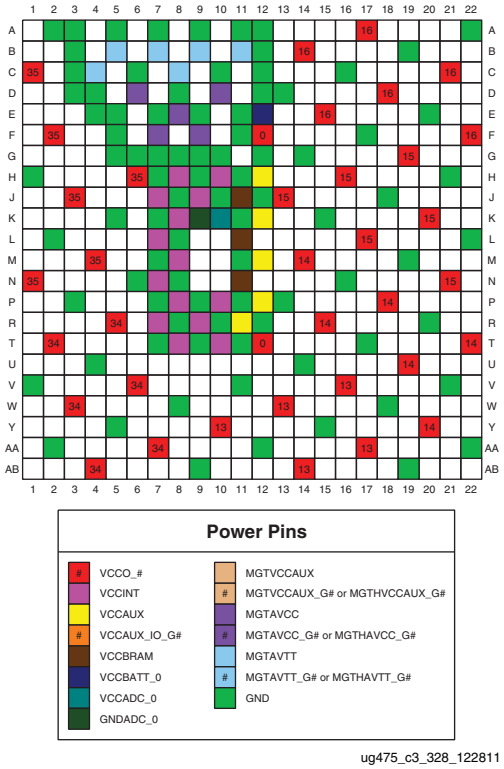


Figure 3-76: **FG484 and FGG484 Packages—XC7A75T and XC7A100T Power and GND Placement**

FG676 and FGG676 Packages—XC7A75T and XC7A100T

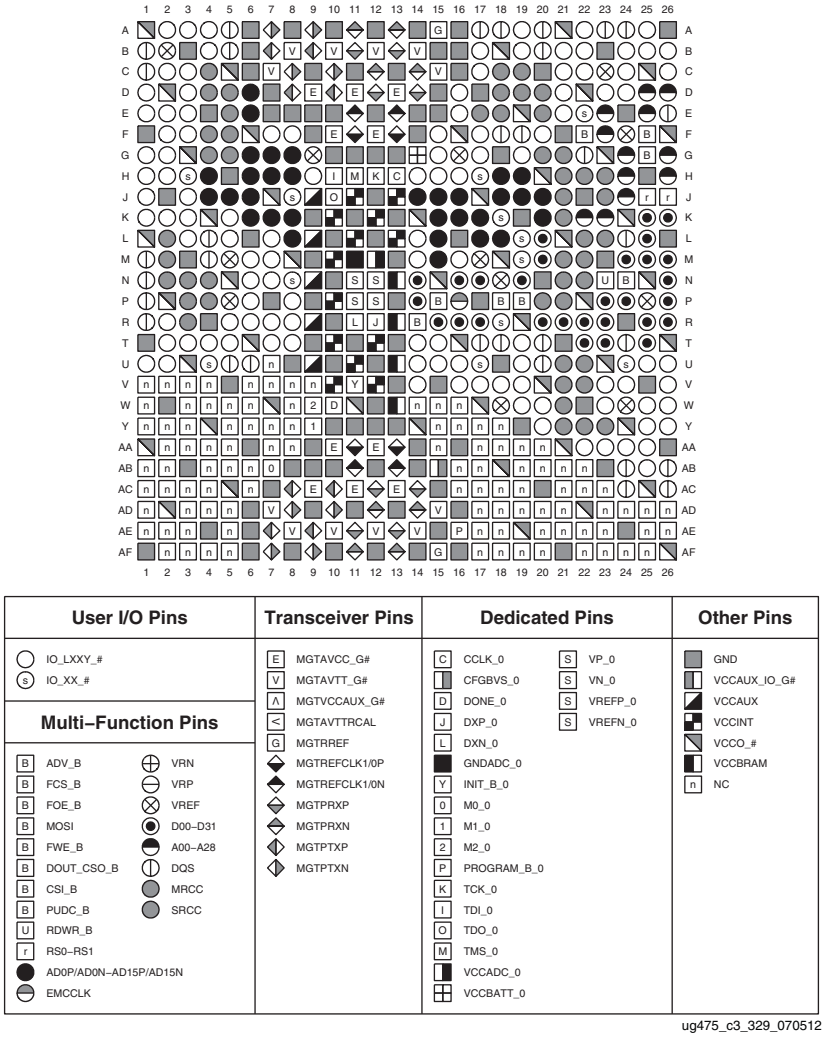


Figure 3-77: **FG676 and FGG676 Packages—XC7A75T and XC7A100T Pinout Diagram**

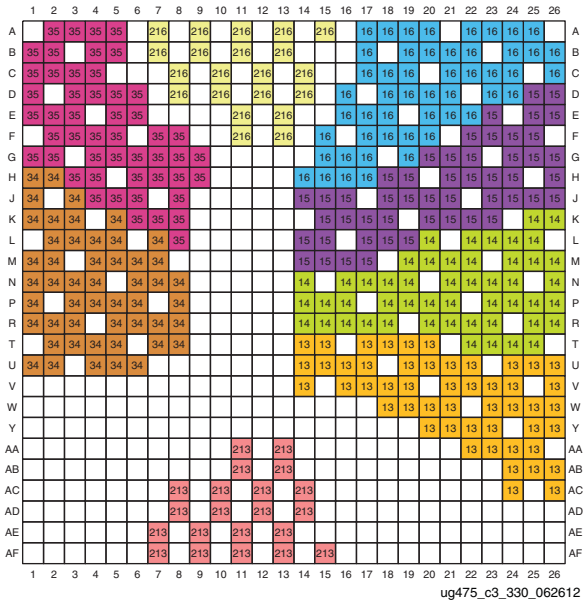


Figure 3-78: **FG676 and FGG676 Packages—XC7A75T and XC7A100T I/O Banks**

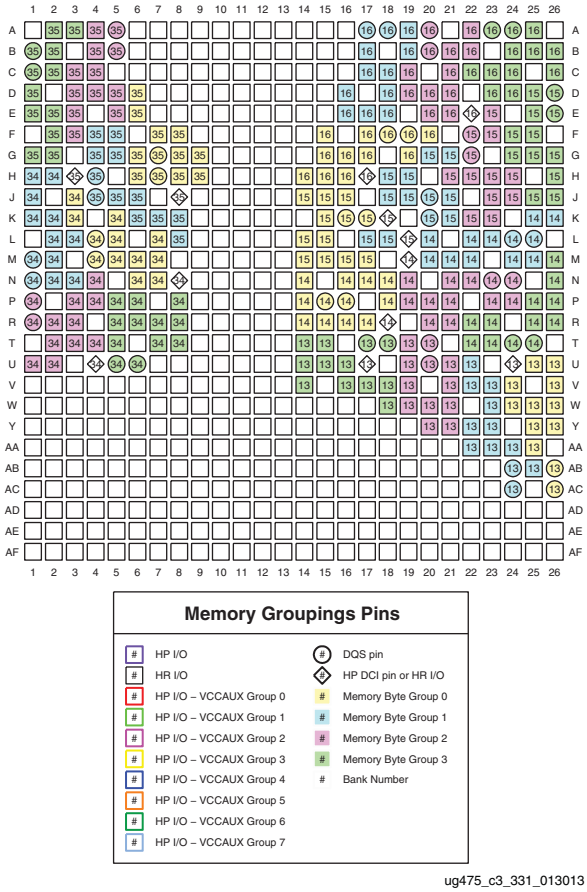


Figure 3-79: **FG676 and FGG676 Packages—XC7A75T and XC7A100T Memory Groupings**

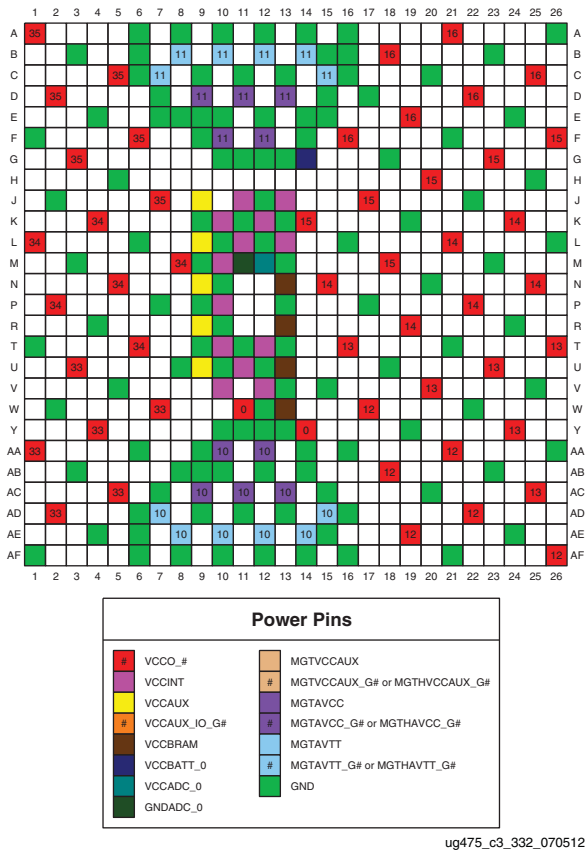


Figure 3-80: **FG676 and FGG676 Packages—XC7A75T and XC7A100T Power and GND Placement**

SB484, SBG484, SBV484, and RS484 Packages—XC7A200T

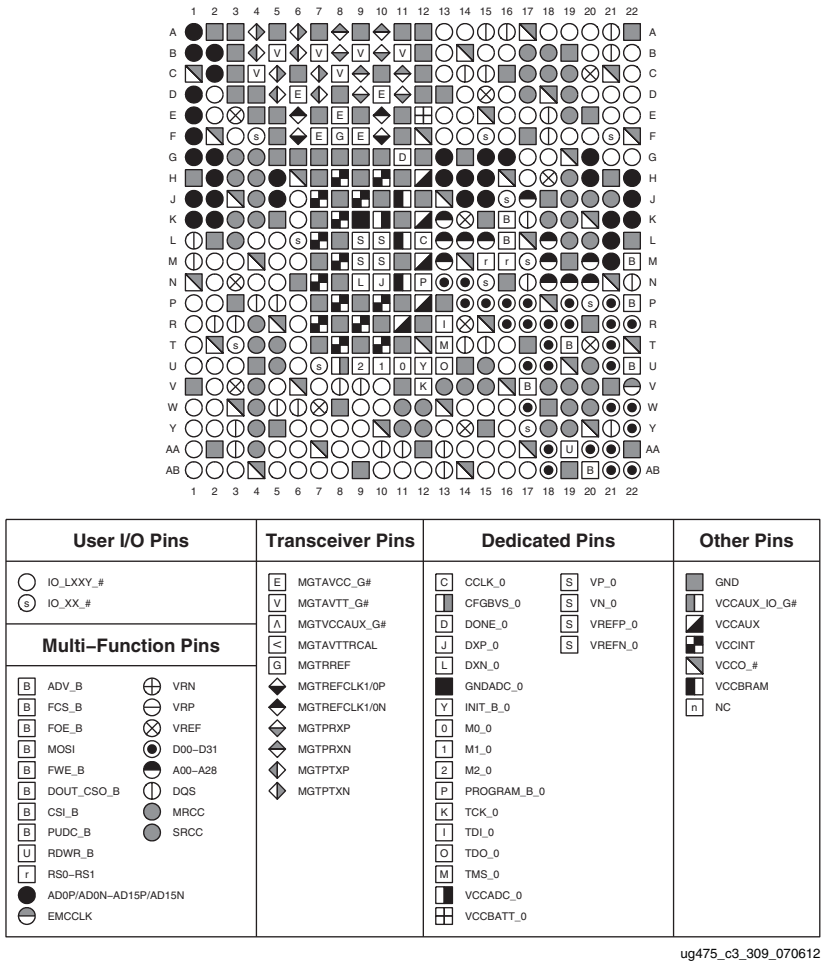


Figure 3-81: **SB484, SBG484, SBV484, and RS484 Packages—XC7A200T Pinout Diagram**

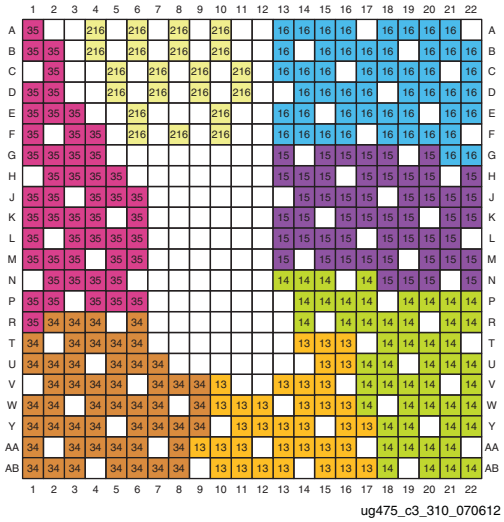


Figure 3-82: **SB484, SBG484, SBV484, and RS484 Packages—XC7A200T I/O Banks**

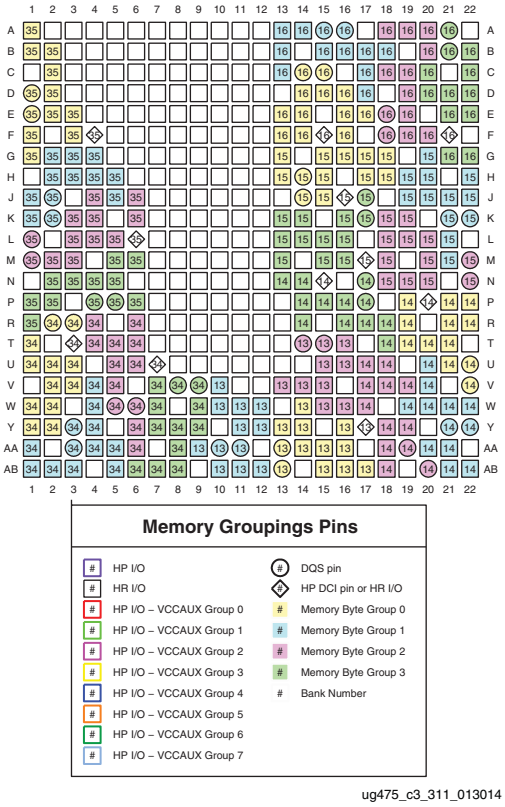


Figure 3-83: **SB484, SBG484, SBV484, and RS484 Packages—XC7A200T Memory Groupings**

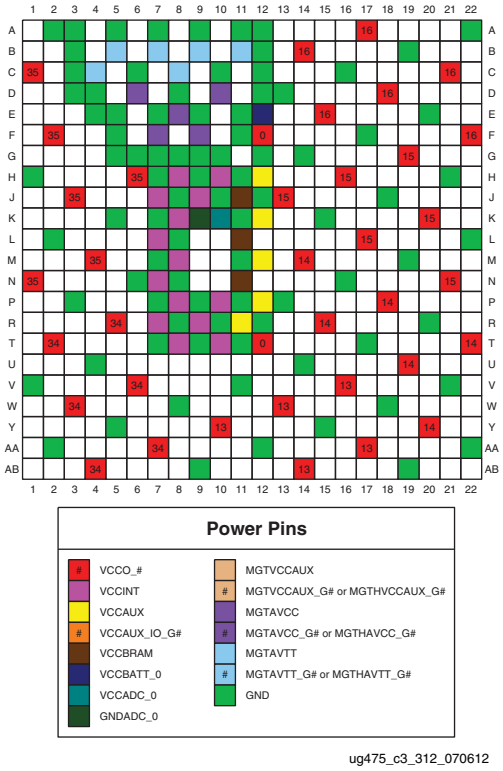


Figure 3-84: **SB484, SBG484, SBV484, and RS484 Packages—XC7A200T Power and GND Placement**

FB484, FBG484, FBV484, and RB484 Packages—XC7A200T

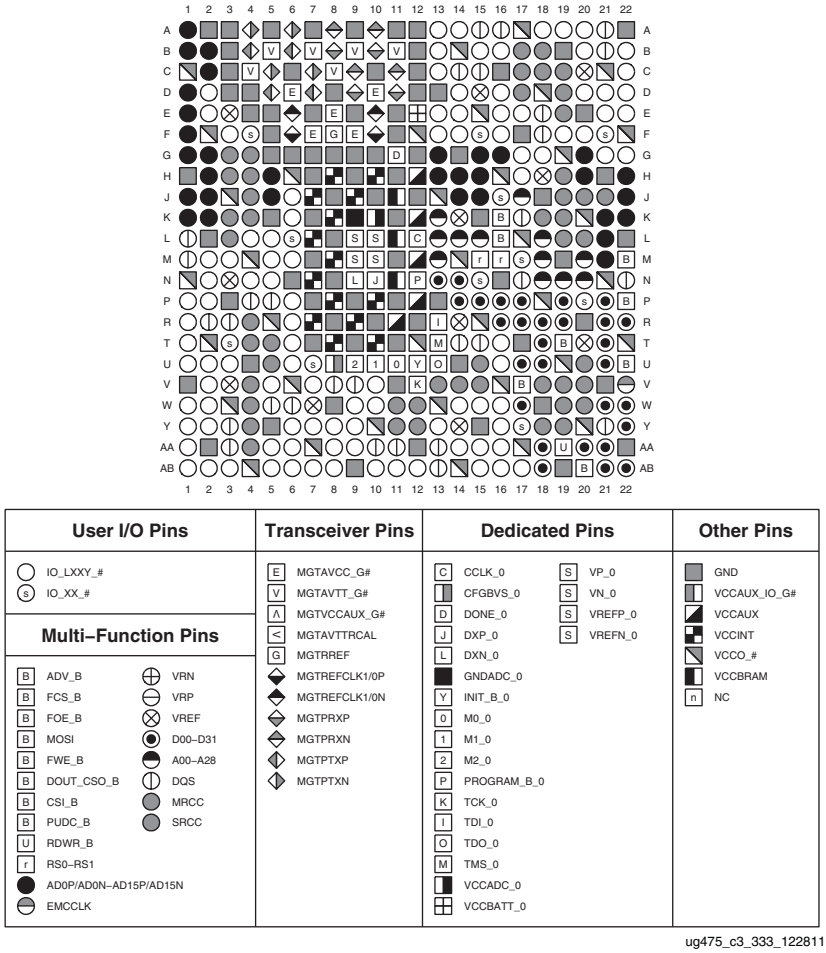


Figure 3-85: **FB484, FBG484, FBV484, and RB484 Packages—XC7A200T Pinout Diagram**

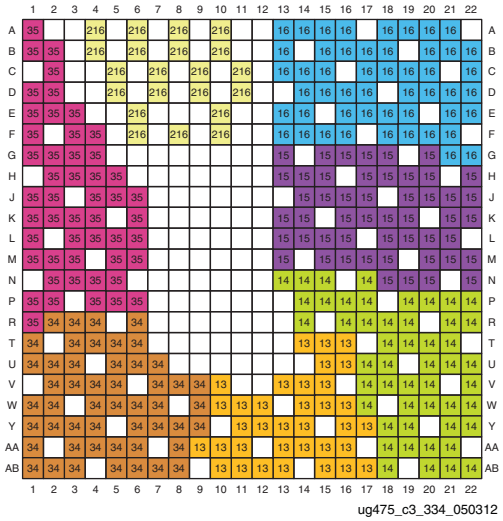


Figure 3-86: **FB484, FBG484, FBV484, and RB484 Packages—XC7A200T I/O Banks**

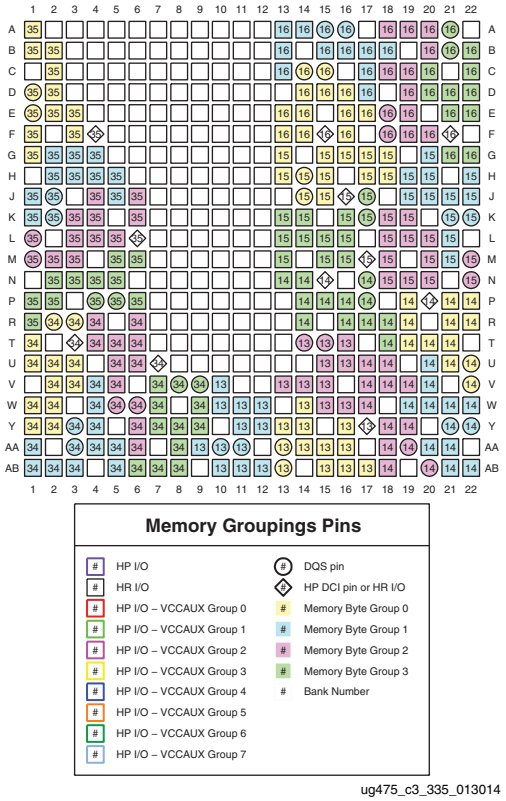


Figure 3-87: **FB484, FBG484, FBV484, and RB484 Packages—XC7A200T Memory Groupings**

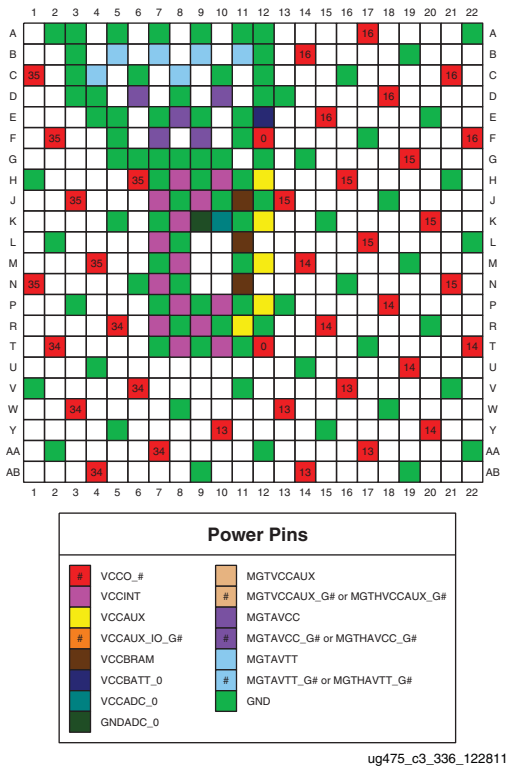


Figure 3-88: **FB484, FBG484, FBV484, and RB484 Packages—XC7A200T Power and GND Placement**

FB676, FBG676, FBV676, and RB676 Packages—XC7A200T

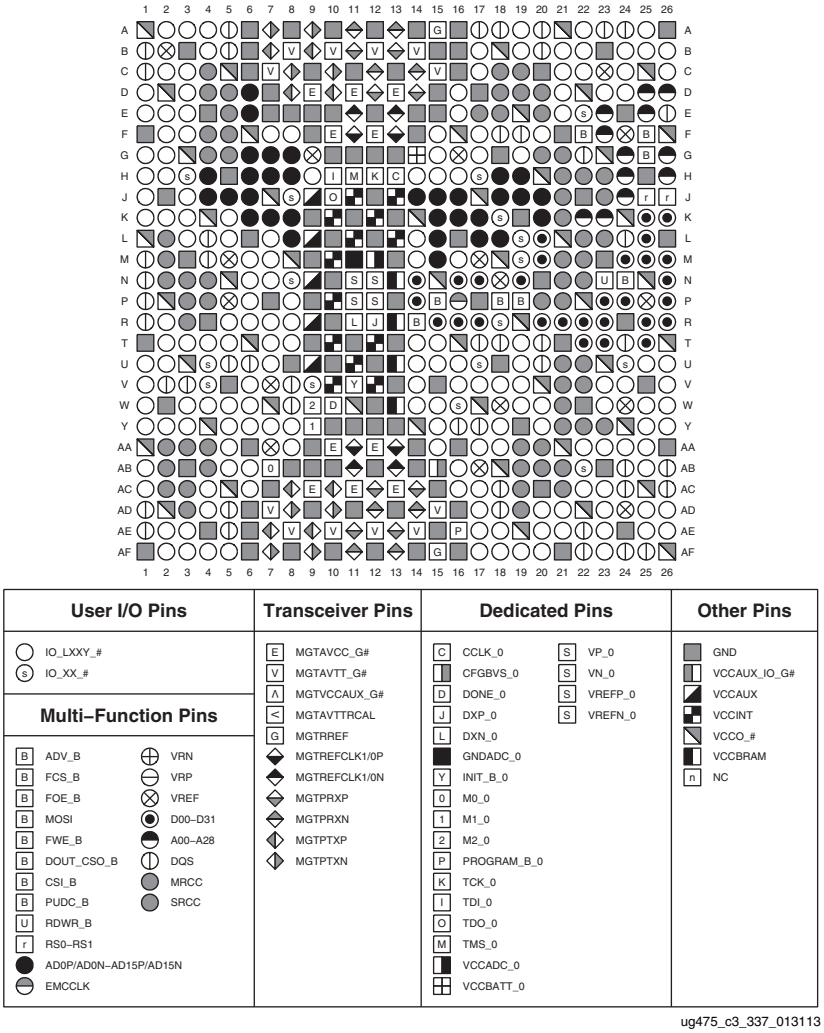


Figure 3-89: **FB676, FBG676, FBV676, and RB676 Packages—XC7A200T Pinout Diagram**

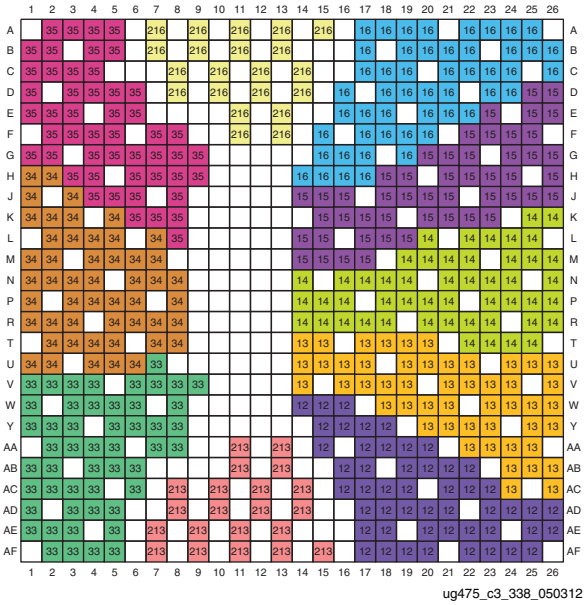


Figure 3-90: **FB676, FBG676, FBV676, and RB676 Packages—XC7A200T I/O Banks**

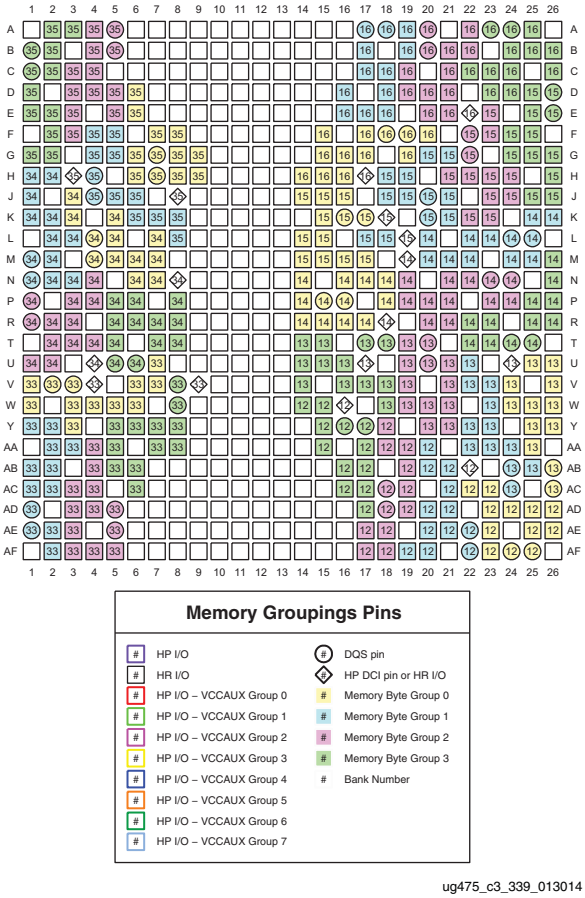


Figure 3-91: **FB676, FBG676, FBV676, and RB676 Packages—XC7A200T Memory Groupings**

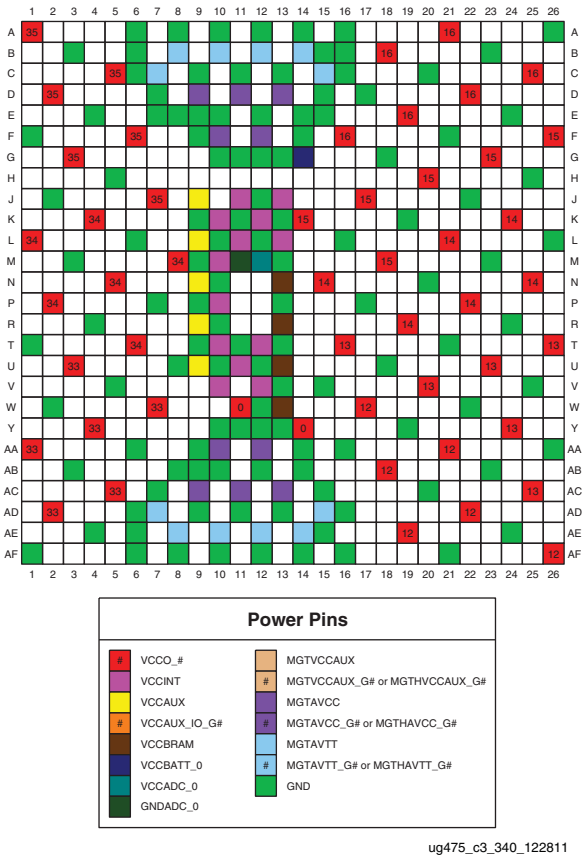


Figure 3-92: **FB676, FBG676, FBV676, and RB676 Packages—XC7A200T Power and GND Placement**

FF1156, FFG1156, and FFV1156 Packages—XC7A200T

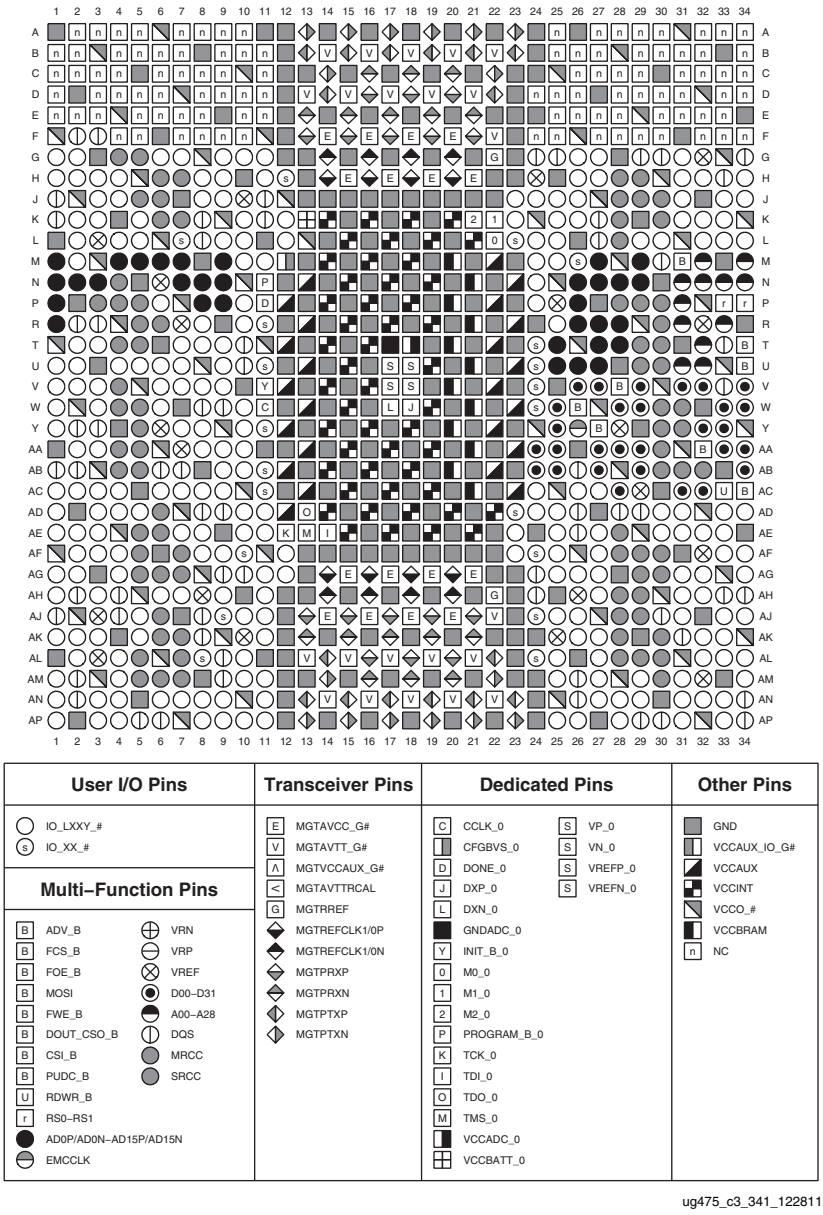


Figure 3-93: **FF1156, FFG1156, and FFV1156 Packages—XC7A200T Pinout Diagram**

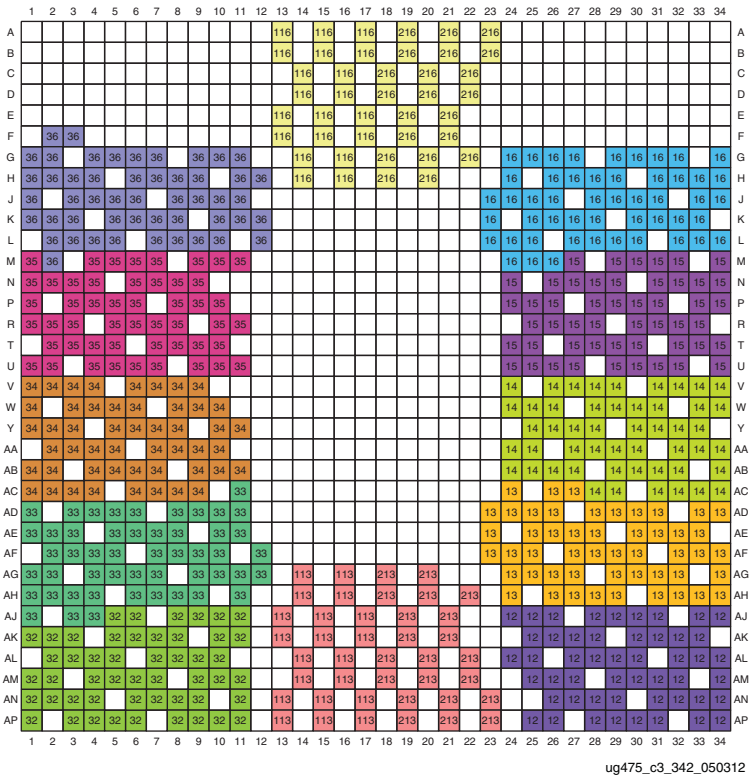


Figure 3-94: **FF1156, FFG1156, and FFV1156 Packages—XC7A200T I/O Banks**

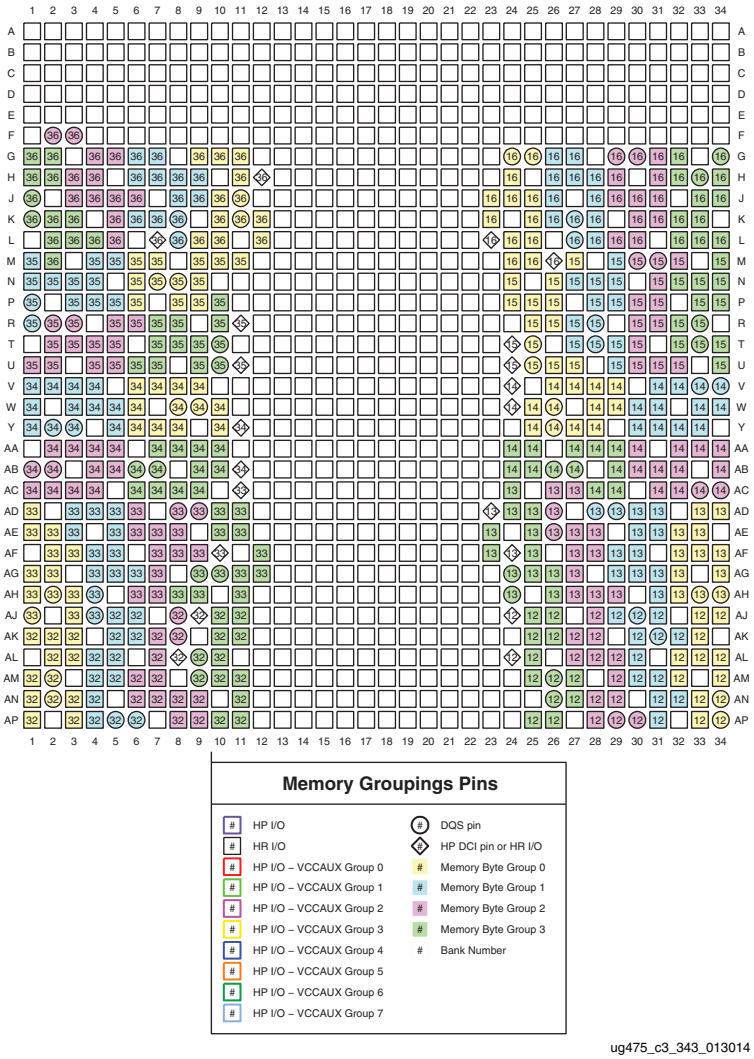


Figure 3-95: **FF1156, FFG1156, and FFV1156 Packages—XC7A200T Memory Groupings**

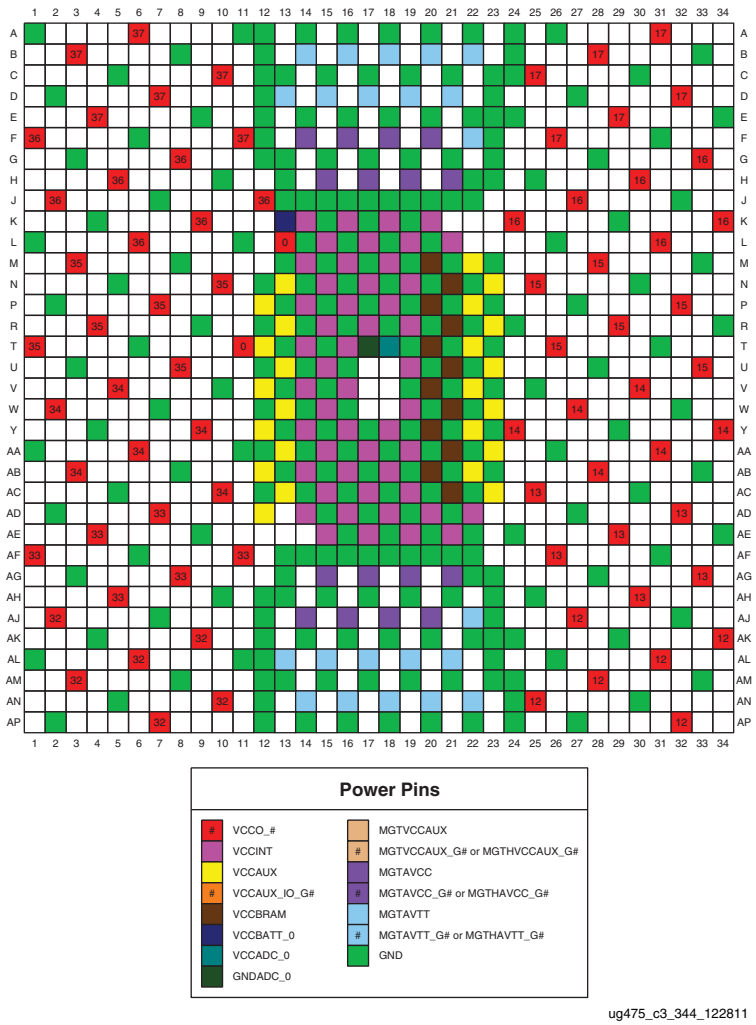


Figure 3-96: **FF1156, FFG1156, and FFV1156 Packages—XC7A200T Power and GND Placement**

Kintex-7 FPGAs Device Diagrams

Table 3-3: **Kintex-7 FPGAs Device Diagrams Cross-Reference**

Device	FB484 FBG484 FBV484	FB676 FBG676 FBV676	FB900 FBG900 FBV900	FF676 FFG676 FFV676 RF676	FF900 FFG900 FFV900 RF900	FF901 FFG901 FFV901	FF1156 FFG1156 FFV1156
XC7K70T	page 133	page 136					
XC7K160T	page 133	page 139		page 146			
XC7K325T		page 139	page 142	page 146	page 150		
XC7K355T						page 154	
XC7K410T		page 139	page 142	page 146	page 150		
XC7K420T						page 158	page 162
XC7K480T						page 158	page 162

FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T

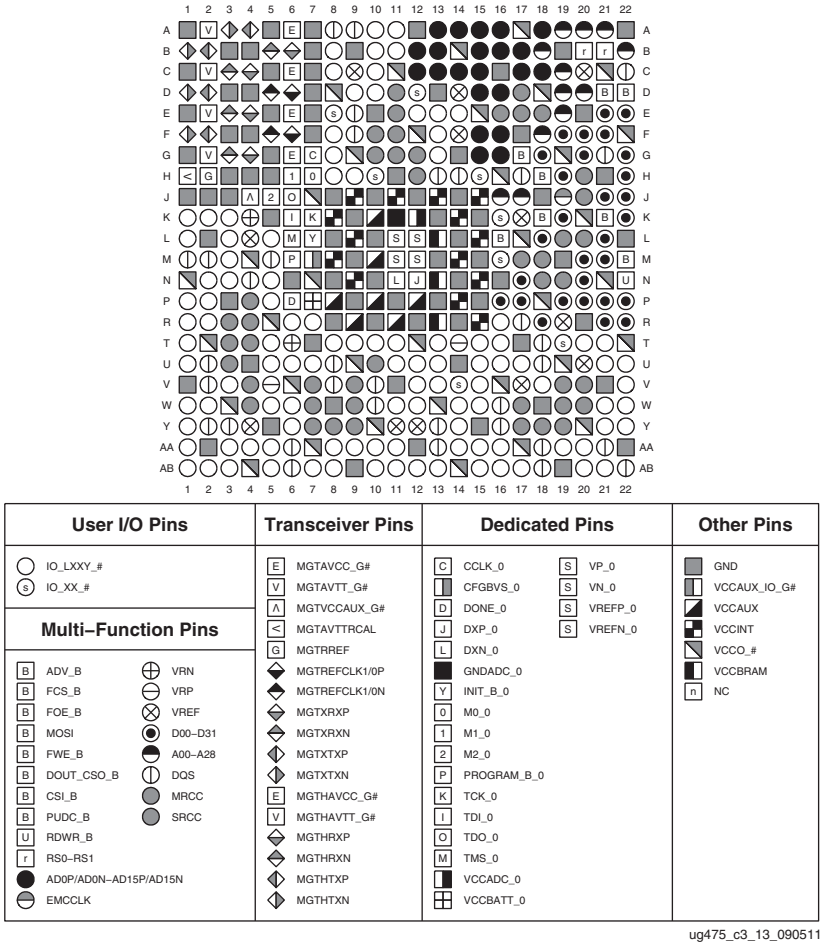


Figure 3-97: **FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T Pinout Diagram**

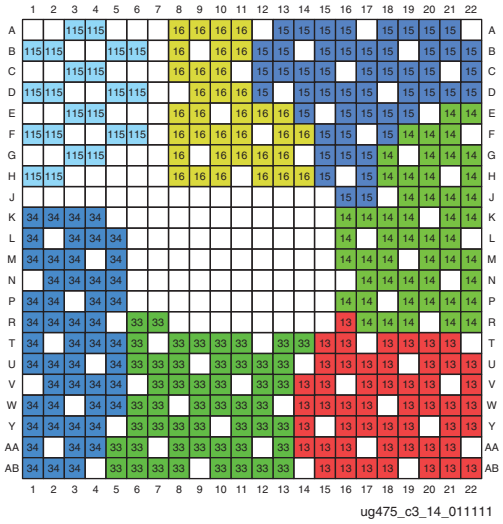


Figure 3-98: **FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T I/O Banks**

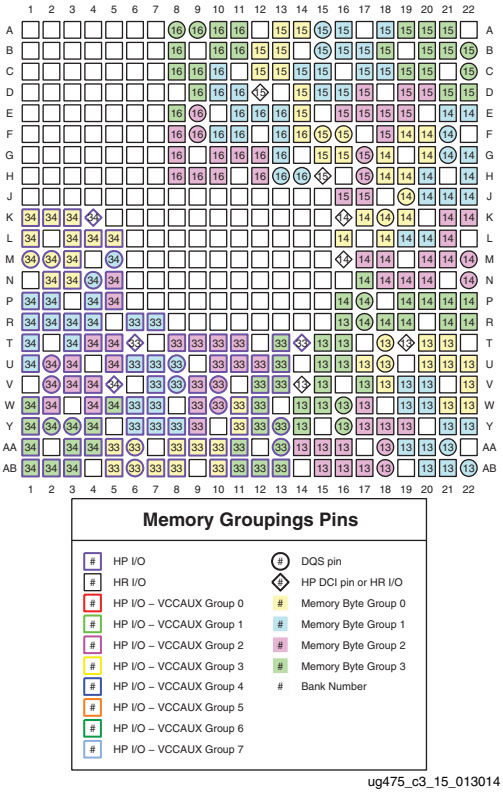


Figure 3-99: **FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T Memory Groupings**

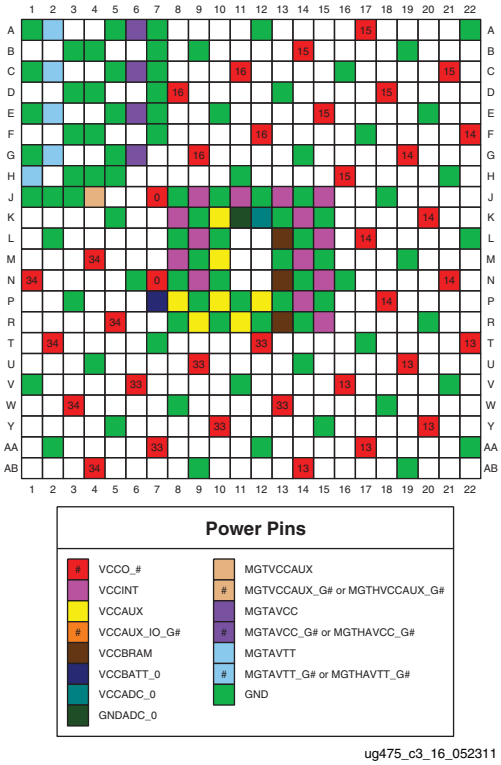
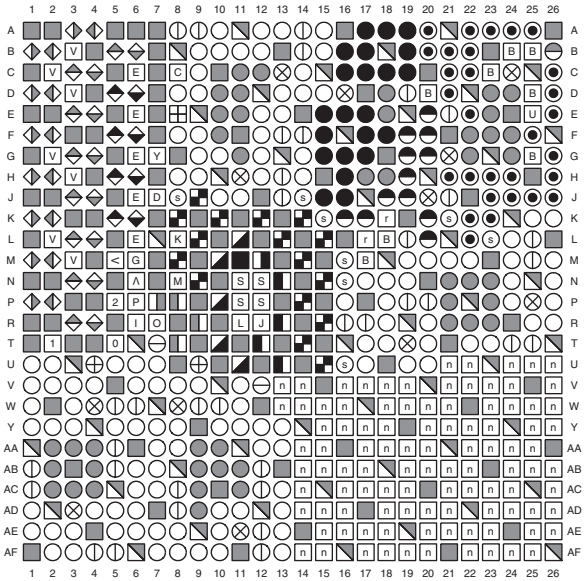


Figure 3-100: **FB484, FBG484, and FBV484 Packages—XC7K70T and XC7K160T Power and GND Placement**

FB676, FBG676, and FBV676 Packages—XC7K70T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

ug475_c3_05_090511

Figure 3-101: **FB676, FBG676, and FBV676 Packages—XC7K70T Pinout Diagram**

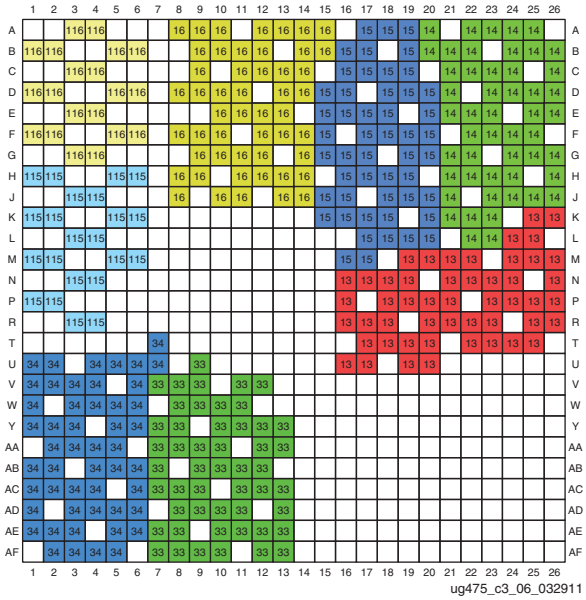


Figure 3-102: **FB676, FBG676, and FBV676 Packages—XC7K70T I/O Banks**

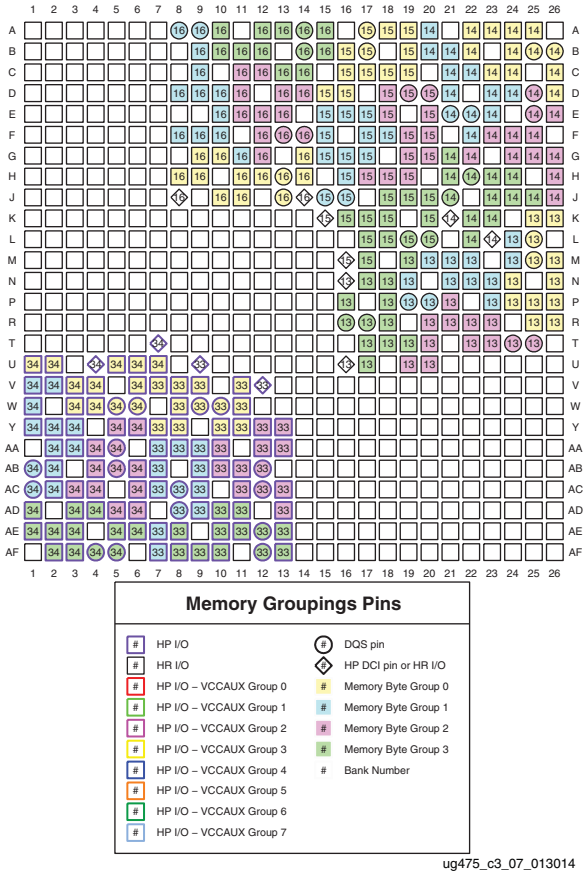


Figure 3-103: **FB676, FBG676, and FBV676 Packages—XC7K70T Memory Groupings**

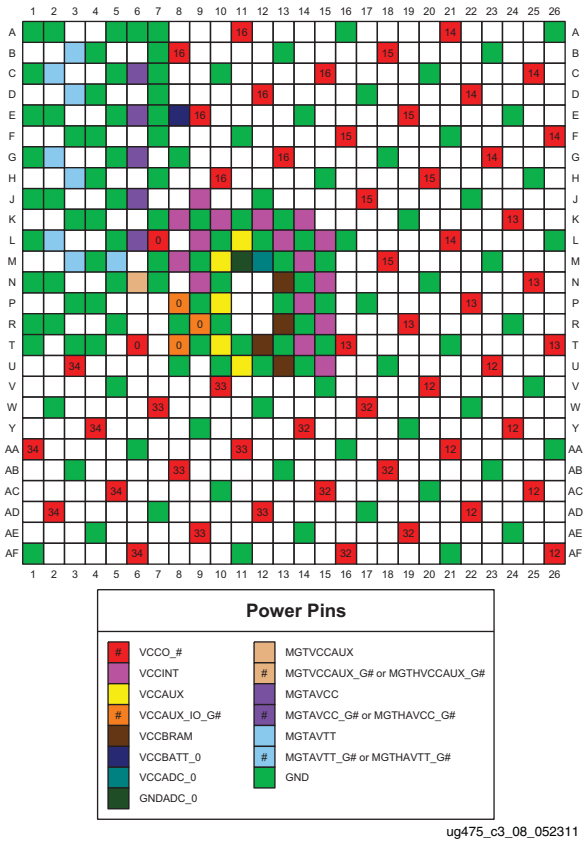


Figure 3-104: **FB676, FBG676, and FBV676 Packages—XC7K70T Power and GND Placement**

FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T

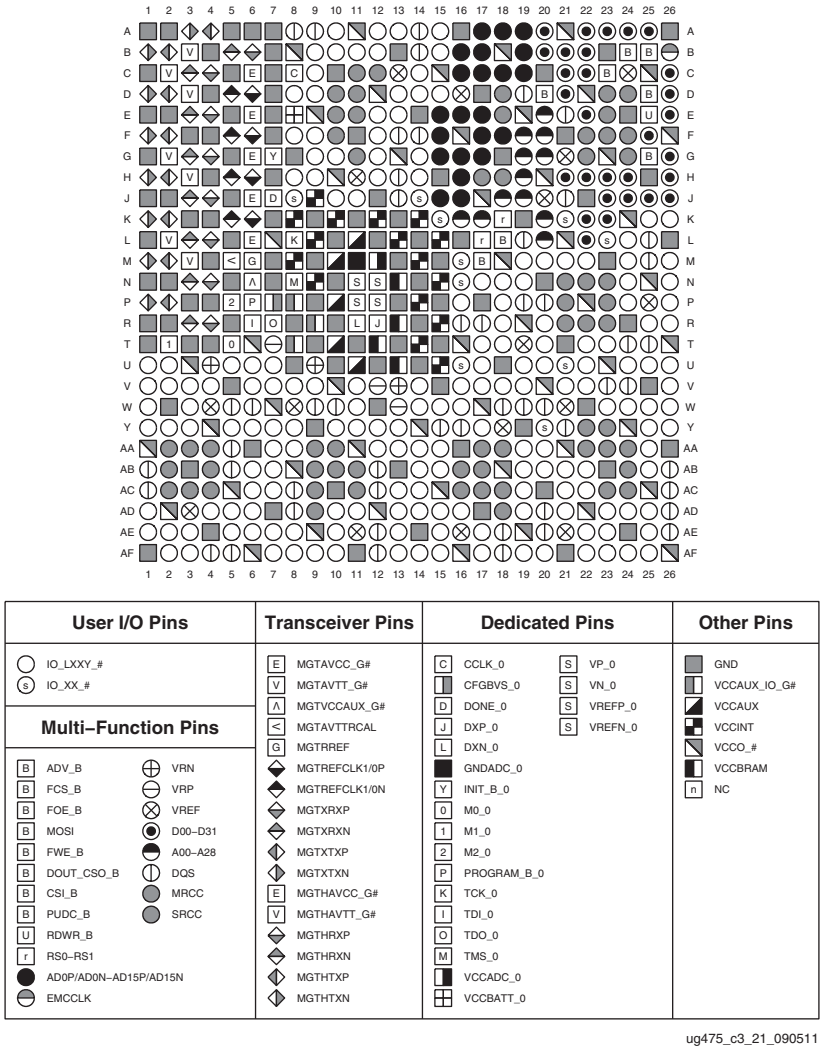


Figure 3-105: **FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram**

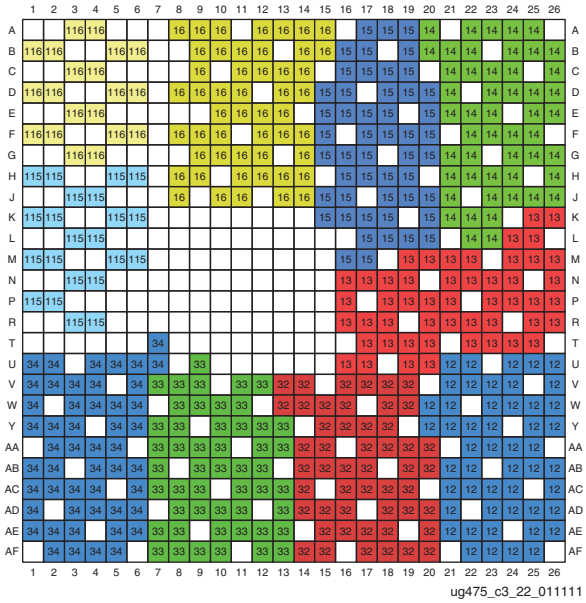


Figure 3-106: **FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T I/O Banks**

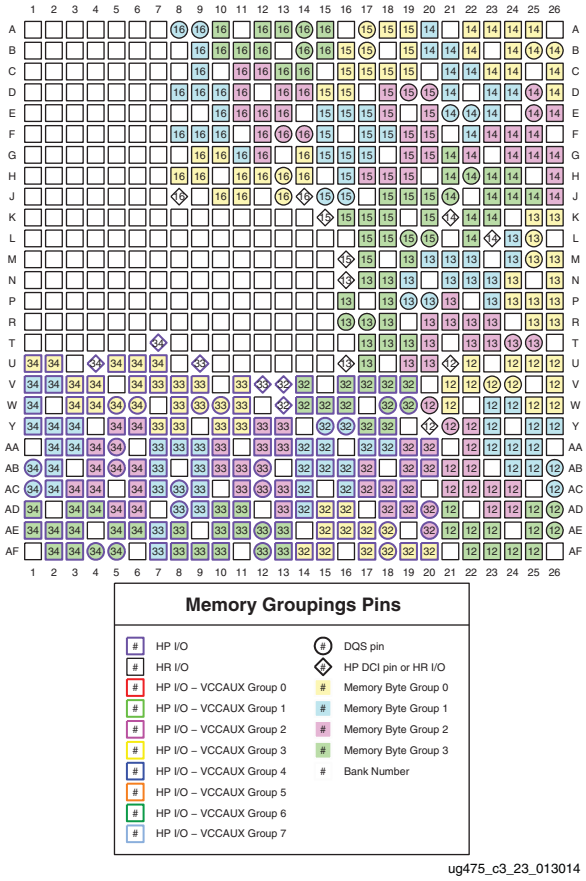


Figure 3-107: **FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T Memory Groupings**

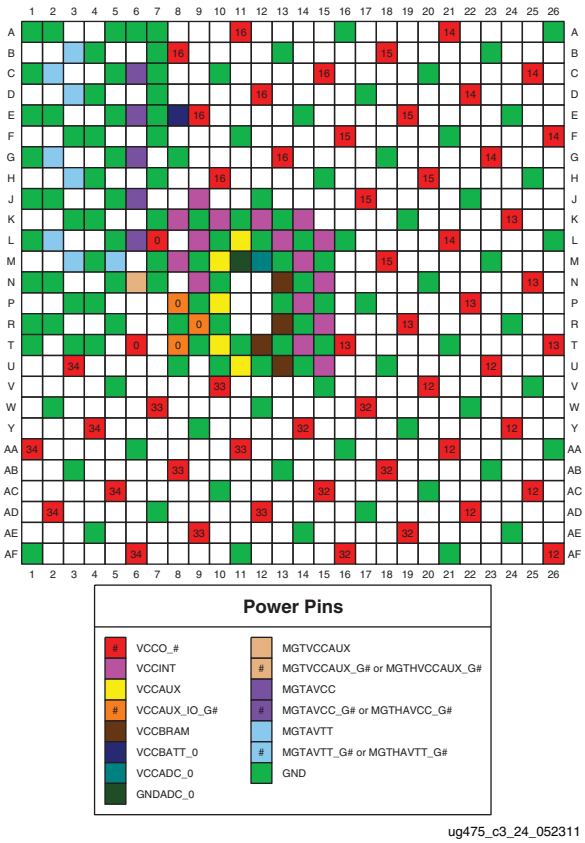
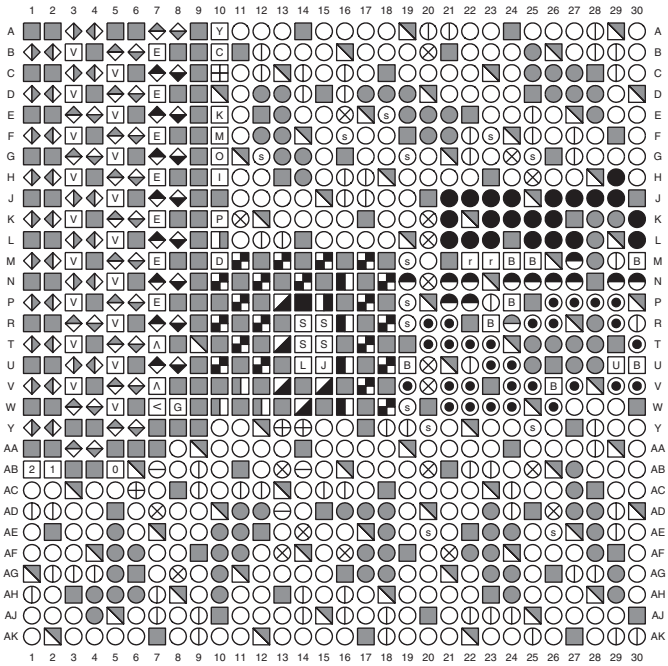


Figure 3-108: **FB676, FBG676, and FBV676 Packages—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement**

FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	VP_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VN_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VREFP_0	VCCAUX
ADV_B	VRN	MGTAVTTRCAL	DXP_0	VREFN_0	VCCINT
FCS_B	VRP	MGTRREF	DXN_0	VCCO_#
FOE_B	VREF	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	D00–D31	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	A00–A28	MGTXRXP	M0_0
DOUT_CSO_B	DQS	MGTXRXN	M1_0
CSI_B	MRCC	MGTXTXP	M2_0
PUDC_B	SRCC	MGTXTXN	PROGRAM_B_0
RDWR_B	MGTHAVCC_G#	TCK_0
RS0–RS1	MGTHAVTT_G#	TDI_0
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0
EMCCLK	MGTHRXN	TMS_0
	MGTHTXP	VCCADC_0
	MGTHTXN	VCCBATT_0

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Figure 3-109: **FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T Pinout Diagram**

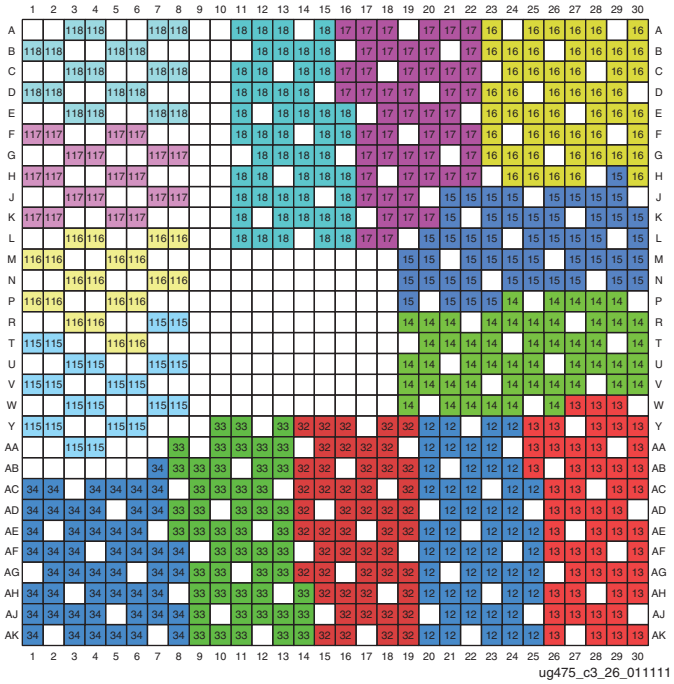


Figure 3-110: **FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T I/O Banks**

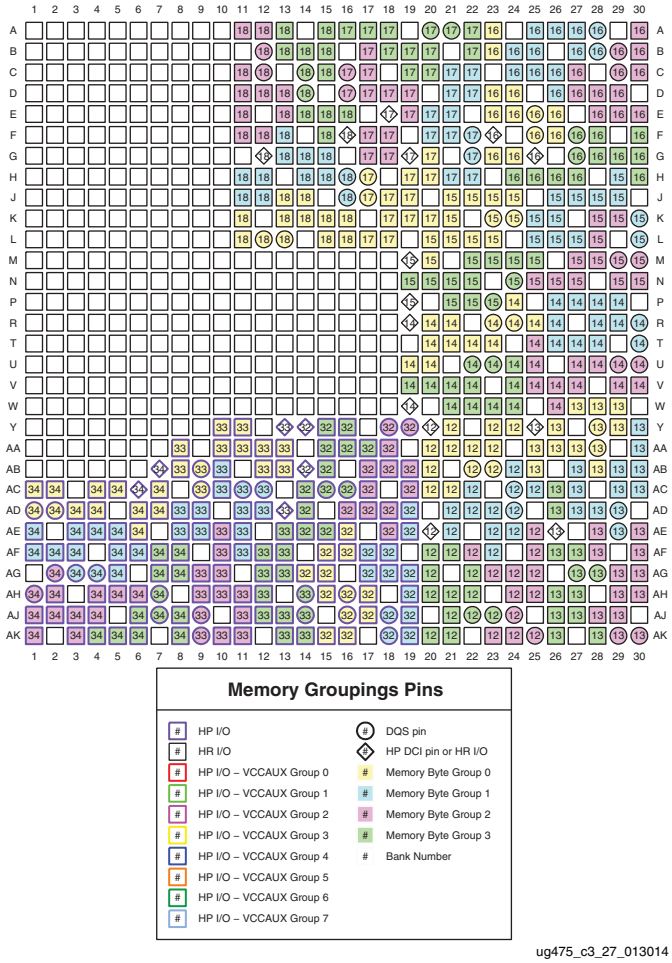


Figure 3-111: **FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T Memory Groupings**

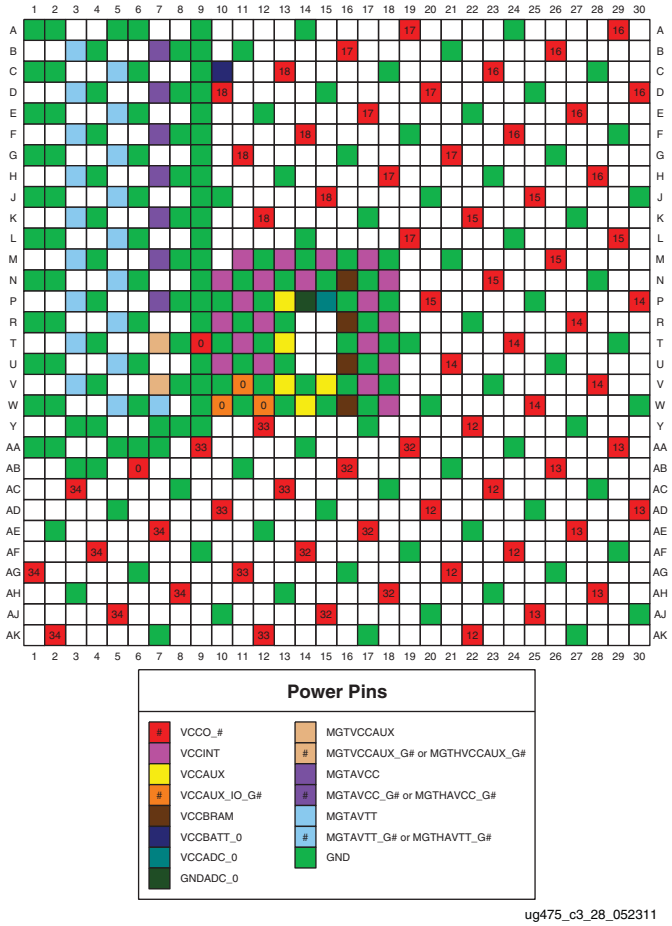


Figure 3-112: **FB900, FBG900, and FBV900 Packages—XC7K325T and XC7K410T Power and GND Placement**

FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T

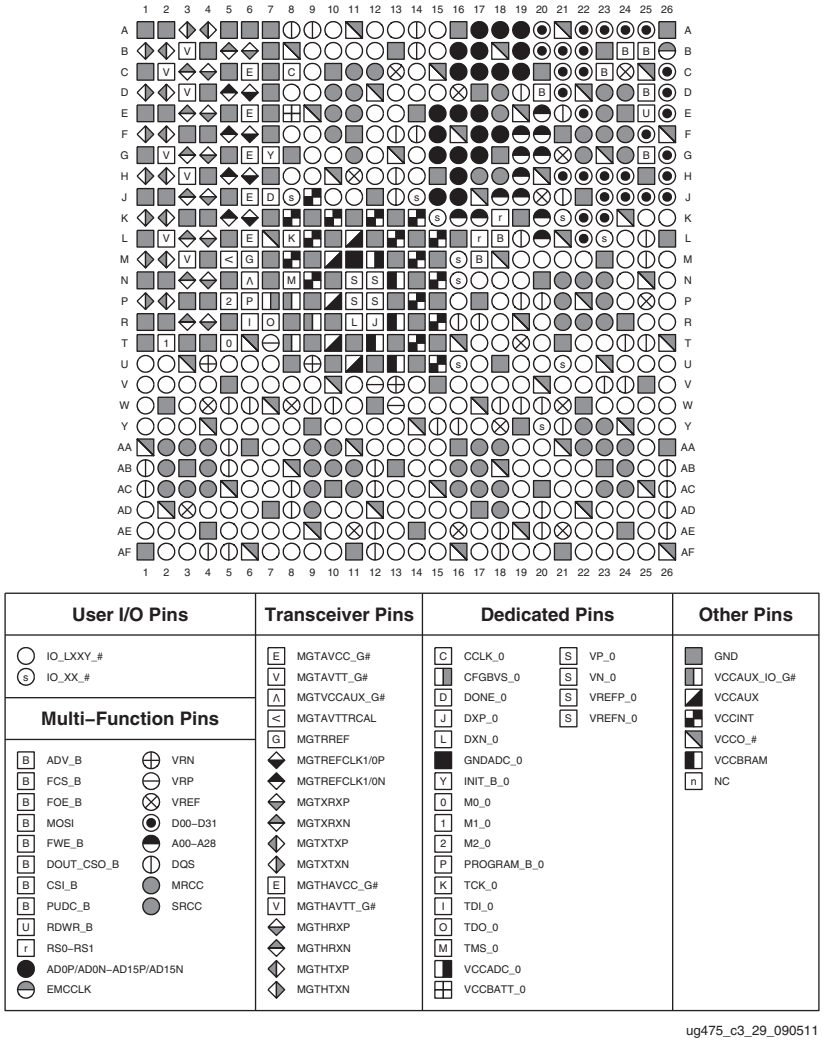


Figure 3-113: **FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram**

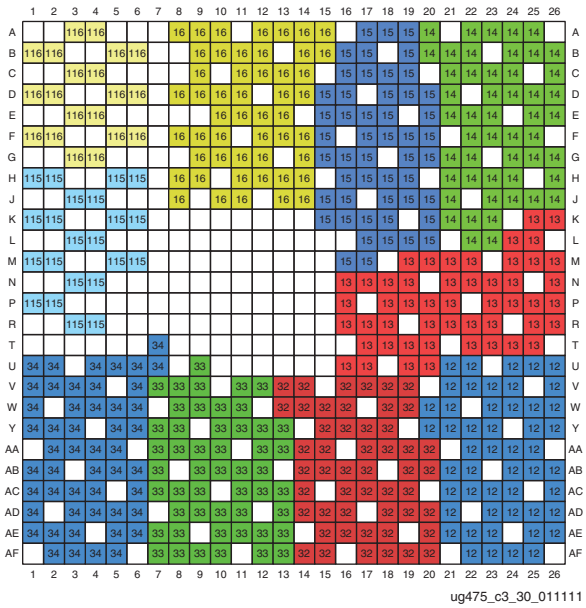


Figure 3-114: **FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T I/O Banks**

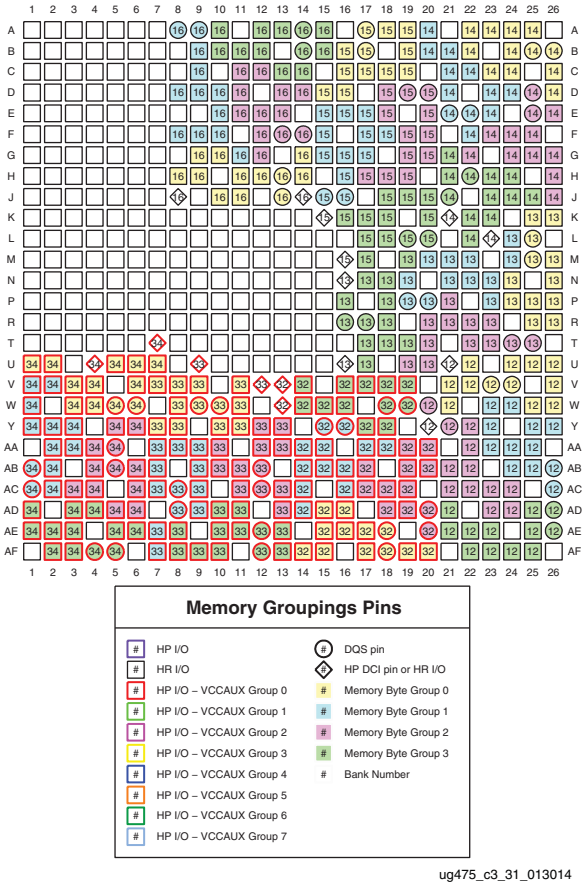


Figure 3-115: **FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T Memory Groupings**

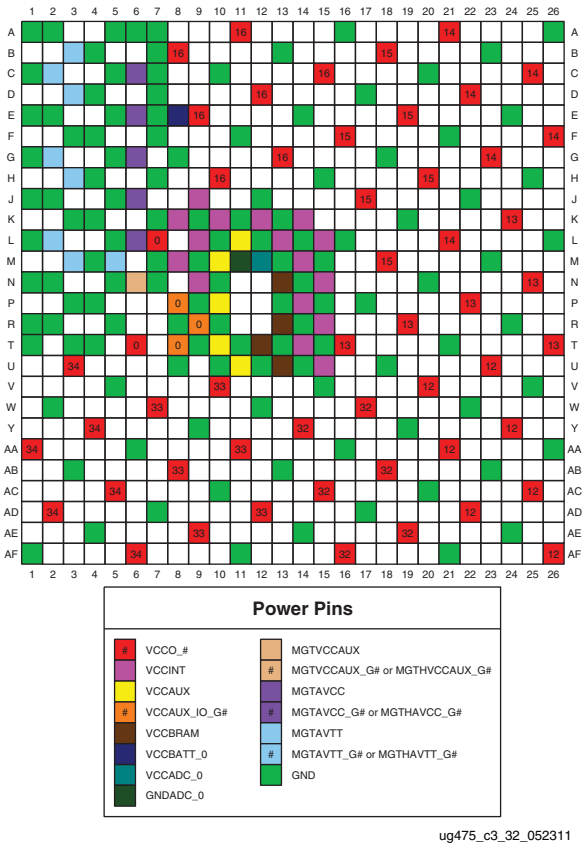
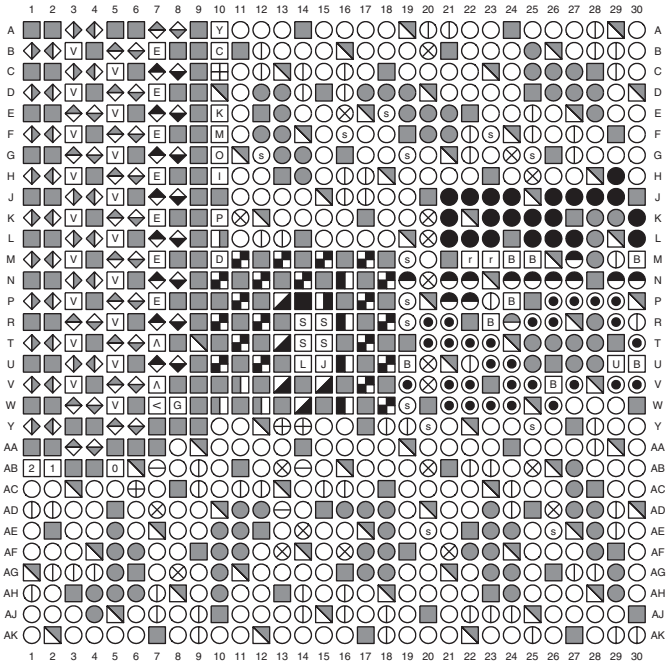


Figure 3-116: **FF676, FFG676, FFV676, and RF676 Packages—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement**

FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	VP_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VN_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VREFP_0	VCCAUX
ADV_B	VRN	MGTAVTTRCAL	DXP_0	VREFN_0	VCCINT
FCS_B	VRP	MGTRREF	DXN_0	VCCO_#
FOE_B	VREF	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	D00–D31	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	A00–A28	MGTXRXP	M0_0
DOUT_CSO_B	DQS	MGTXRXN	M1_0
CSI_B	MRCC	MGTXTXP	M2_0
PUDC_B	SRCC	MGTXTXN	PROGRAM_B_0
RDWR_B	MGTHAVCC_G#	TCK_0
RS0–RS1	MGTHAVTT_G#	TDI_0
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0
EMCCLK	MGTHRXN	TMS_0
	MGTHTXP	VCCADC_0
	MGTHTXN	VCCBATT_0

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Figure 3-117: **FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T Pinout Diagram**

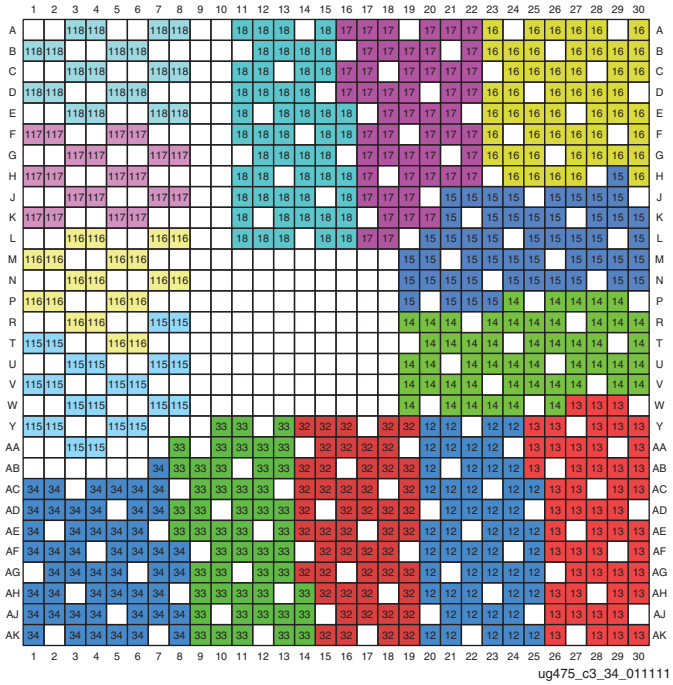


Figure 3-118: **FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T I/O Banks**

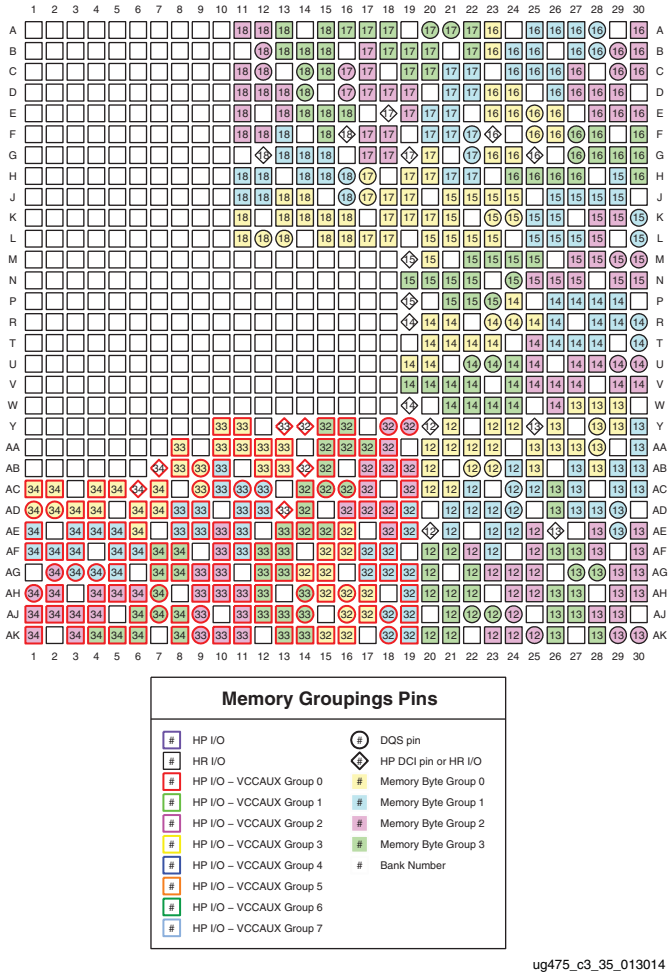


Figure 3-119: **FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T Memory Groupings**

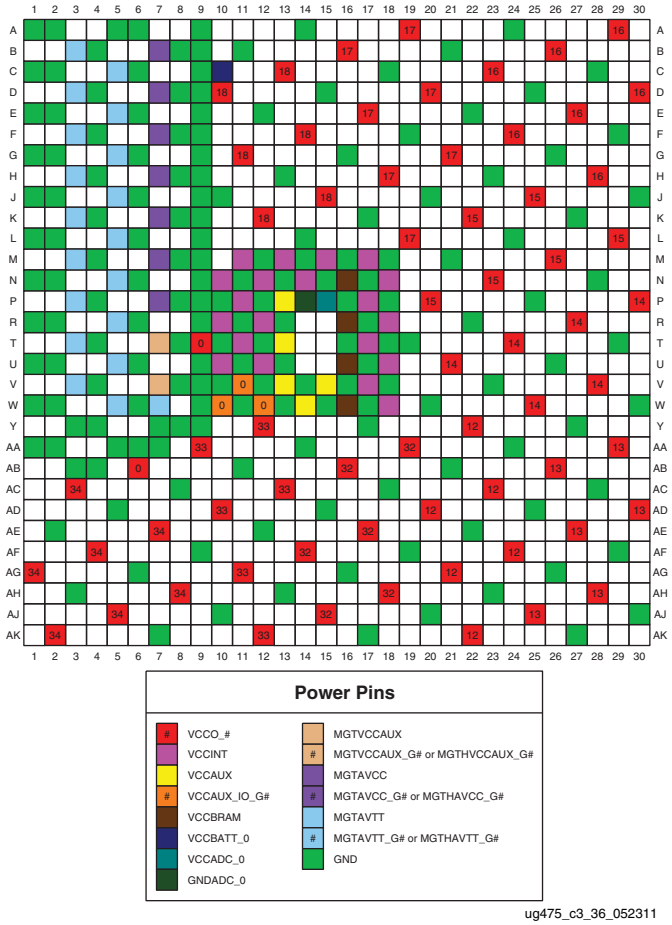


Figure 3-120: **FF900, FFG900, FFV900, and RF900 Packages—XC7K325T and XC7K410T Power and GND Placement**

FF901, FFG901, and FFV901 Packages—XC7K355T

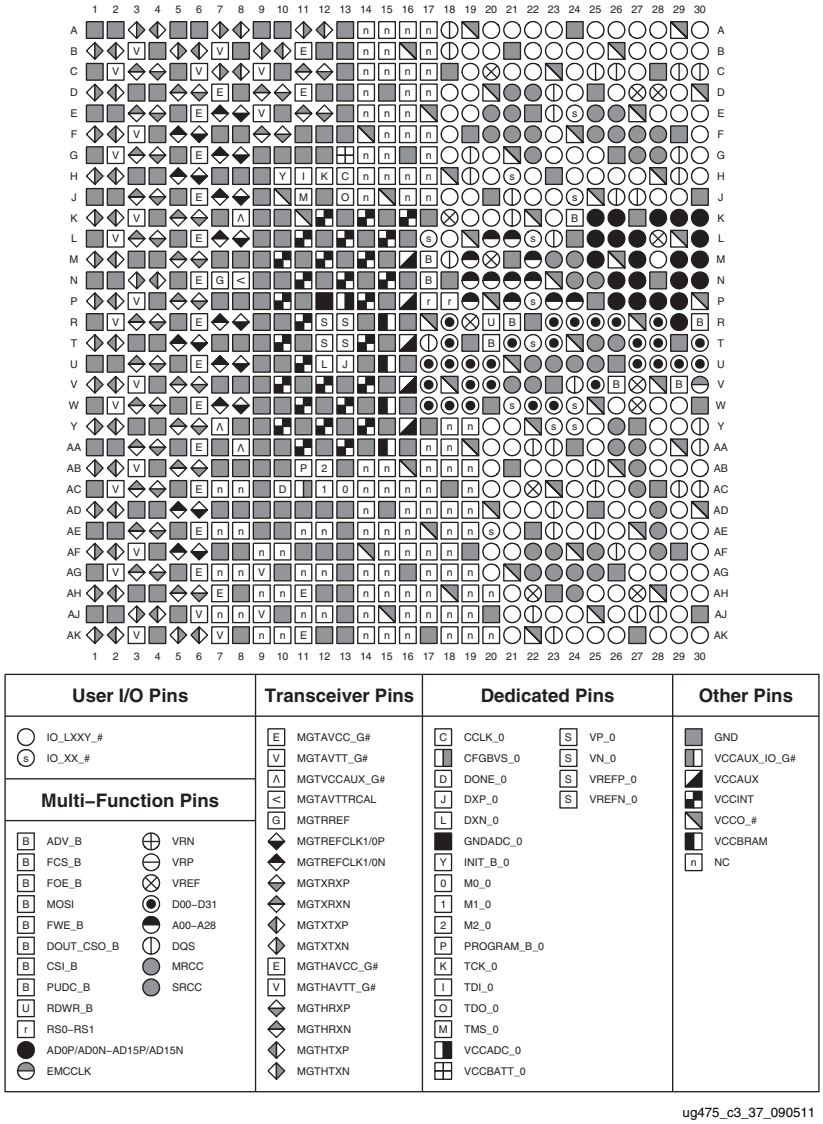


Figure 3-121: **FF901, FFG901, and FFV901 Packages—XC7K355T Pinout Diagram**

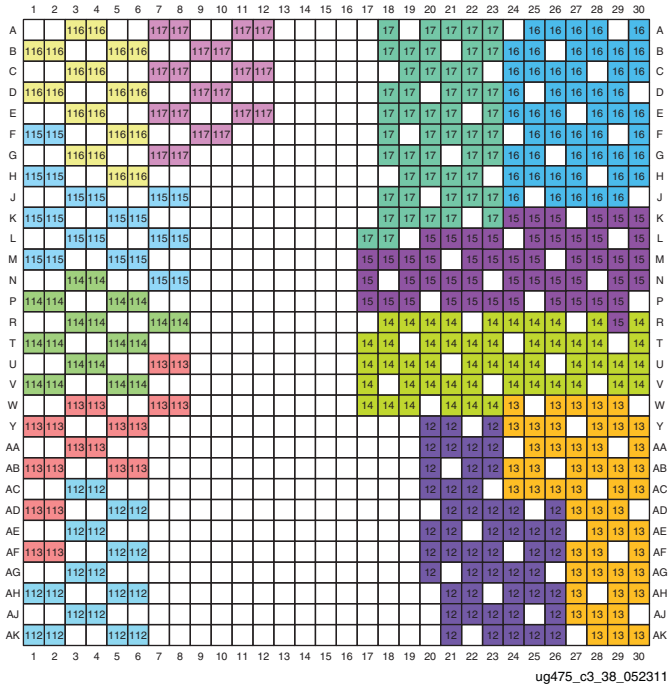


Figure 3-122: **FF901, FFG901, and FFV901 Packages—XC7K355T I/O Banks**

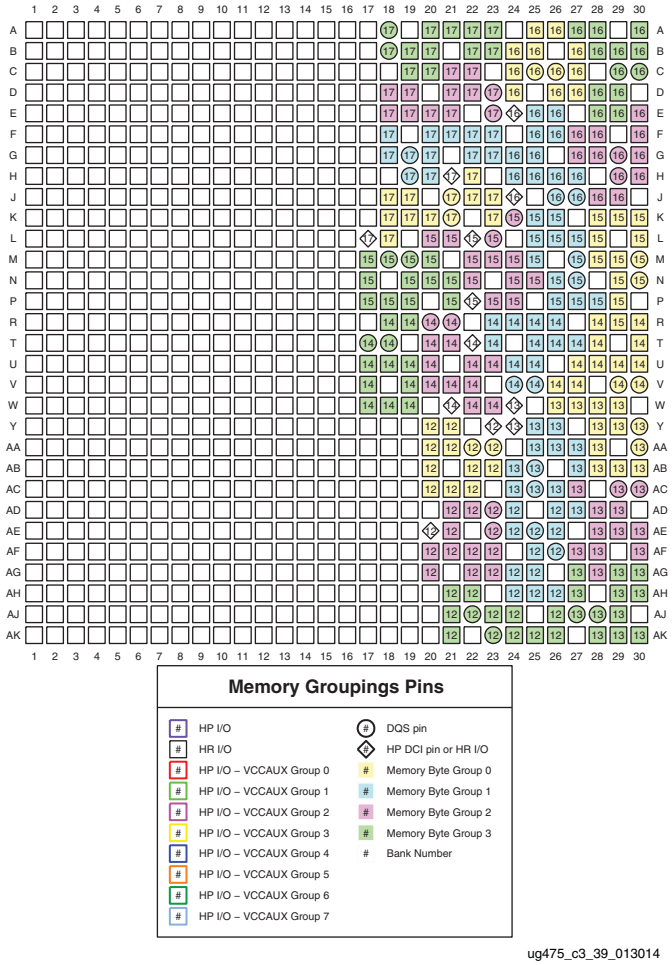


Figure 3-123: **FF901, FFG901, and FFV901 Packages—XC7K355T Memory Groupings**

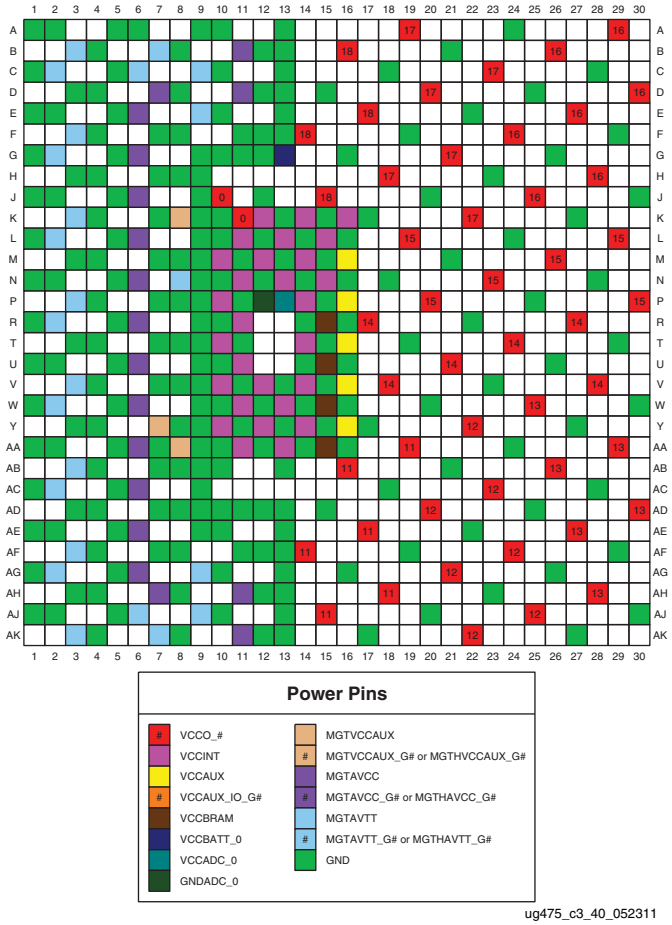


Figure 3-124: **FF901, FFG901, and FFV901 Packages—XC7K355T Power and GND Placement**

FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T

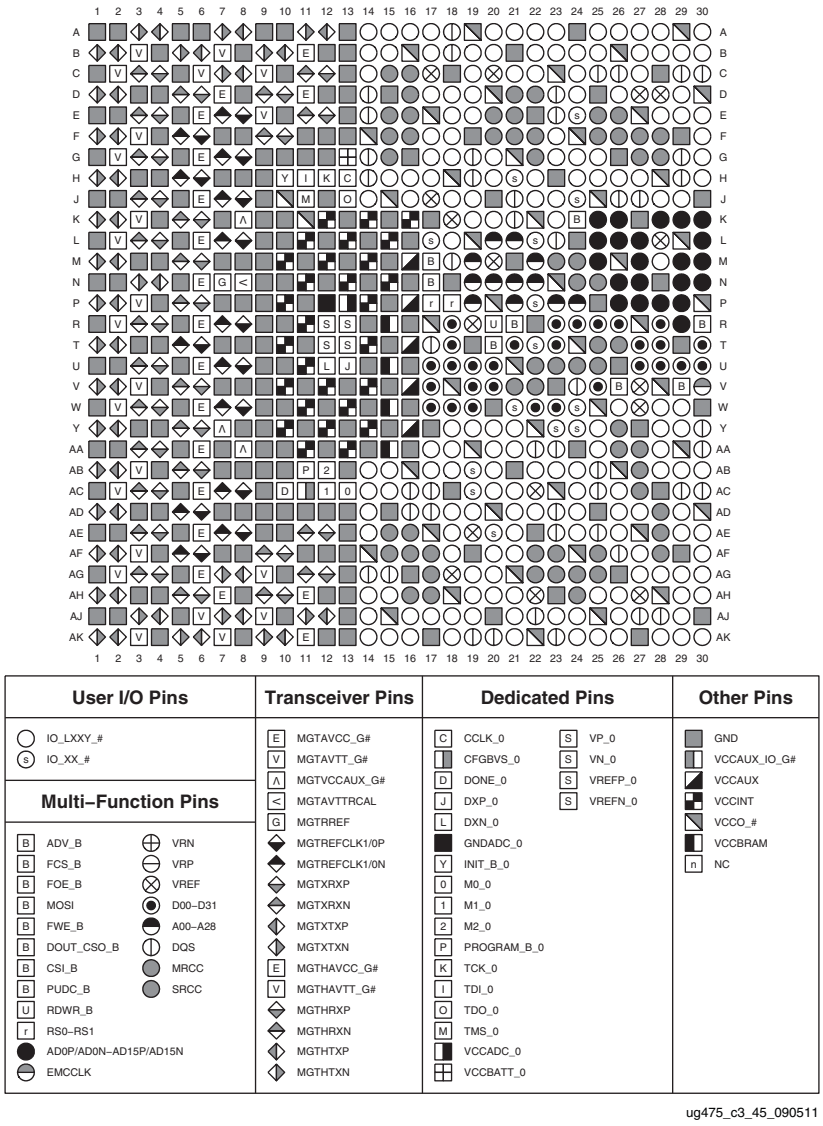


Figure 3-125: **FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T Pinout Diagram**

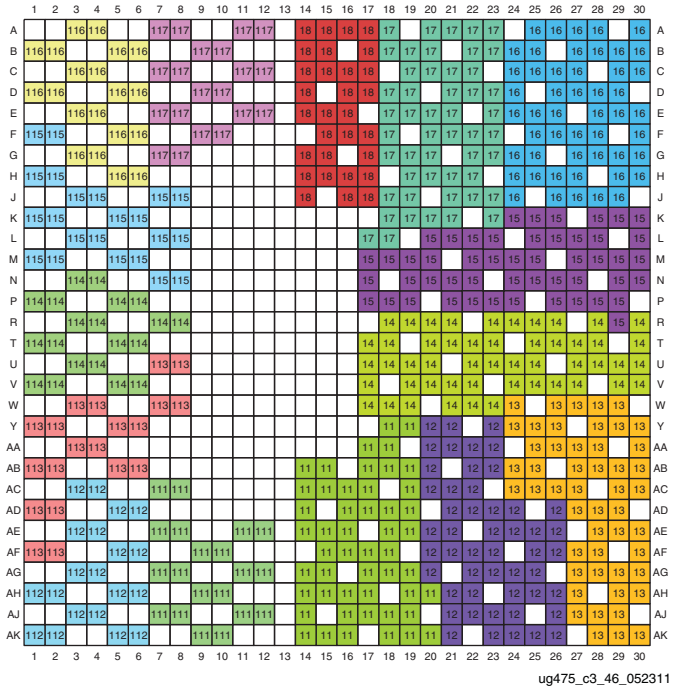


Figure 3-126: **FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T I/O Banks**

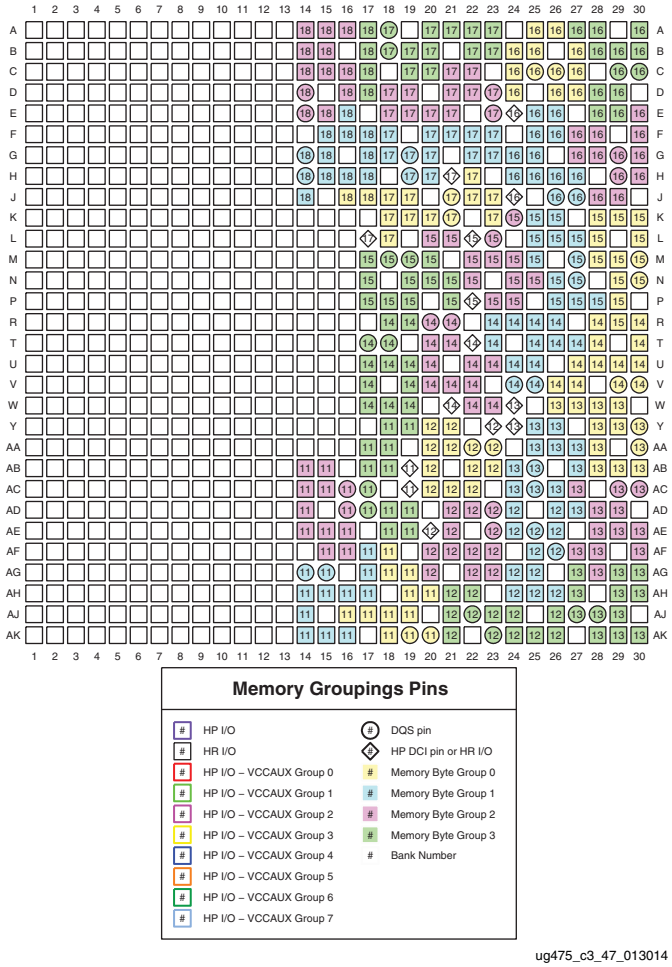


Figure 3-127: **FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T Memory Groupings**

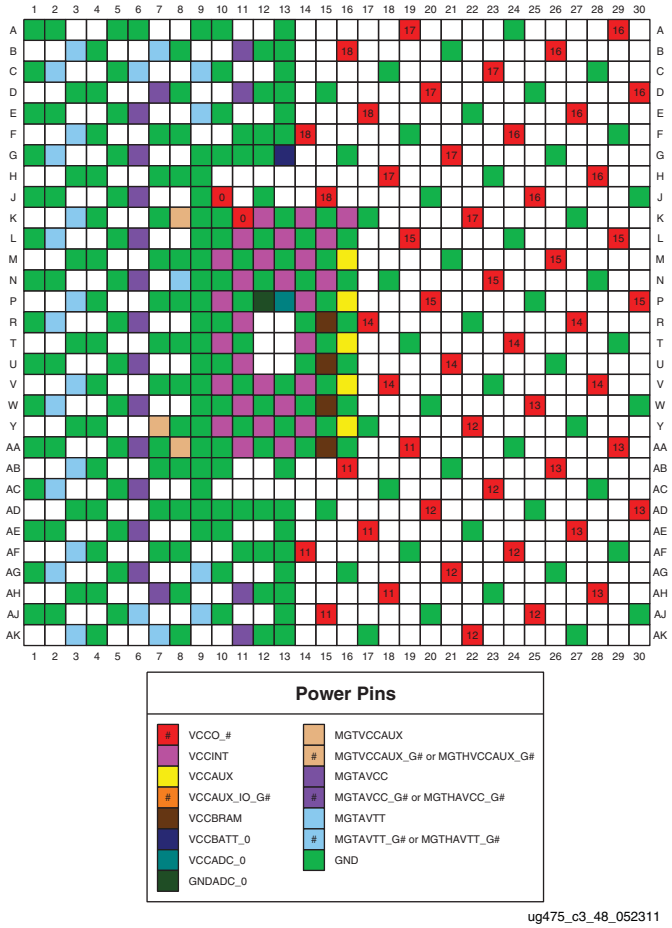


Figure 3-128: **FF901, FFG901, and FFV901 Packages—XC7K420T and XC7K480T Power and GND Placement**

FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T

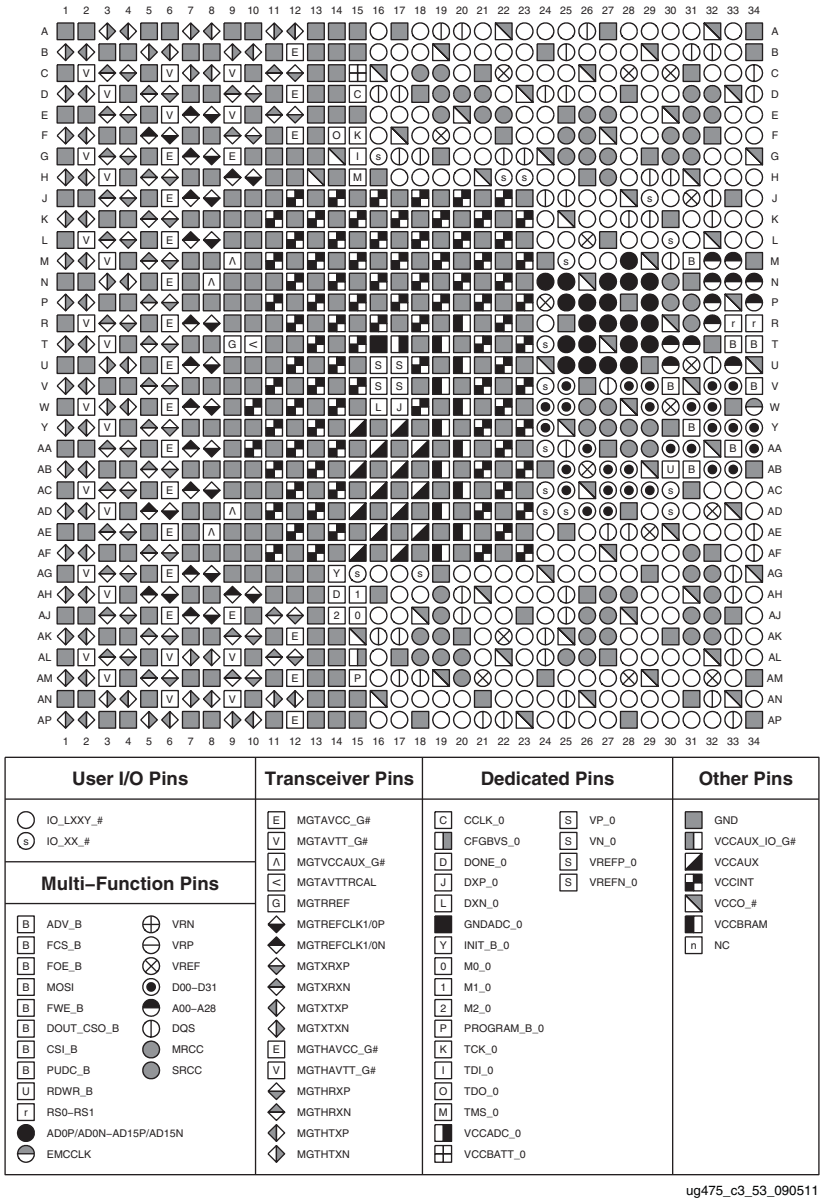


Figure 3-129: **FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T Pinout Diagram**

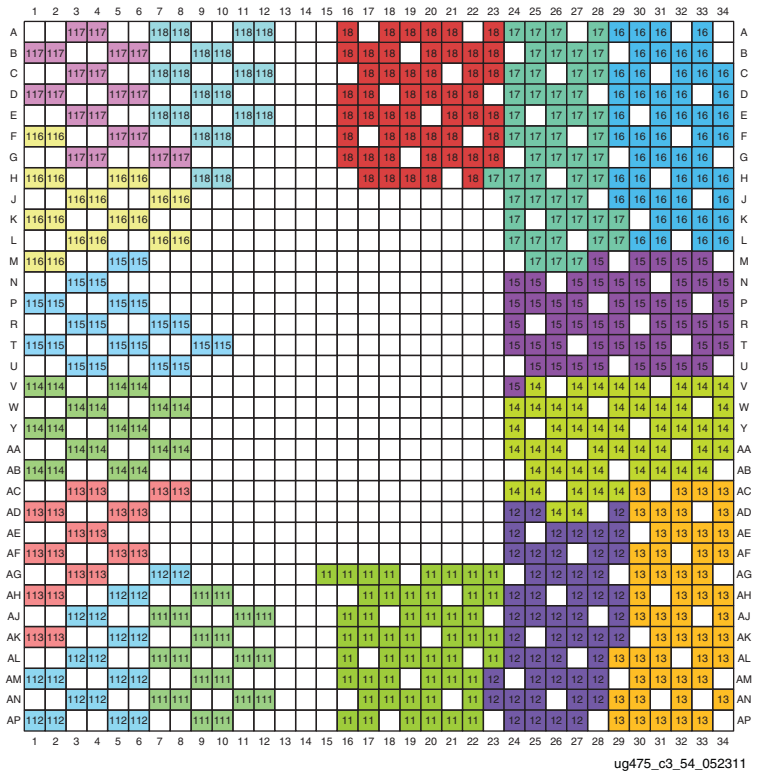


Figure 3-130: **FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T I/O Banks**

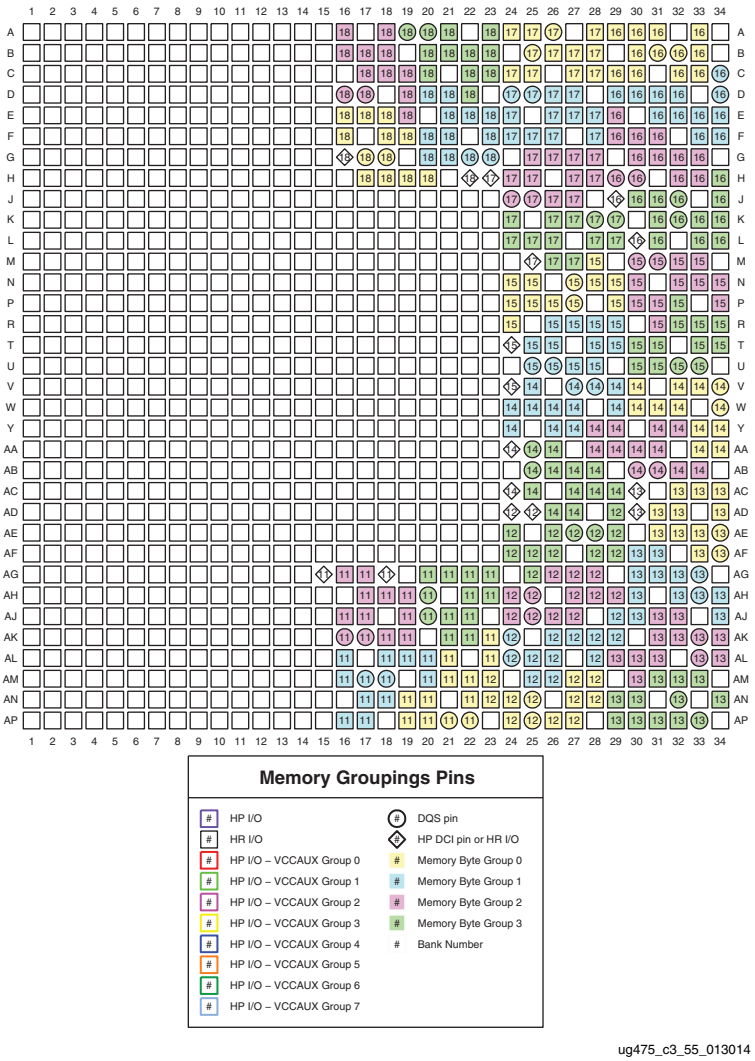


Figure 3-131: **FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T Memory Groupings**

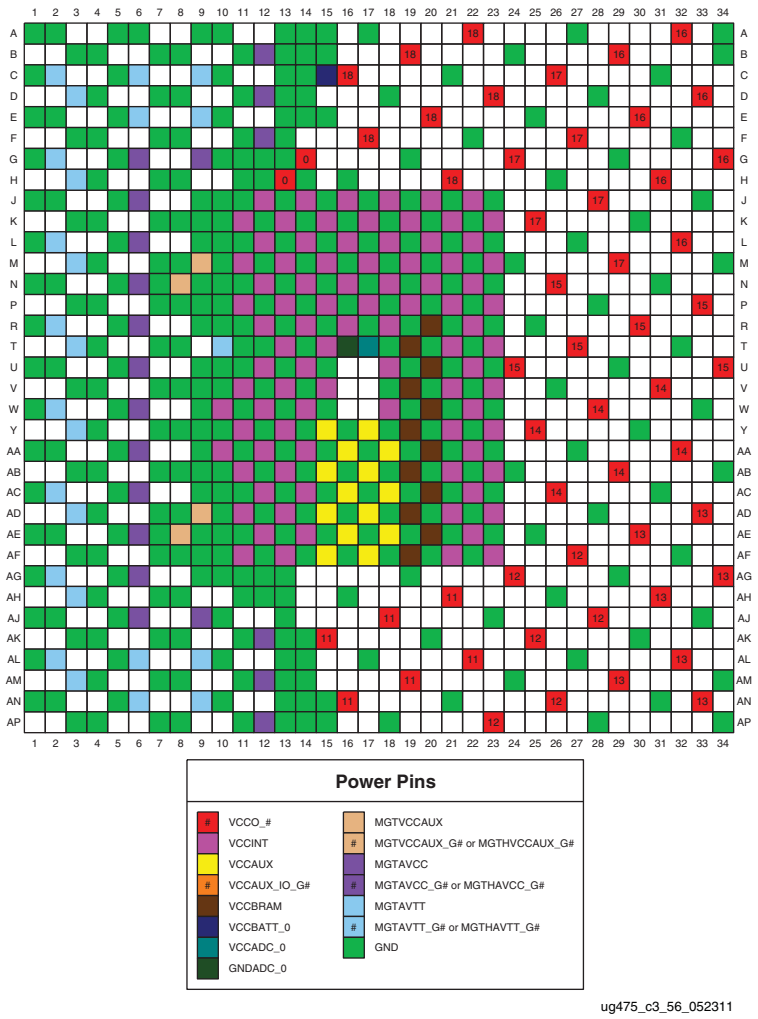


Figure 3-132: **FF1156, FFG1156, and FFV1156 Packages—XC7K420T and XC7K480T Power and GND Placement**

Virtex-7 FPGAs Device Diagrams

Table 3-4: **Virtex-7 T FPGAs Device Diagrams Cross Reference**

Device	FF1157 FFG1157 RF1157	FF1761 FFG1761 RF1761	FL1925 FLG1925	FH1761 FHG1761
XC7V585T	page 167	page 171		
XC7V2000T			page 175	page 179

Table 3-5: **Virtex-7 XT FPGAs Device Diagrams Cross Reference**

Device	FF1157 FFG1157 FFV1157 RF1157	FF1158 FFG1158 FFV1158 RF1158	FF1761 FFG1761 FFV1761 RF1761	FF1926 FFG1926	FF1927 FFG1927 FFV1927	FF1928 FFG1928	FF1930 FFG1930 RF1930	FL1926 FLG1926	FL1928 FLG1928	FL1930 FLG1930
XC7VX330T	page 183		page 187							
XC7VX415T	page 183	page 191			page 195					
XC7VX485T	page 199	page 203	page 207		page 211		page 215			
XC7VX550T		page 191			page 227					
XC7VX690T	page 183	page 191	page 219	page 223	page 227		page 231			
XC7VX980T				page 223		page 235	page 239			
XC7VX1140T								page 243	page 247	page 251

FF1157, FFG1157, and RF1157 Packages—XC7V585T

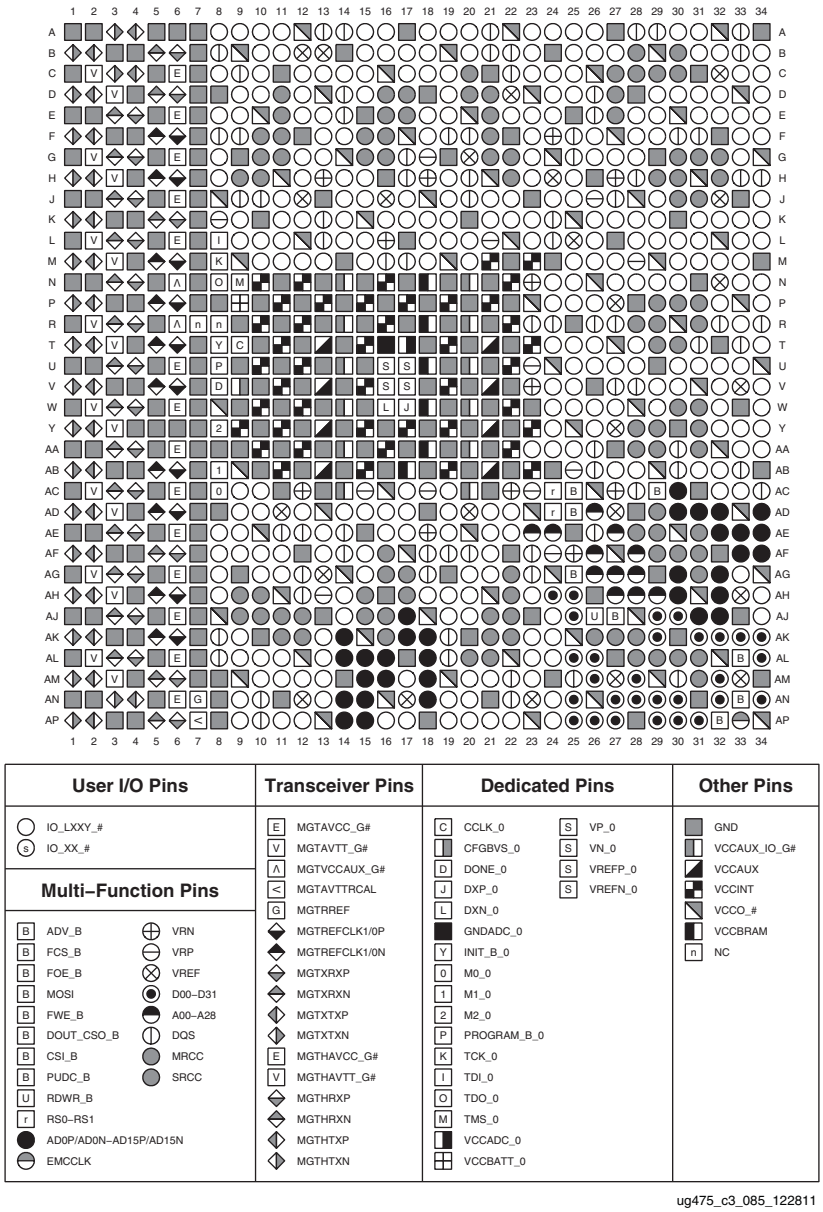


Figure 3-133: **FF1157, FFG1157, and RF1157 Packages—XC7V585T Pinout Diagram**

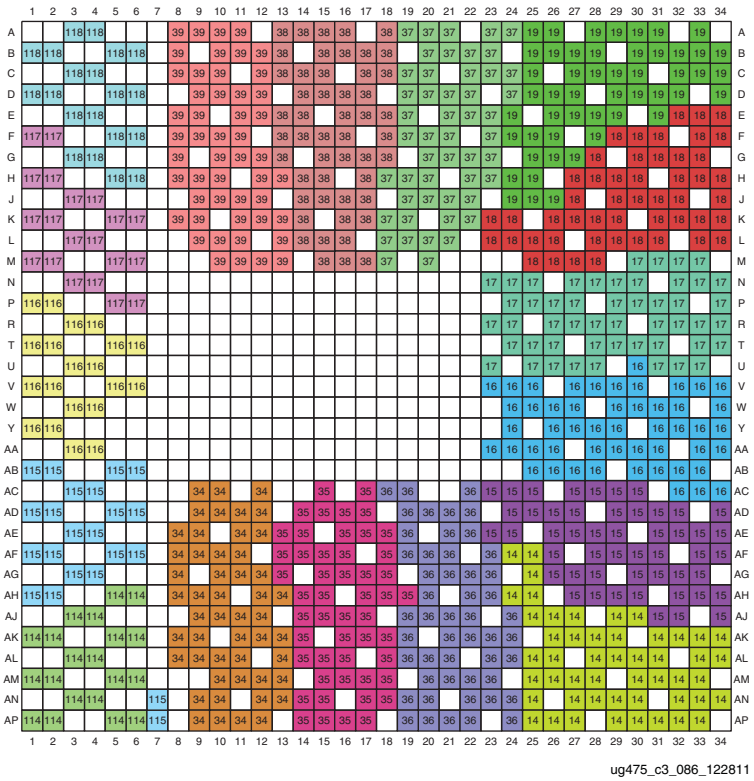


Figure 3-134: **FF1157, FFG1157, and RF1157 Packages—XC7V585T I/O Banks**

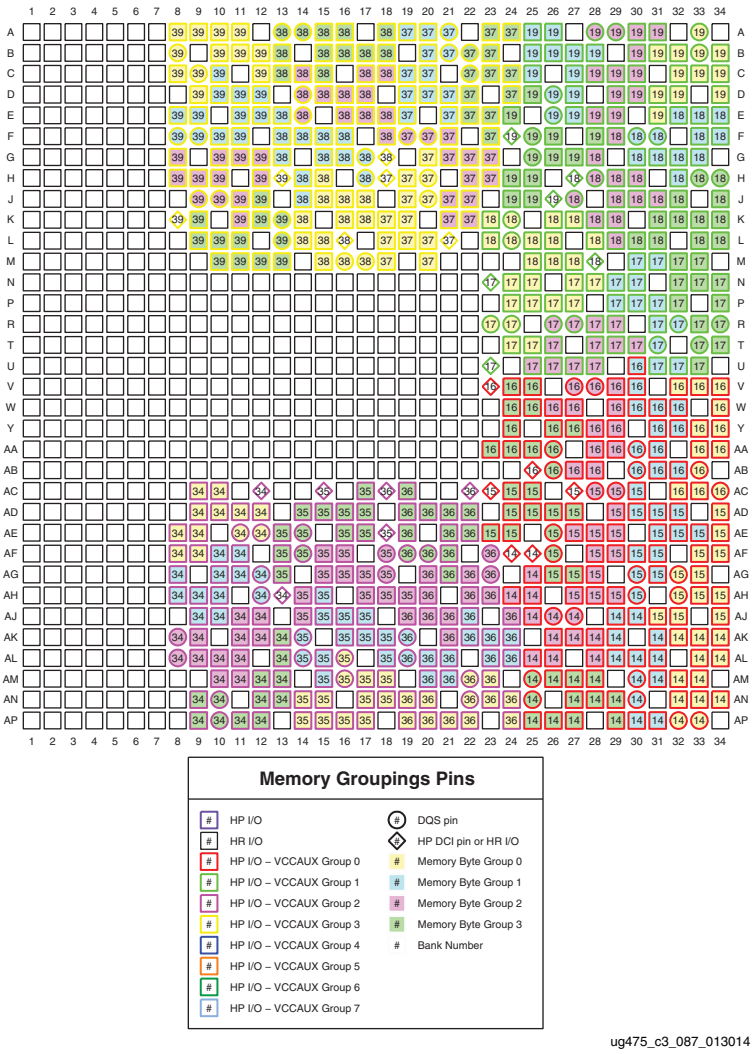


Figure 3-135: **FF1157, FFG1157, and RF1157 Packages—XC7V585T Memory Groupings**

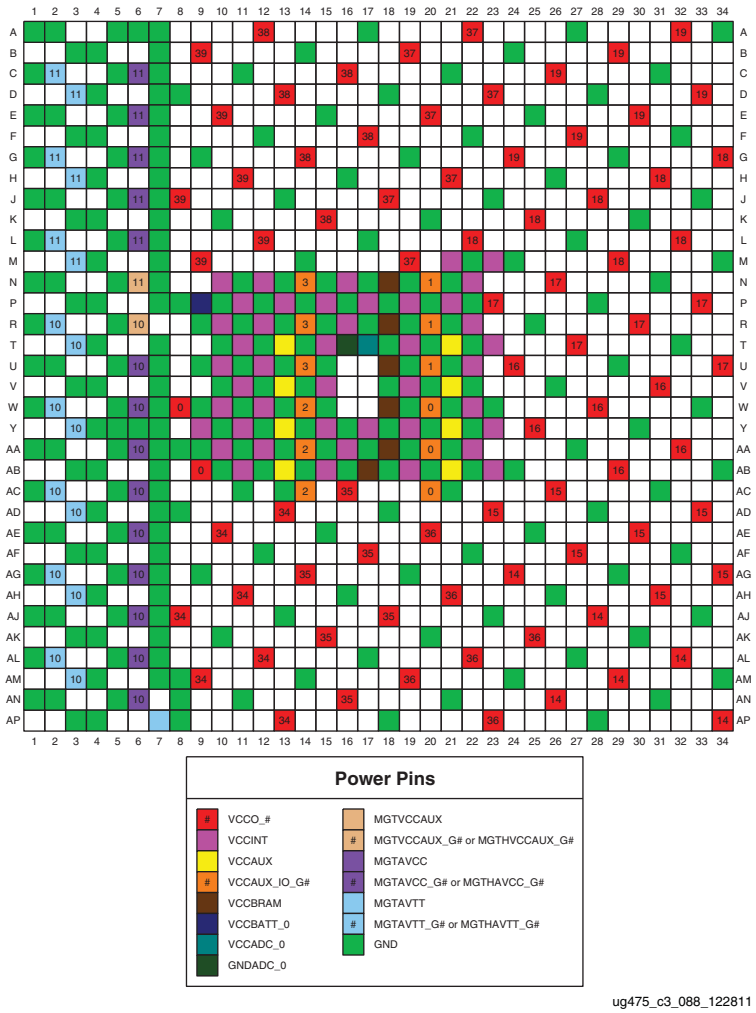


Figure 3-136: **FF1157, FFG1157, and RF1157 Packages—XC7V585T Power and GND Placement**

FF1761, FFG1761, and RF1761 Packages—XC7V585T

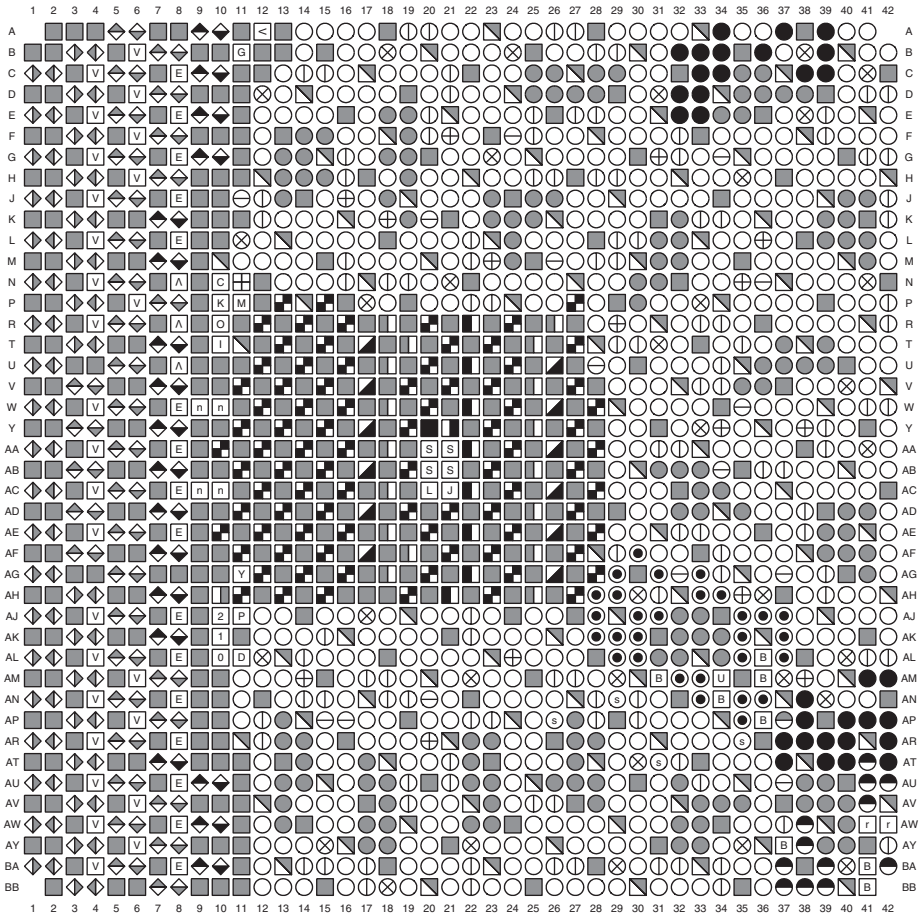


Figure 3-137: **FF1761, FFG1761, and RF1761 Packages—XC7V585T Pinout Diagram**

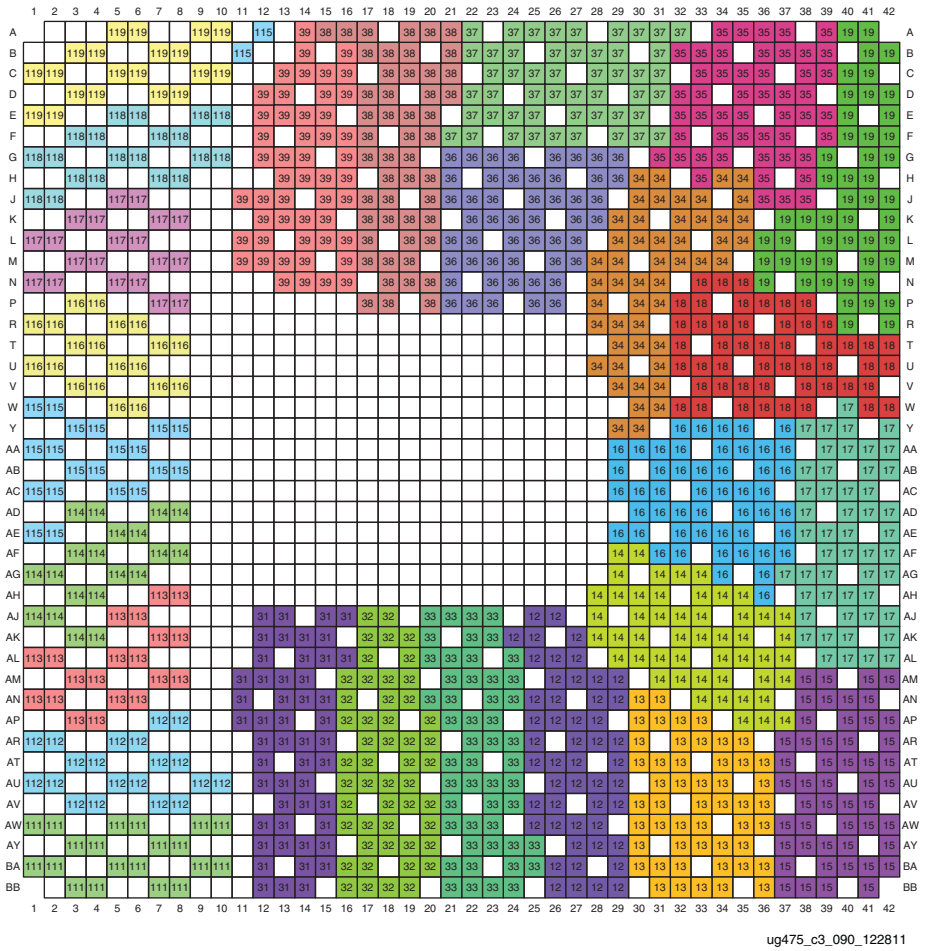


Figure 3-138: **FF1761, FFG1761, and RF1761 Packages—XC7V585T I/O Banks**

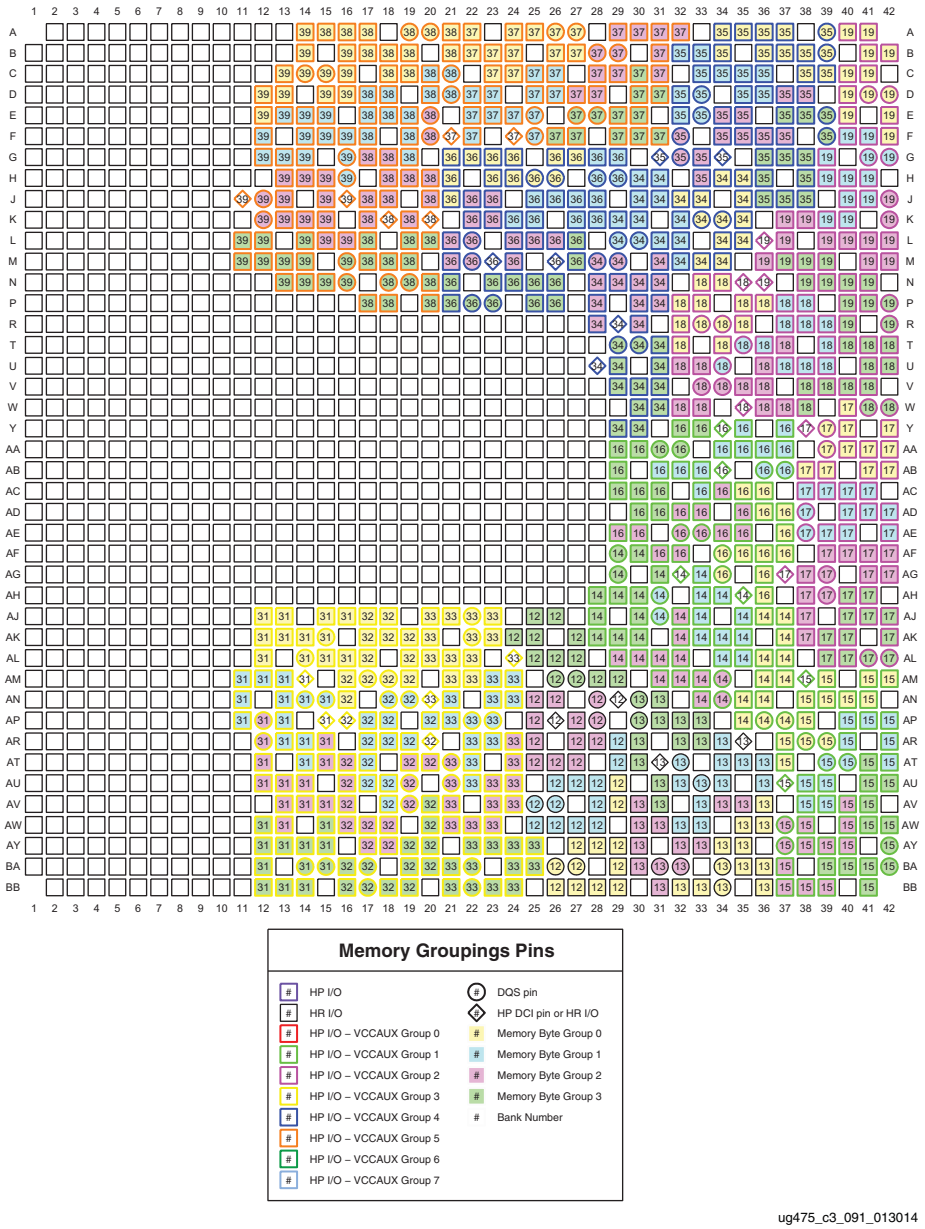


Figure 3-139: **FF1761, FFG1761, and RF1761 Packages—XC7V585T Memory Groupings**

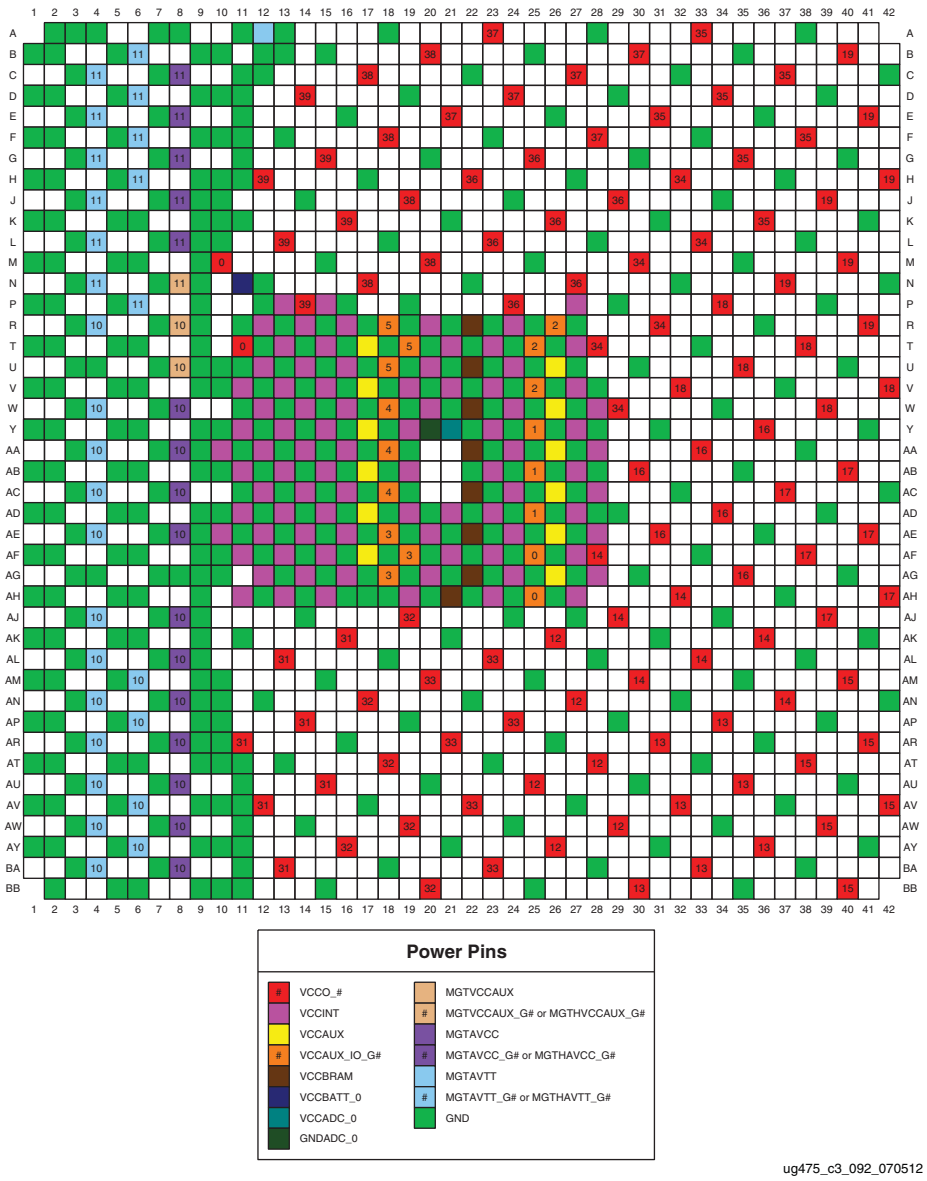


Figure 3-140: **FF1761, FFG1761, and RF1761 Packages—XC7V585T Power and GND Placement**

FL1925 and FLG1925 Packages—XC7V2000T

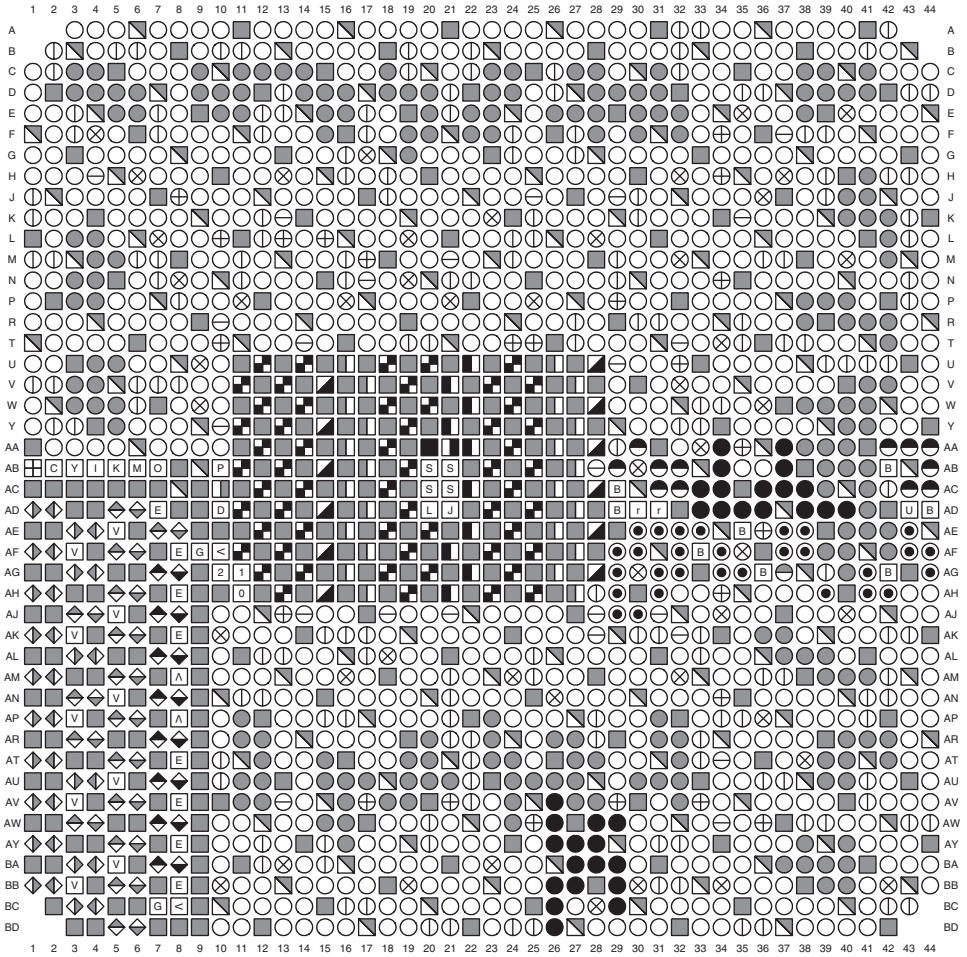


Figure 3-141: **FL1925 and FLG1925 Packages—XC7V2000T Pinout Diagram**

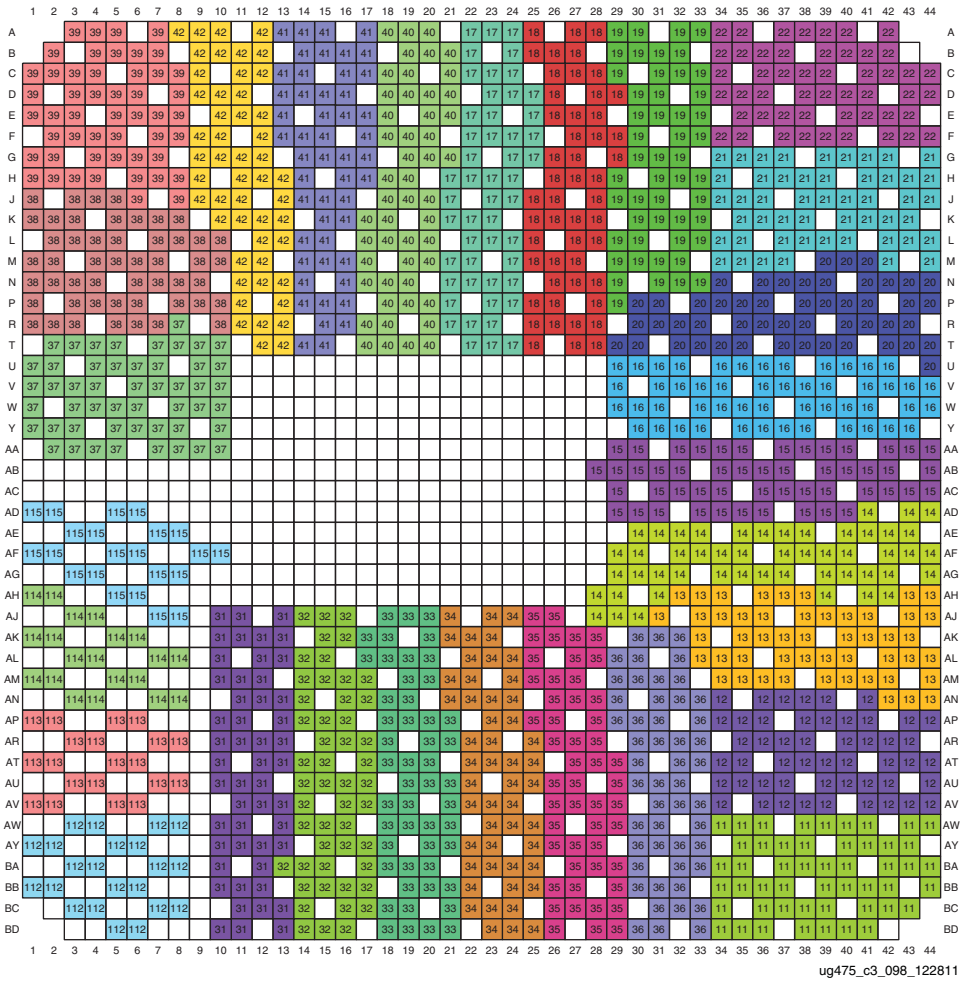


Figure 3-142: **FL1925 and FLG1925 Packages—XC7V2000T I/O Banks**

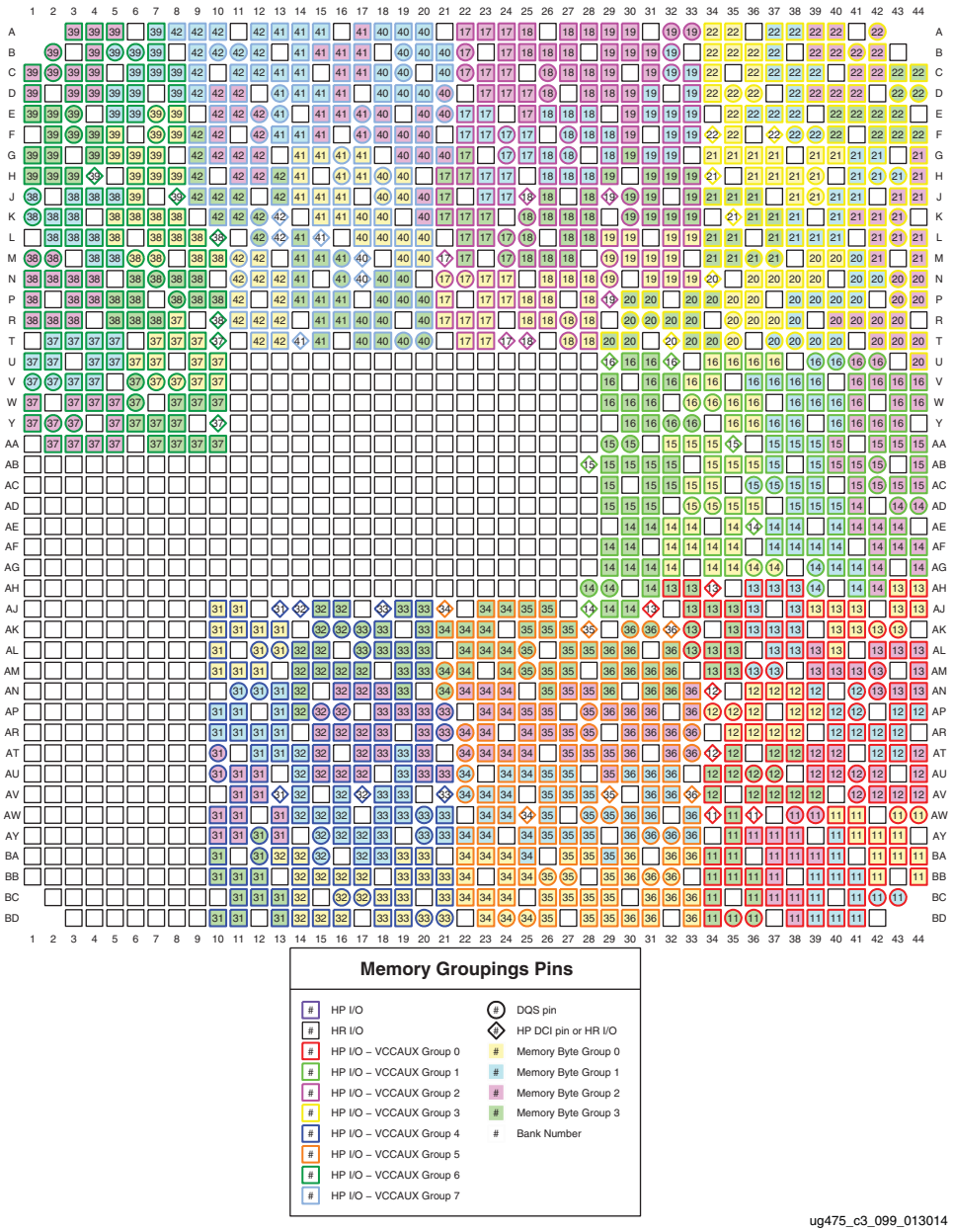


Figure 3-143: **FL1925 and FLG1925 Packages—XC7V2000T Memory Groupings**

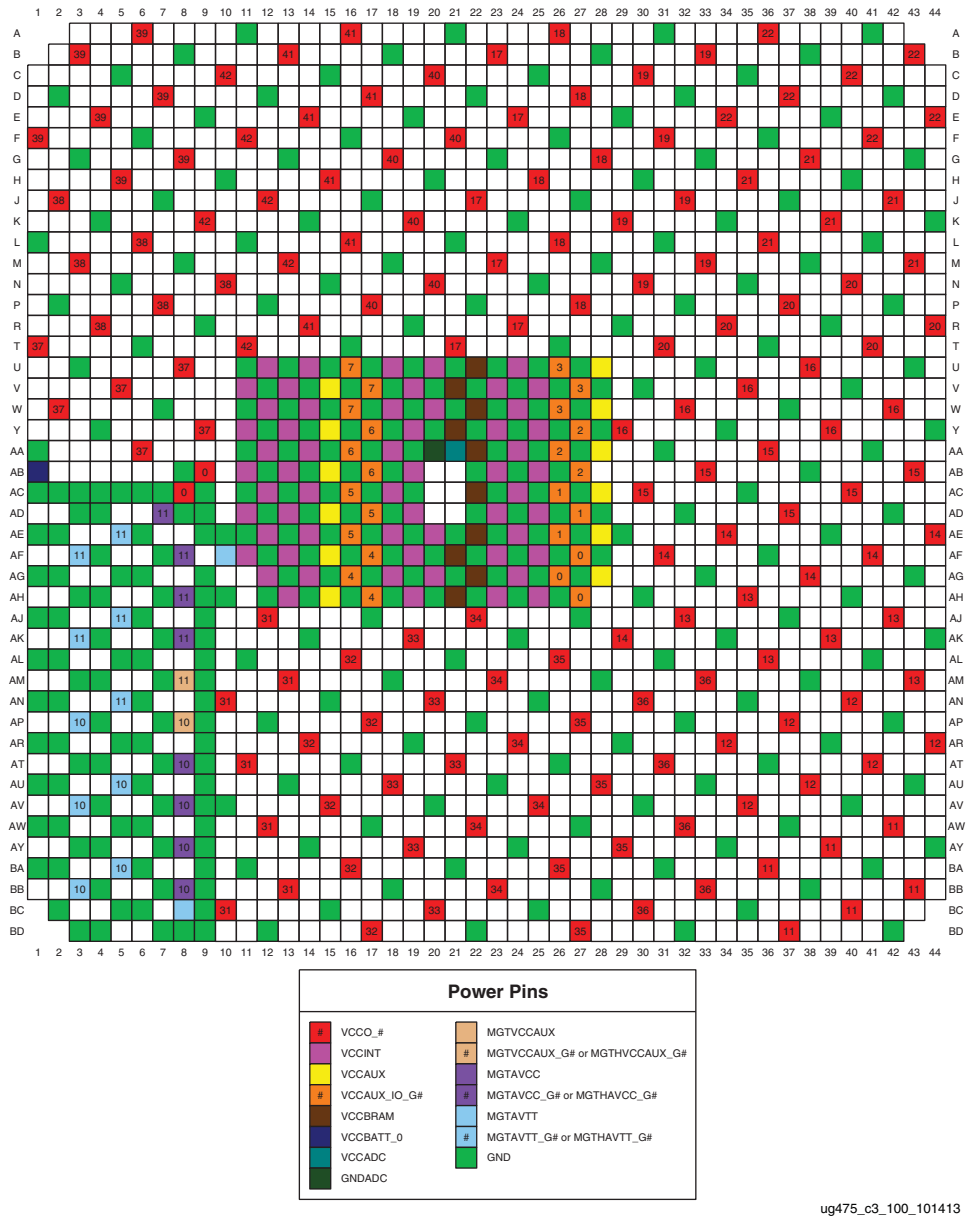


Figure 3-144: **FL1925 and FLG1925 Packages—XC7V2000T Power and GND Placement**

FH1761 and FHG1761 Packages—XC7V2000T

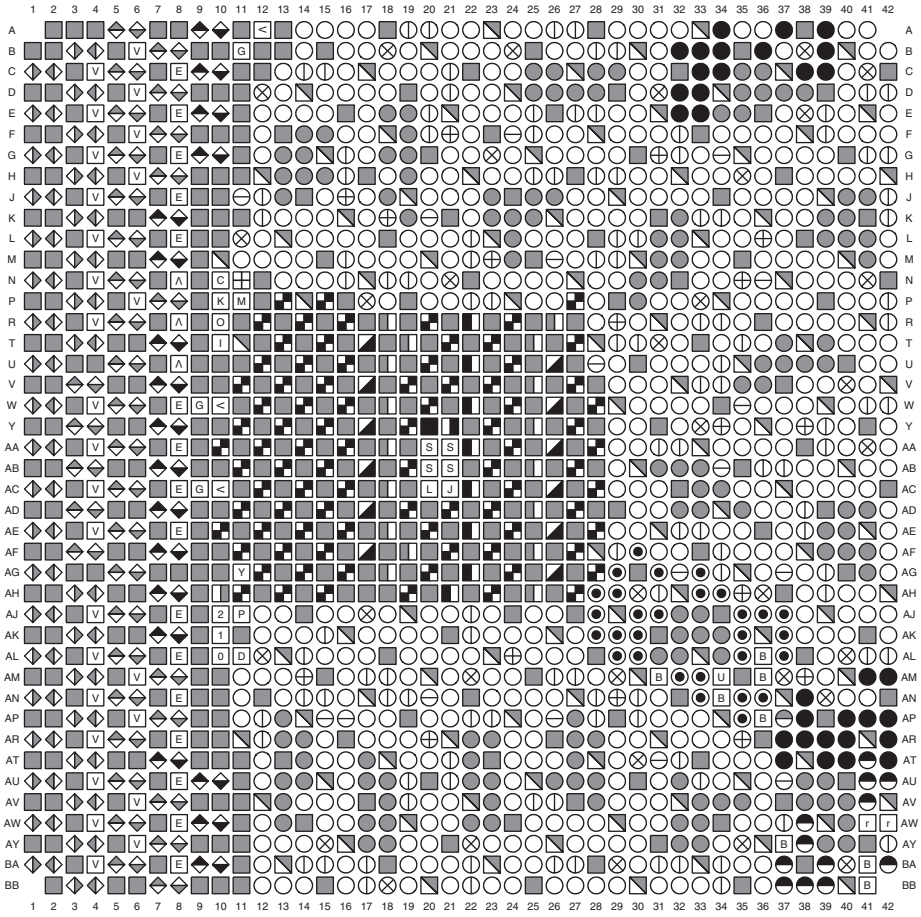


Figure 3-145: **FH1761 and FHG1761 Packages—XC7V2000T Pinout Diagram**

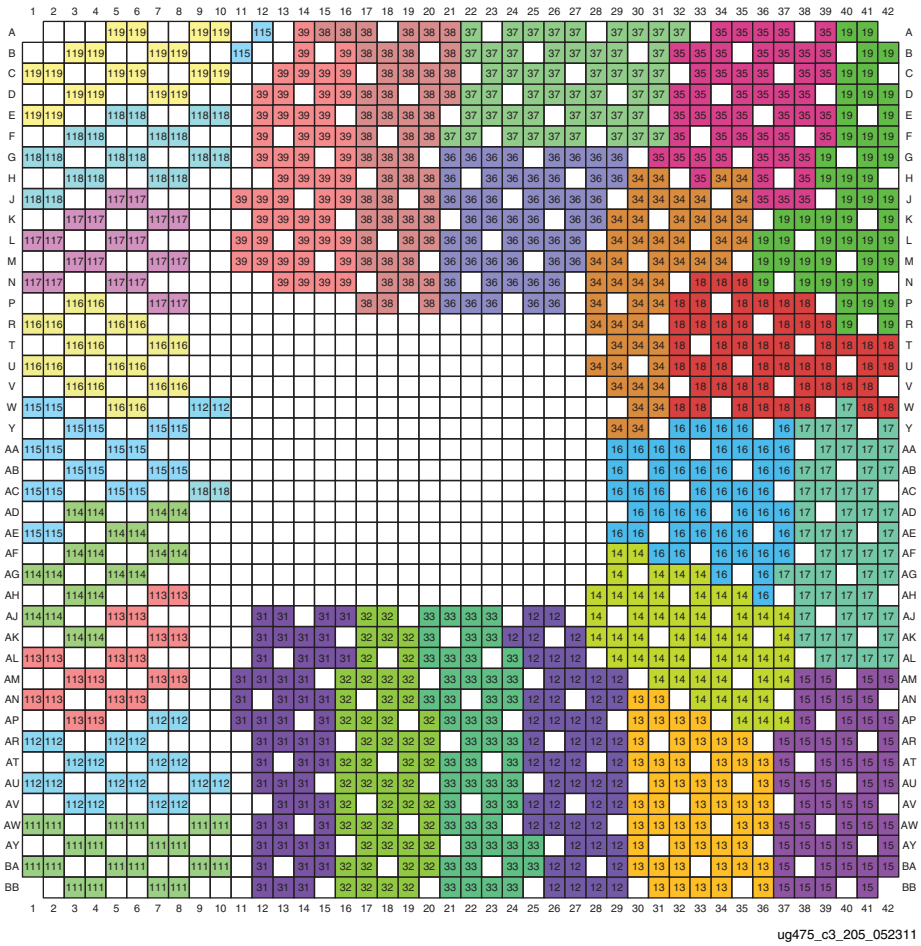


Figure 3-146: **FH1761 and FHG1761 Packages—XC7V2000T I/O Banks**

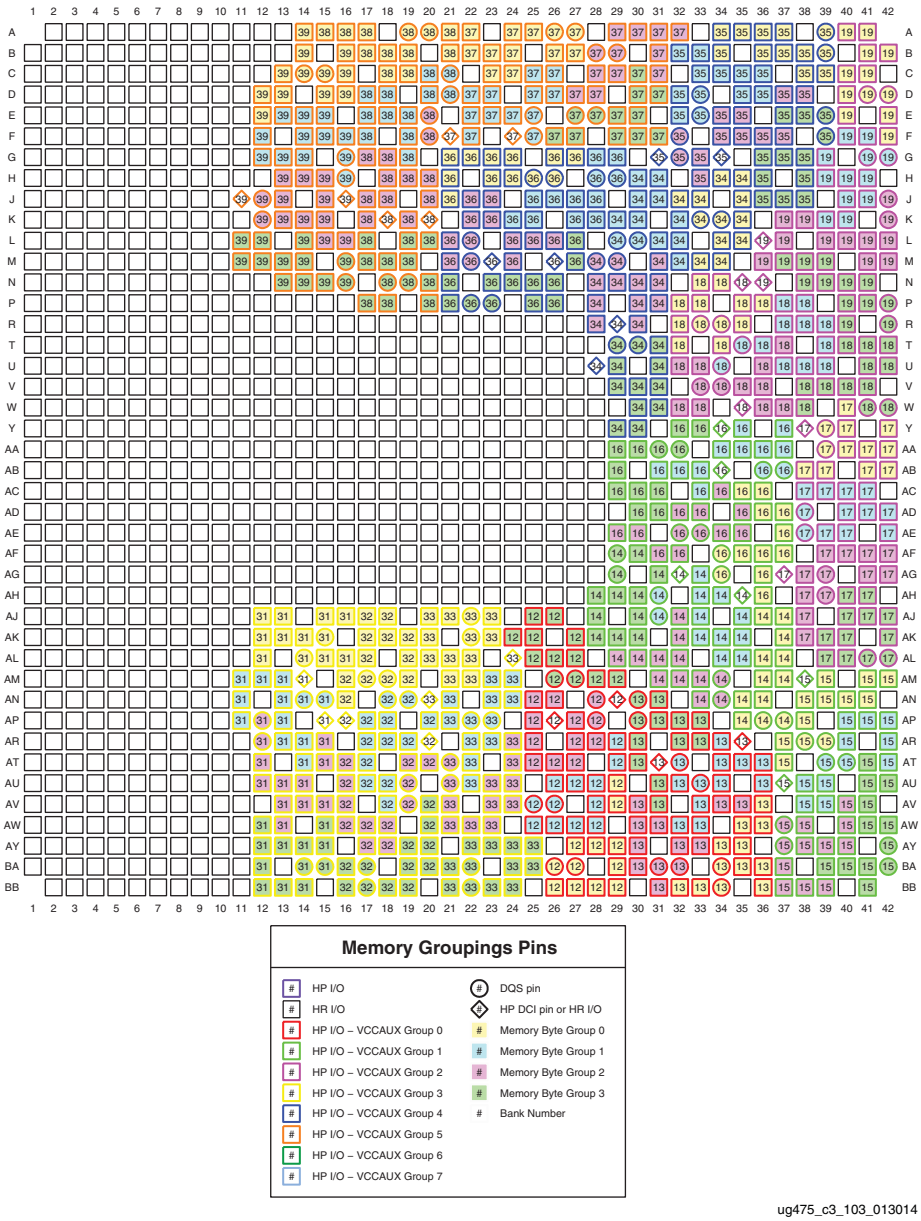


Figure 3-147: **FH1761 and FHG1761 Packages—XC7V2000T Memory Groupings**

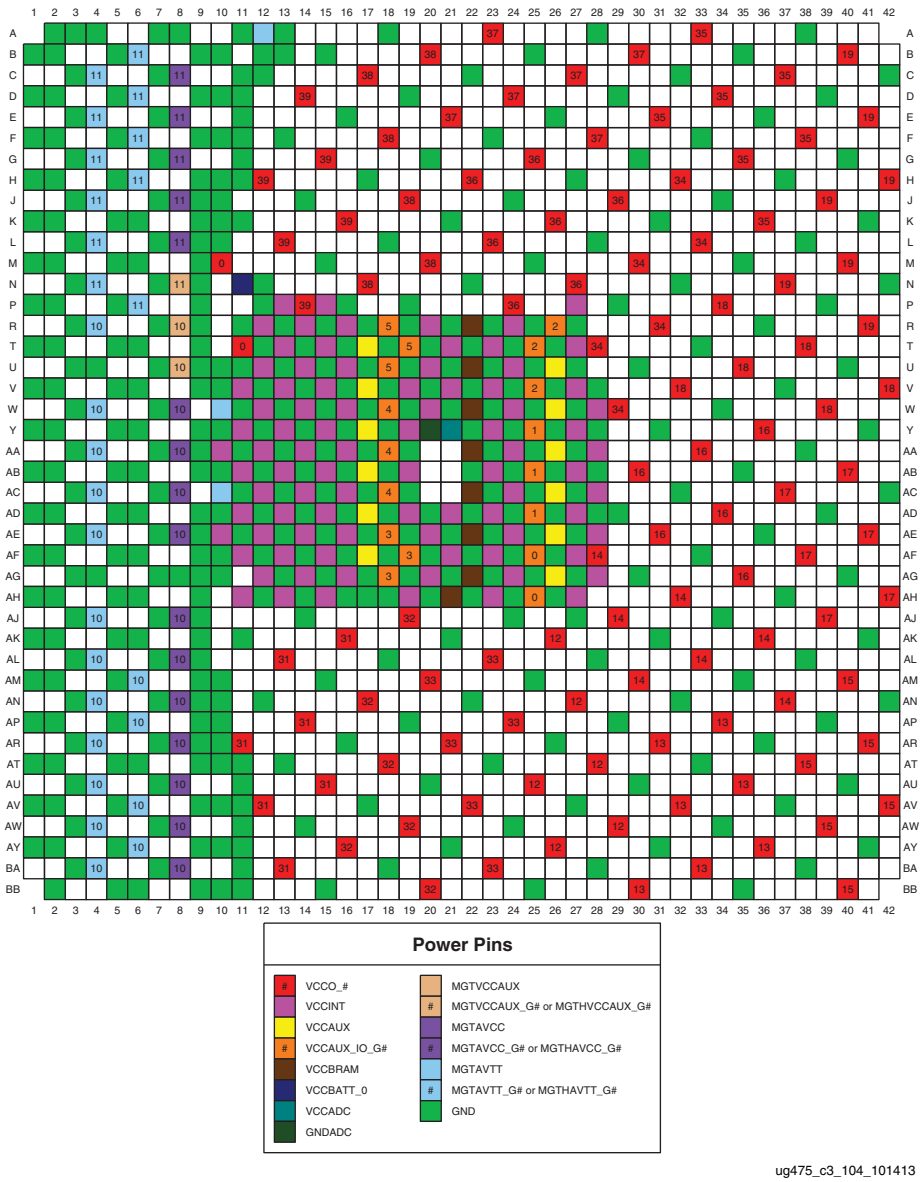


Figure 3-148: **FH1761 and FHG1761 Packages—XC7V2000T Power and GND Placement**

FF1157, FFG1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T

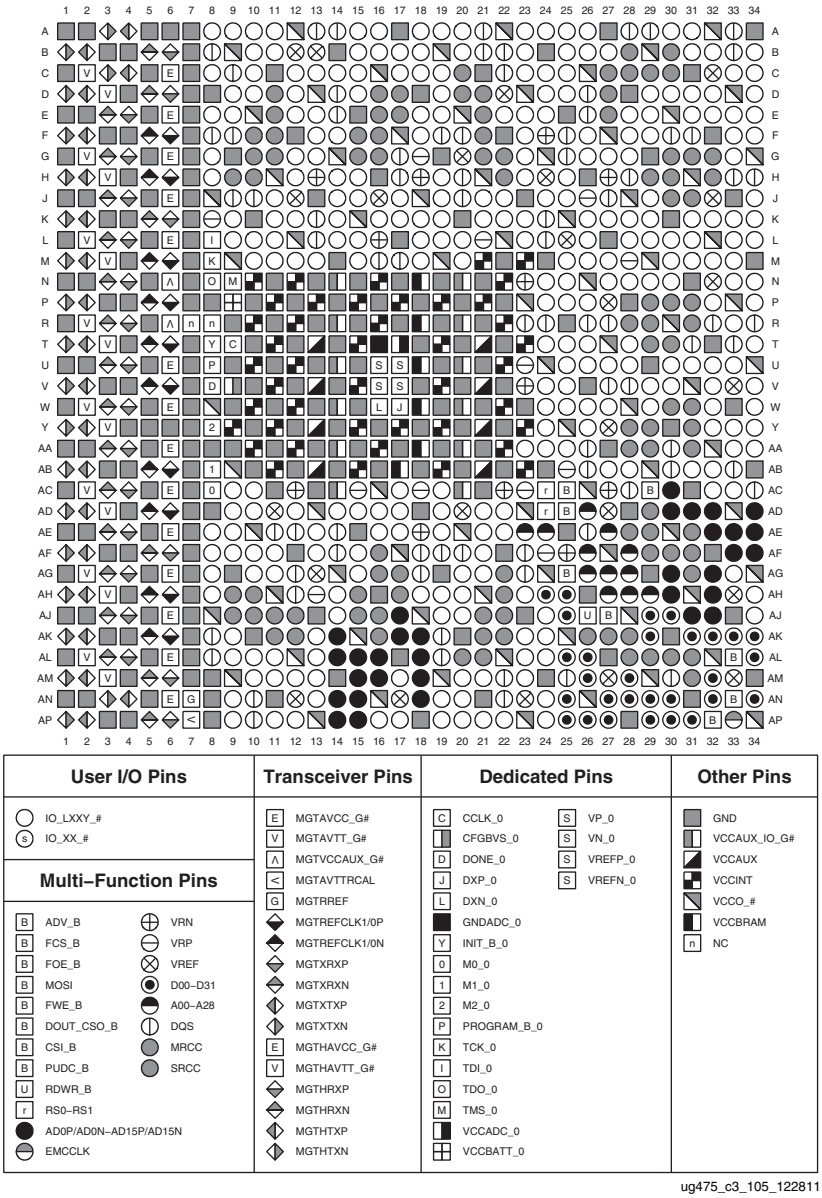


Figure 3-149: **FF1157, FFG1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T Pinout Diagram**

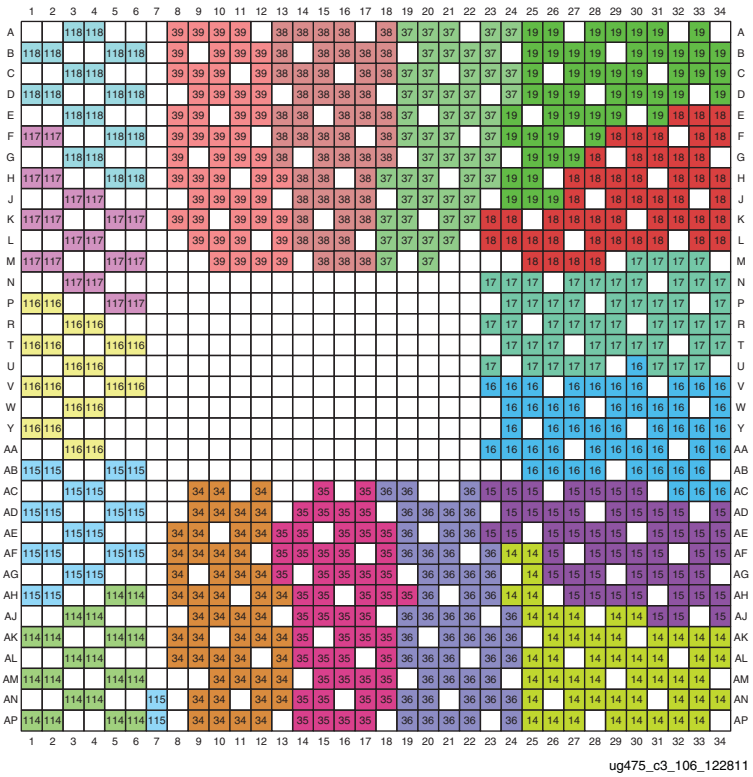


Figure 3-150: **FF1157, FFG1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T I/O Banks**

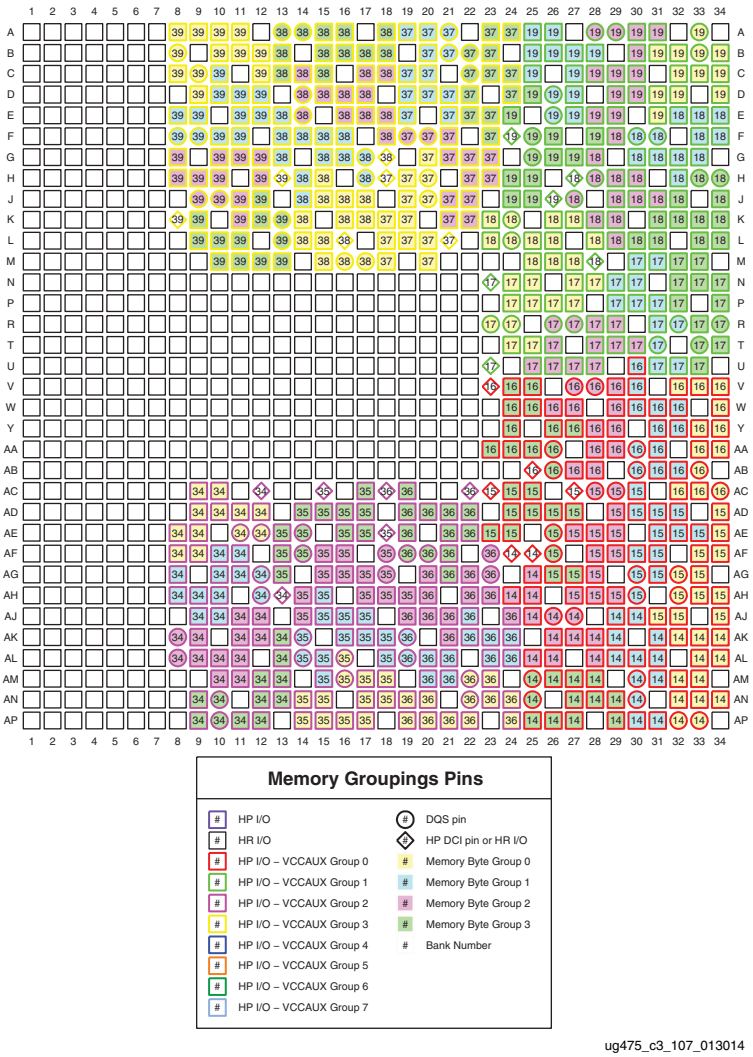


Figure 3-151: **FF1157, FFG1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T Memory Groupings**

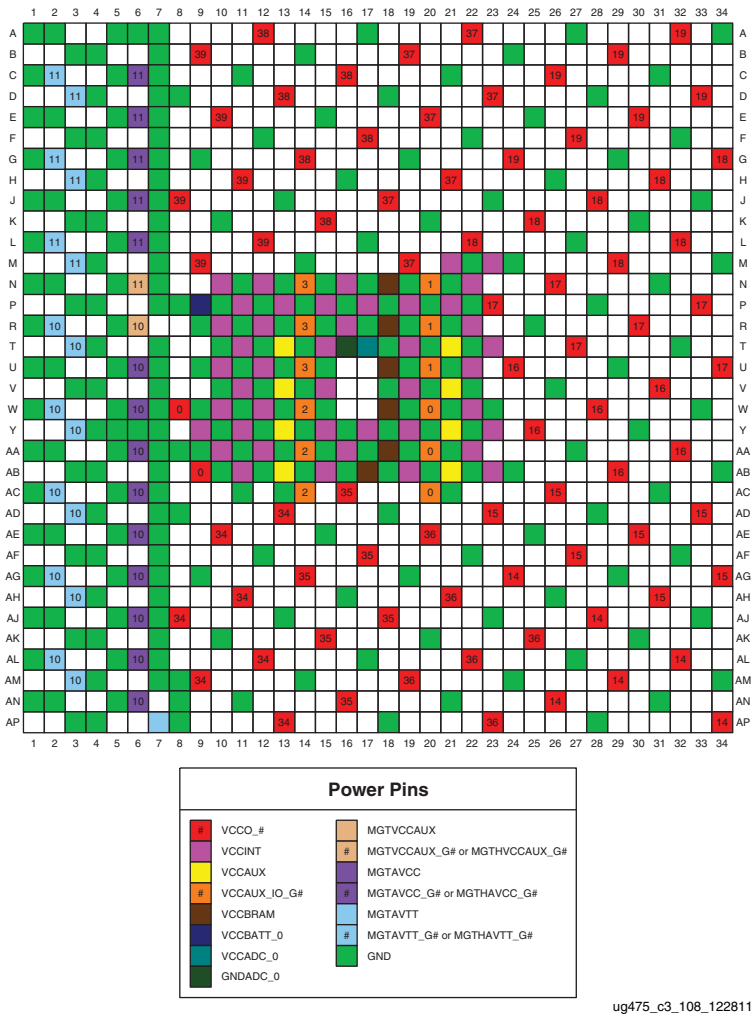


Figure 3-152: **FF1157, FFG1157, and RF1157 Packages—XC7VX330T, XC7VX415T, and XC7VX690T Power and GND Placement**

FF1761, FFG1761, and RF1761 Packages—XC7VX330T

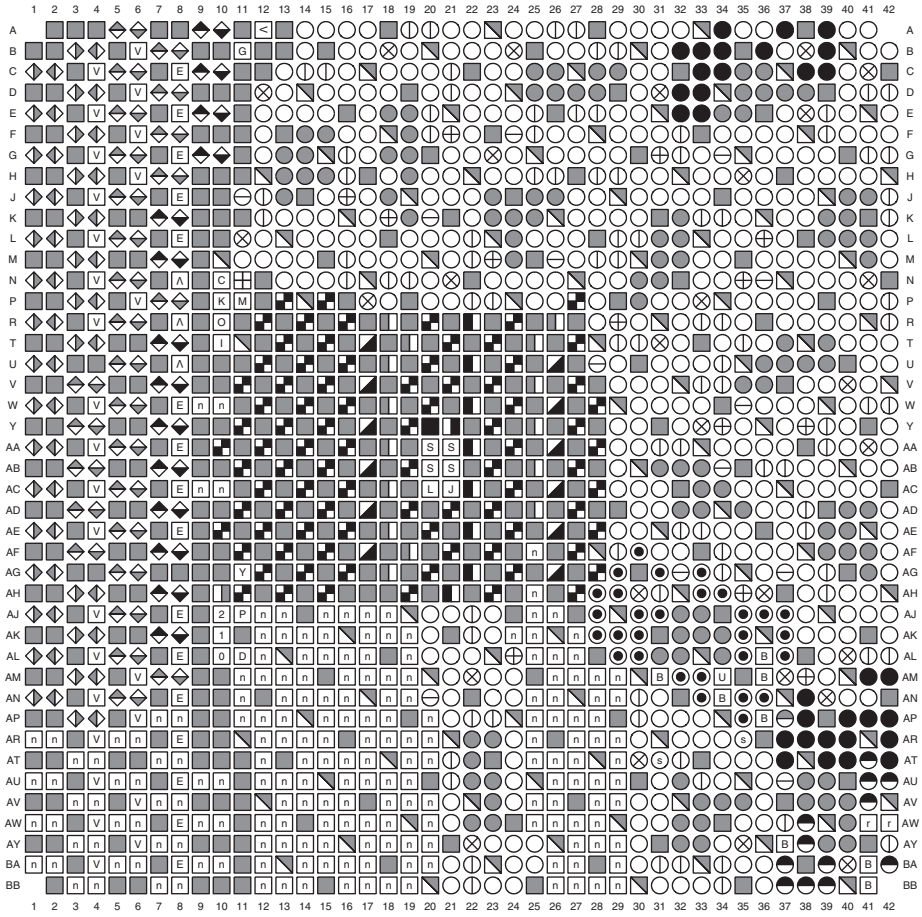


Figure 3-153: **FF1761, FFG1761, and RF1761 Packages—XC7VX330T Pinout Diagram**

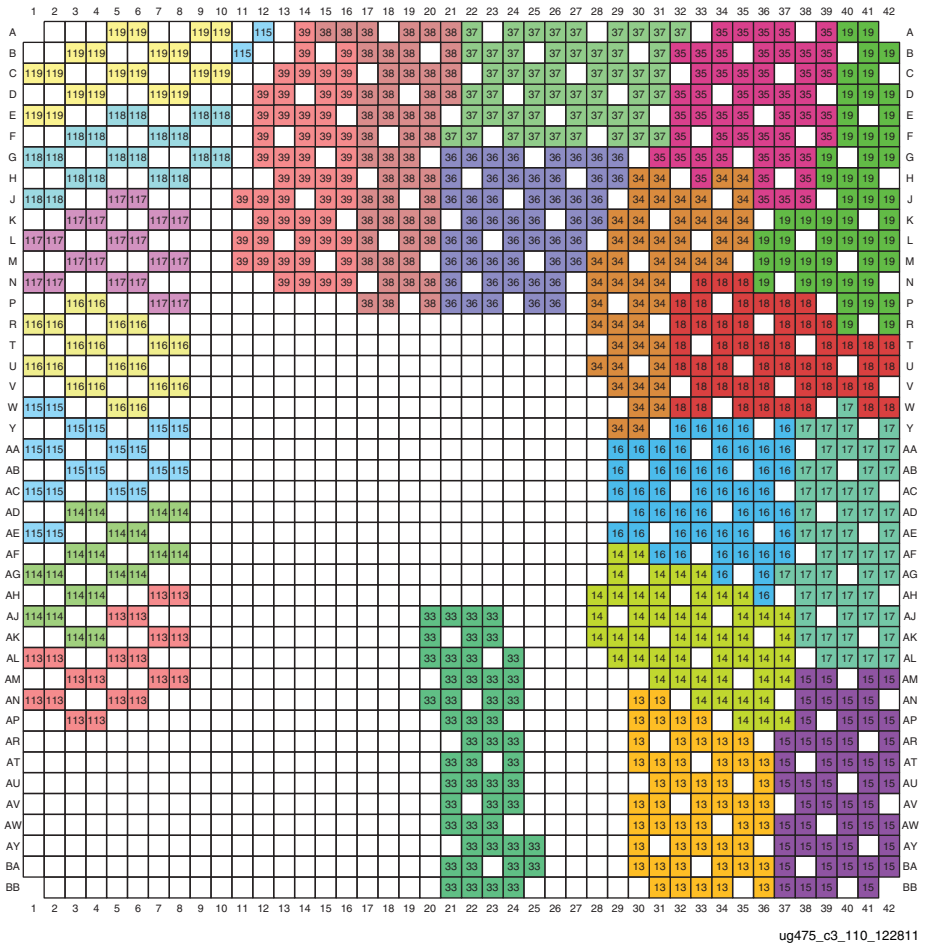


Figure 3-154: **FF1761, FFG1761, and RF1761 Packages—XC7VX330T I/O Banks**

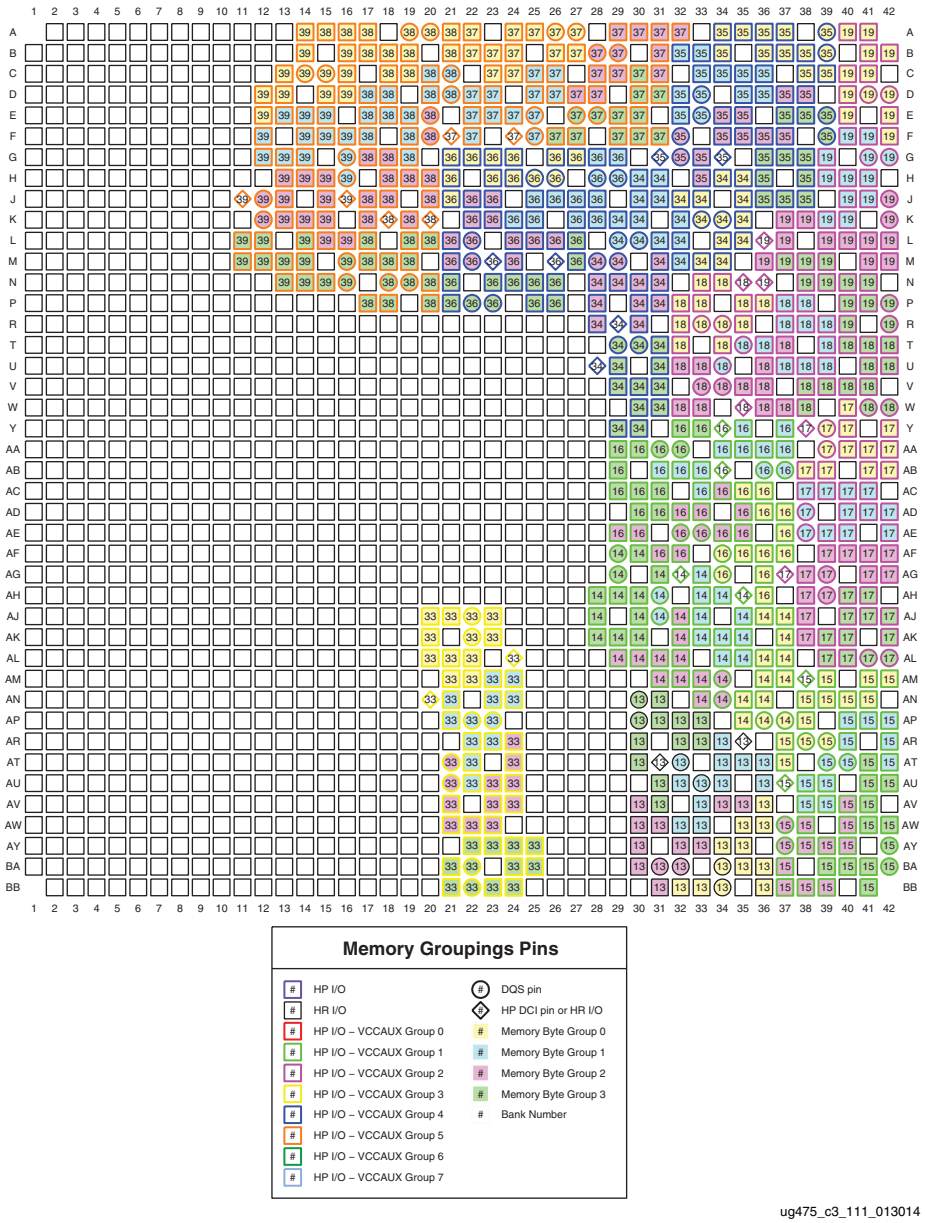


Figure 3-155: **FF1761, FFG1761, and RF1761 Packages—XC7VX330T Memory Groupings**

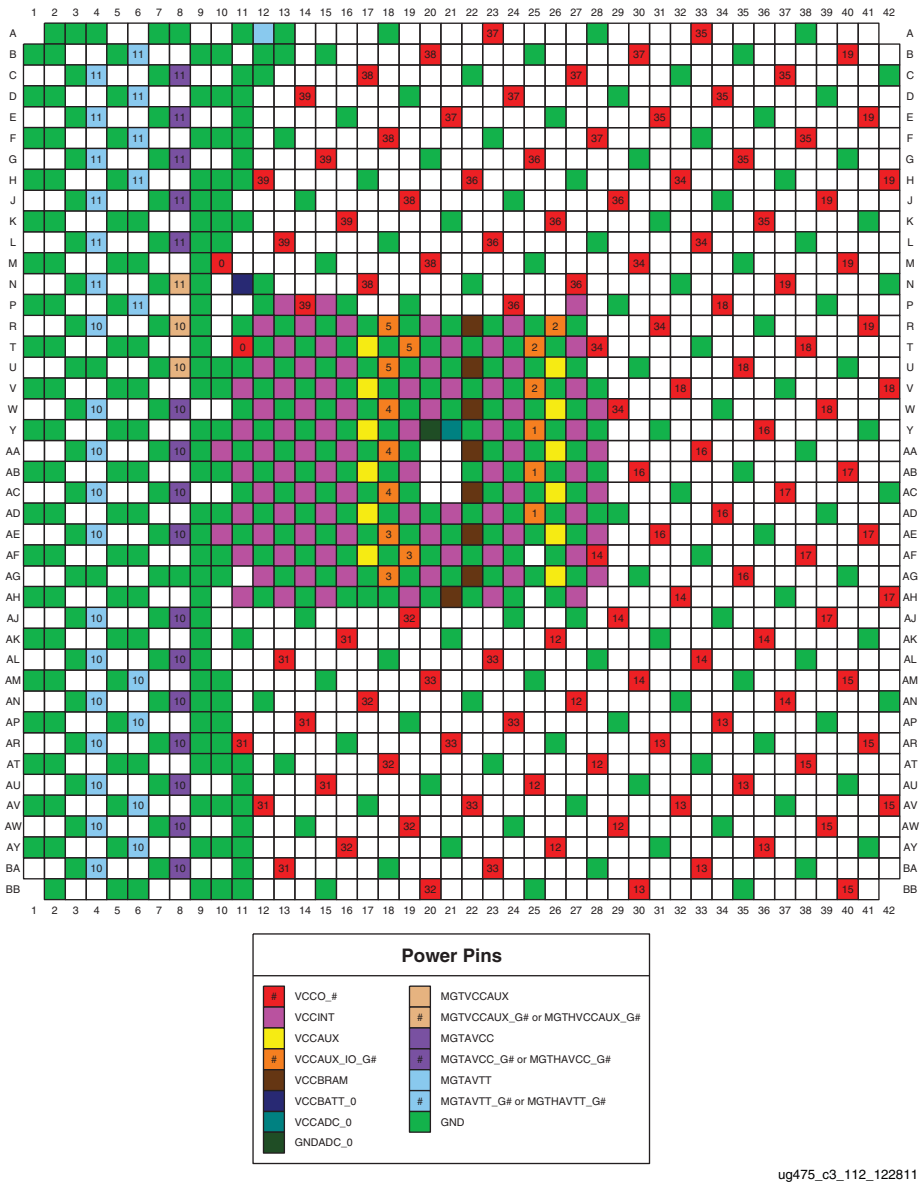


Figure 3-156: **FF1761, FFG1761, and RF1761 Packages—XC7VX330T Power and GND Placement**

FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T

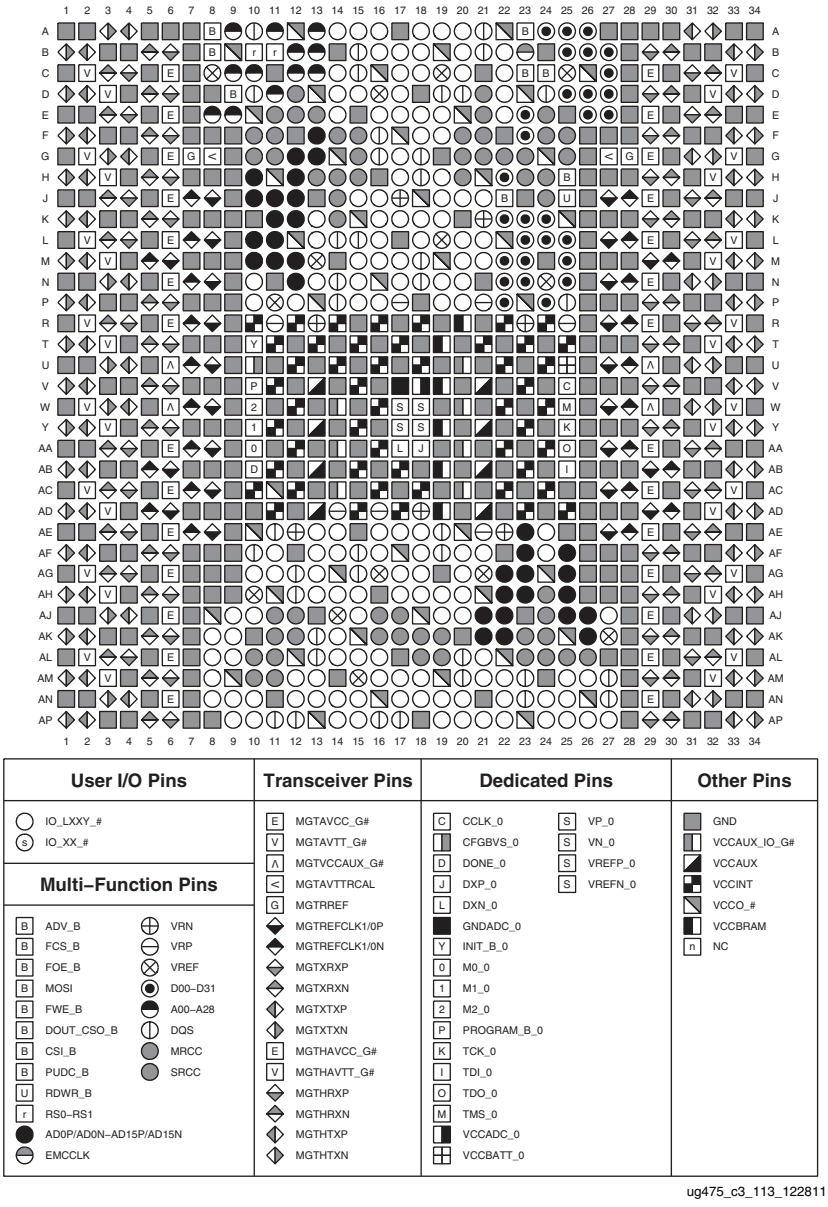


Figure 3-157: **FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T Pinout Diagram**

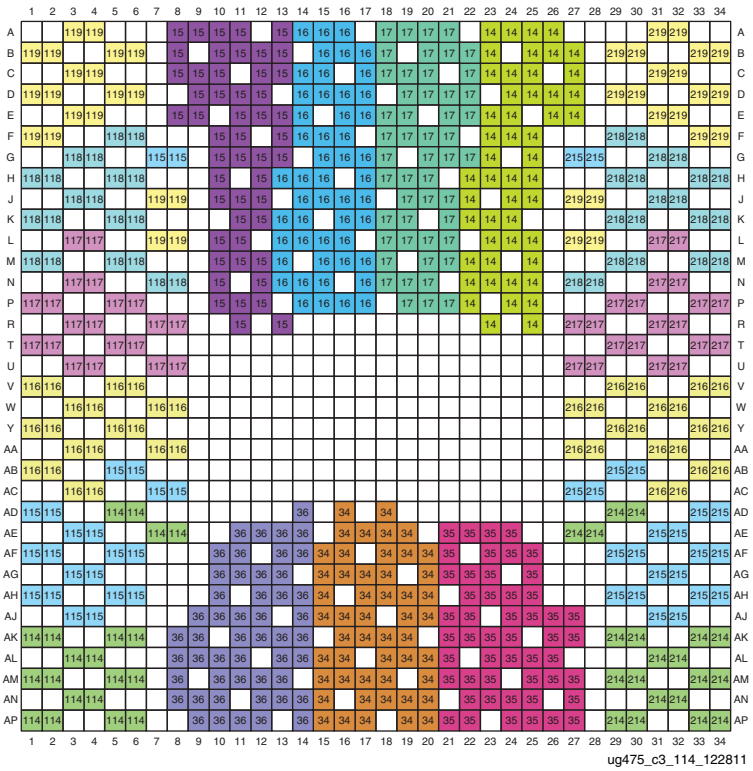


Figure 3-158: **FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T I/O Banks**

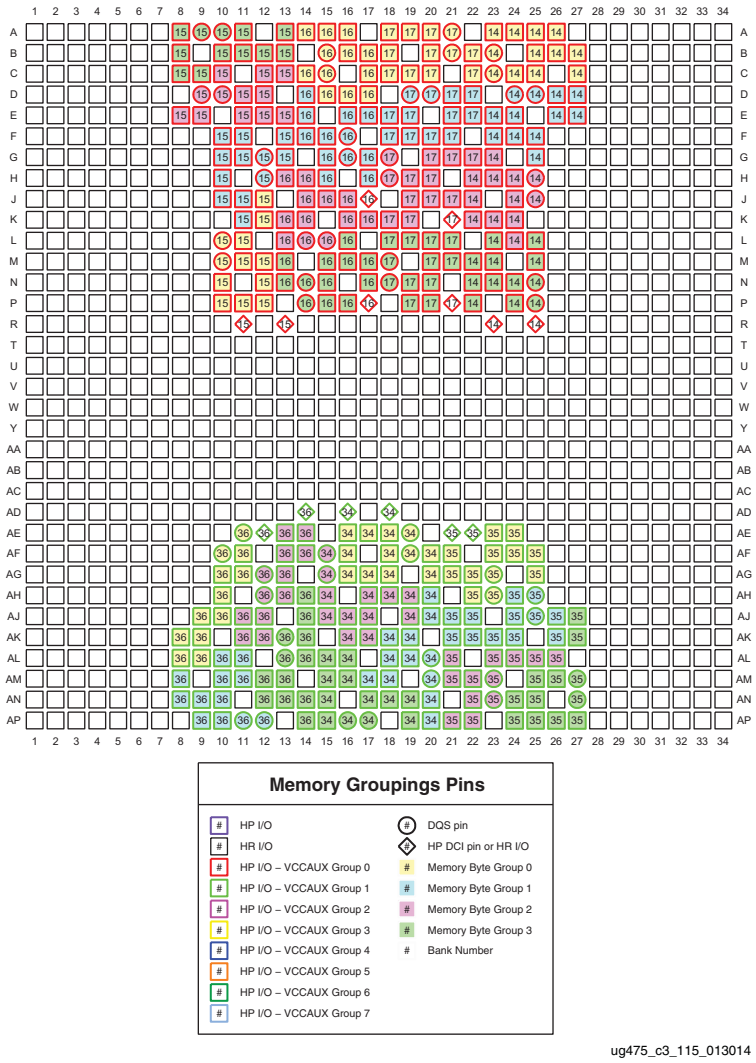


Figure 3-159: **FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T Memory Groupings**

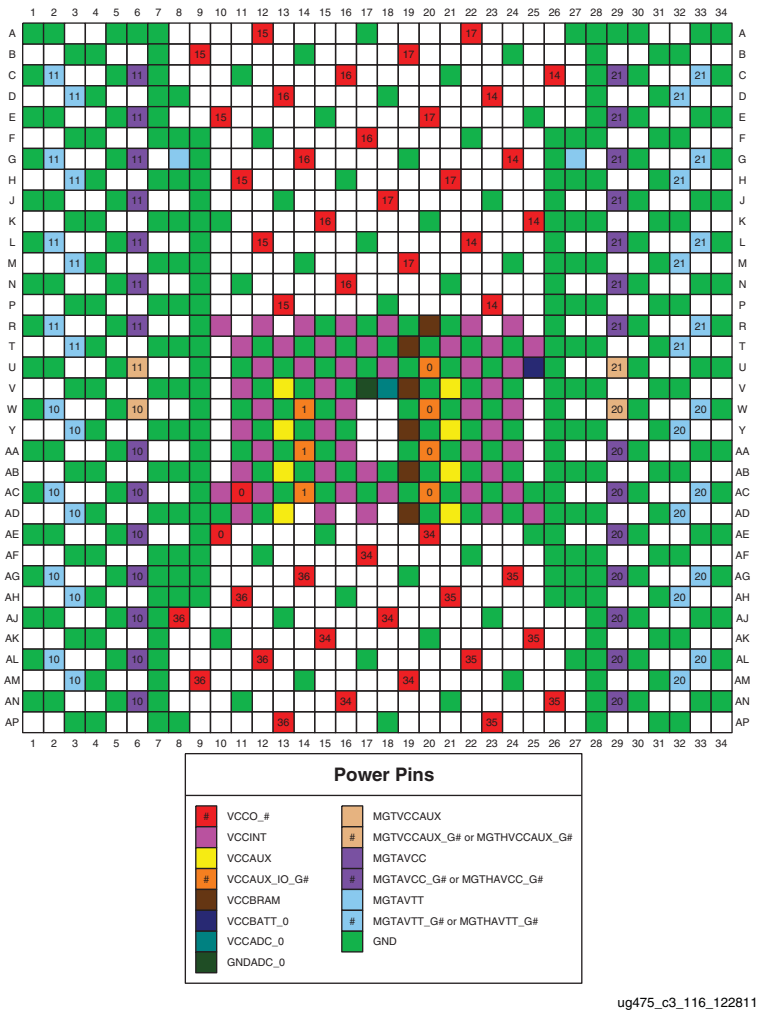


Figure 3-160: **FF1158, FFG1158, FFV1158, and RF1158 Packages—XC7VX415T, XC7VX550T, and XC7VX690T Power and GND Placement**

FF1927, FFG1927, and FFV1927 Packages—XC7VX415T

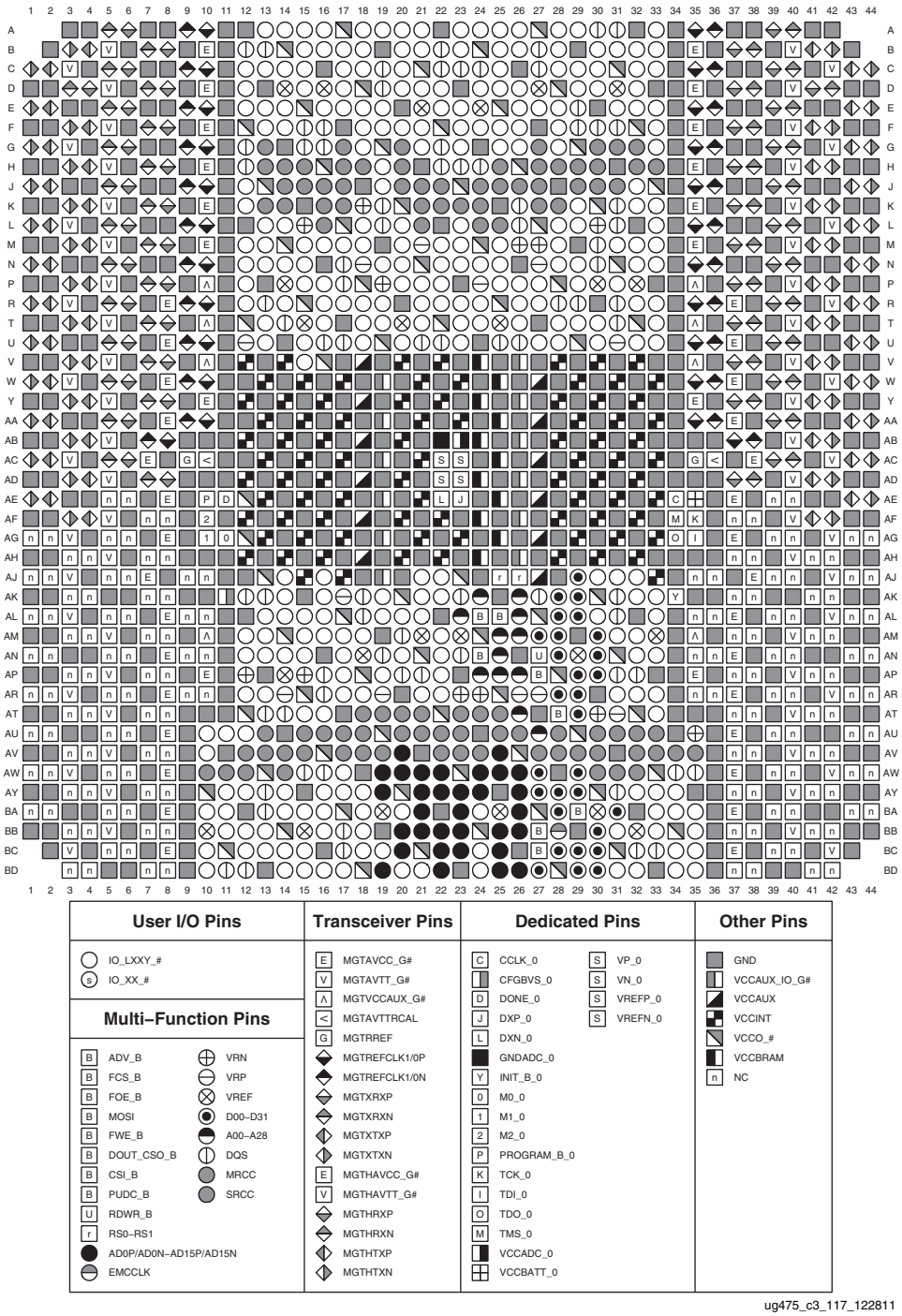


Figure 3-161: **FF1927, FFG1927, and FFV1927 Packages—XC7VX415T Pinout Diagram**

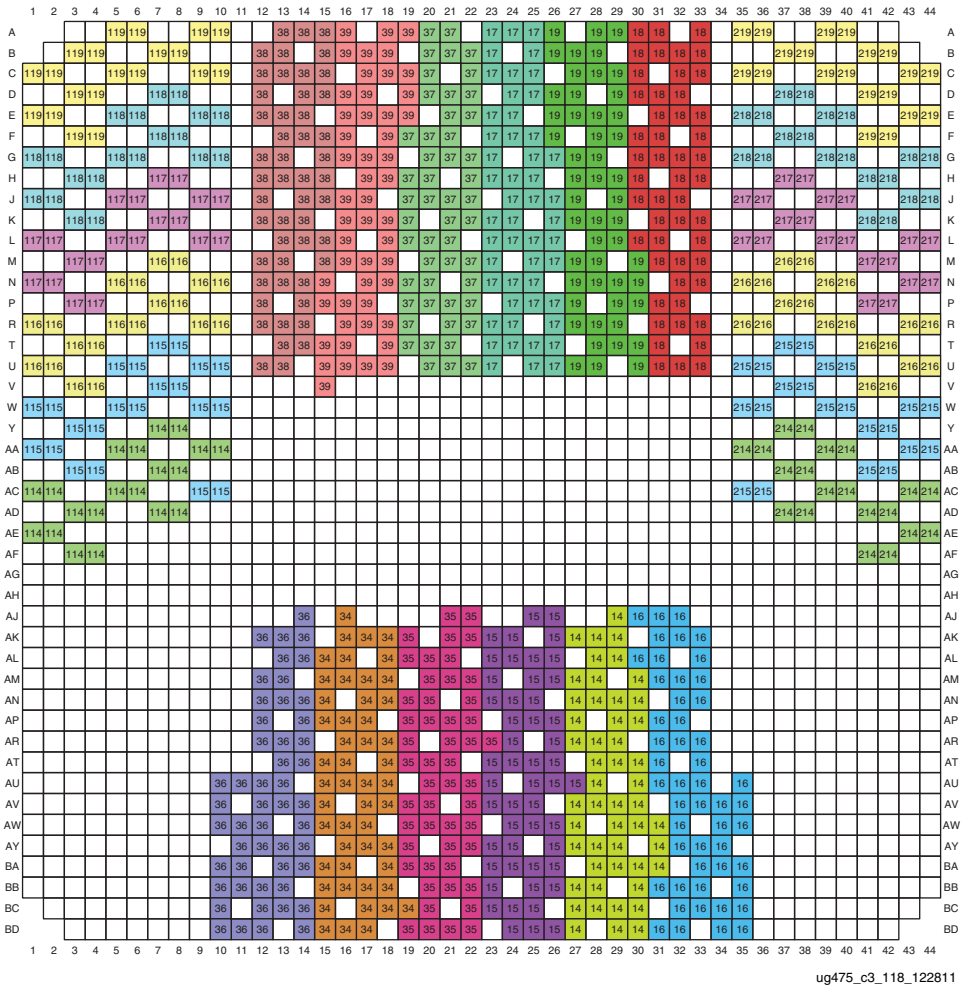


Figure 3-162: **FF1927, FFG1927, and FFV1927 Packages—XC7VX415T I/O Banks**

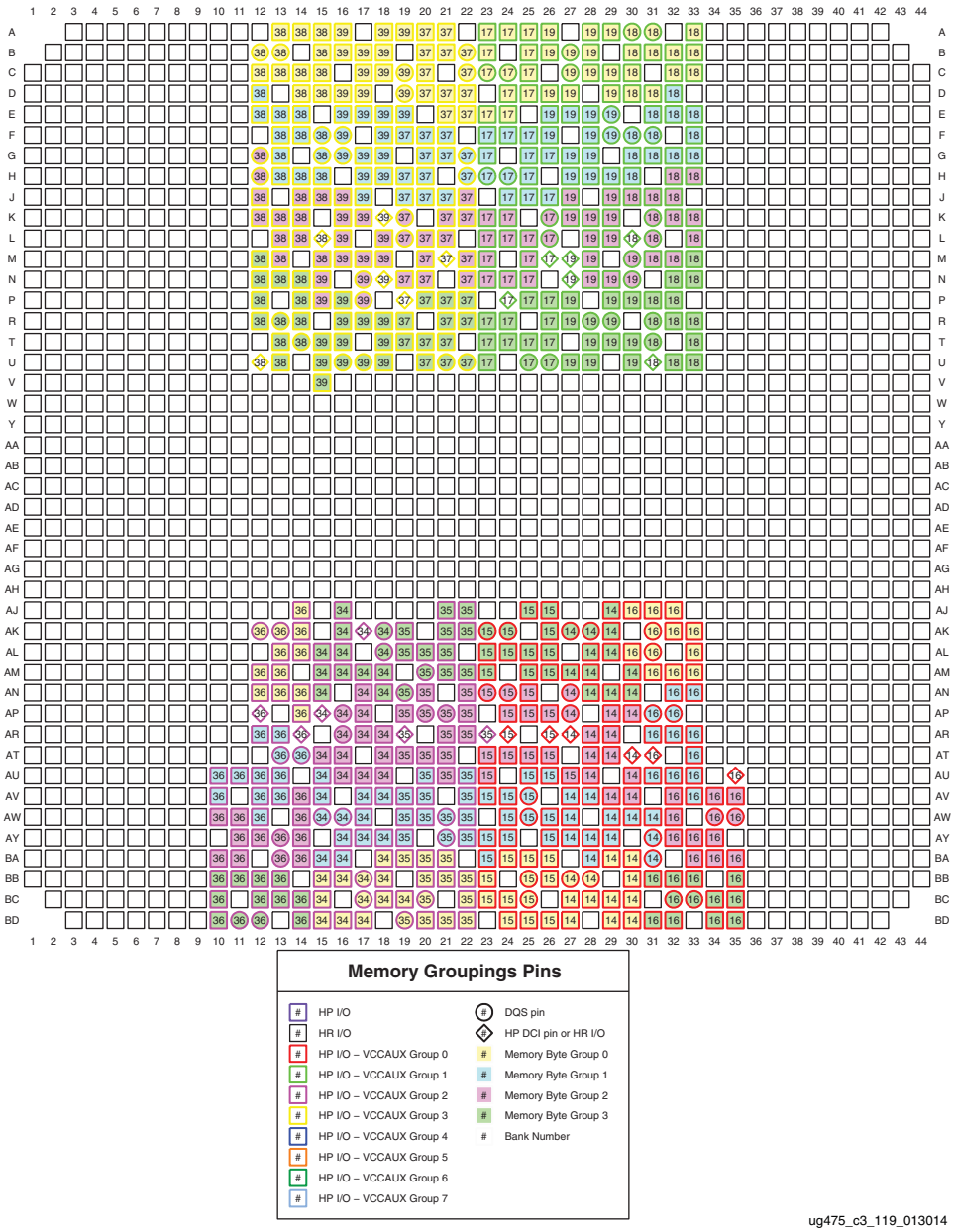


Figure 3-163: **FF1927, FFG1927, and FFV1927 Packages—XC7VX415T Memory Groupings**

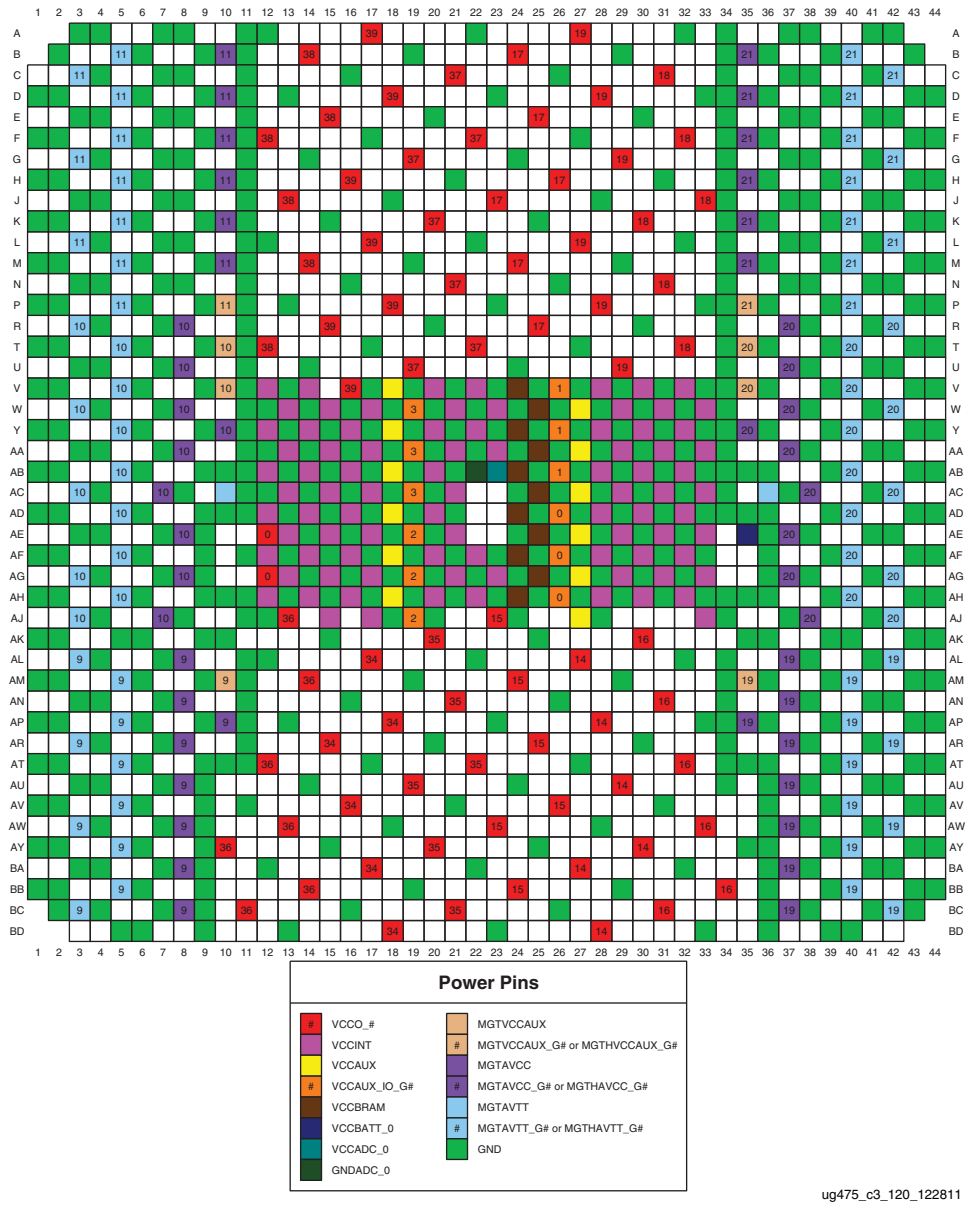


Figure 3-164: **FF1927, FFG1927, and FFV1927 Packages—XC7VX415T Power and GND Placement**

FF1157, FFG1157, and FFV1157 Packages—XC7VX485T

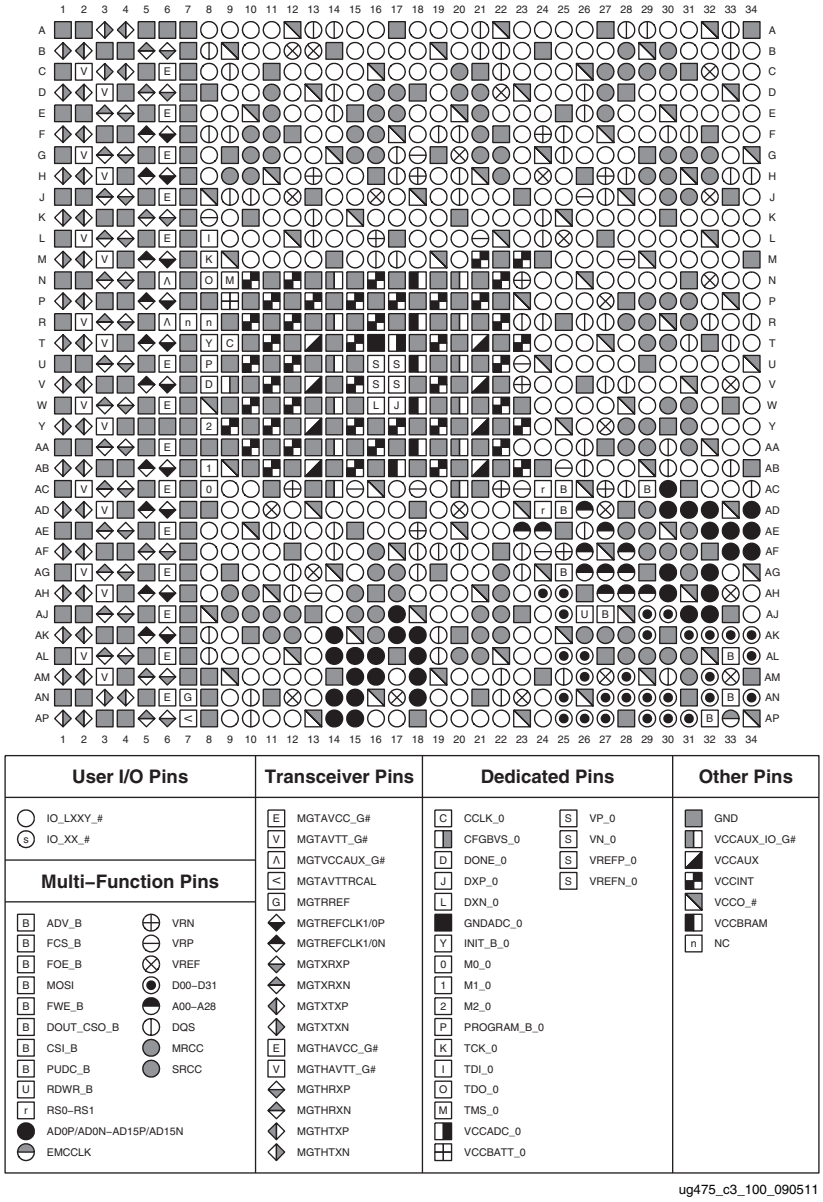


Figure 3-165: **FF1157, FFG1157, and FFV1157 Packages—XC7VX485T Pinout Diagram**

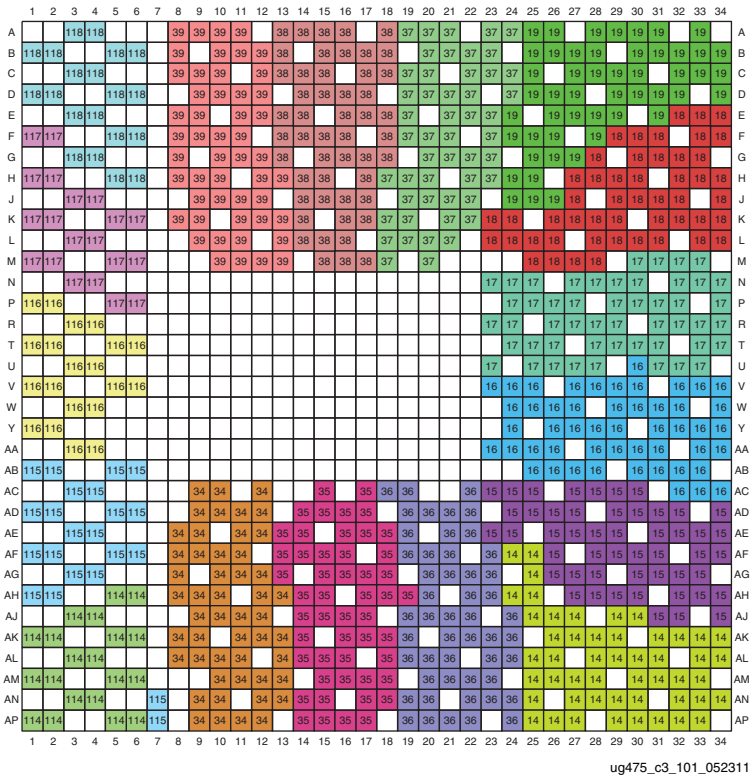


Figure 3-166: **FF1157, FFG1157, and FFV1157 Packages—XC7VX485T I/O Banks**

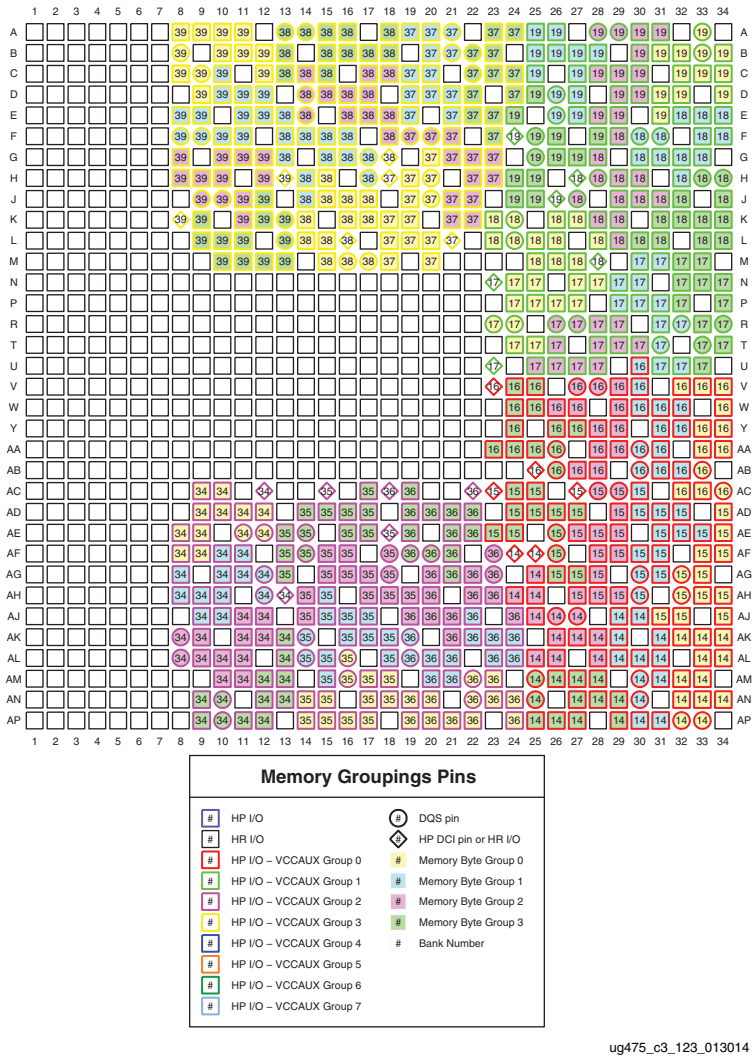


Figure 3-167: **FF1157, FFG1157, and FFV1157 Packages—XC7VX485T Memory Groupings**

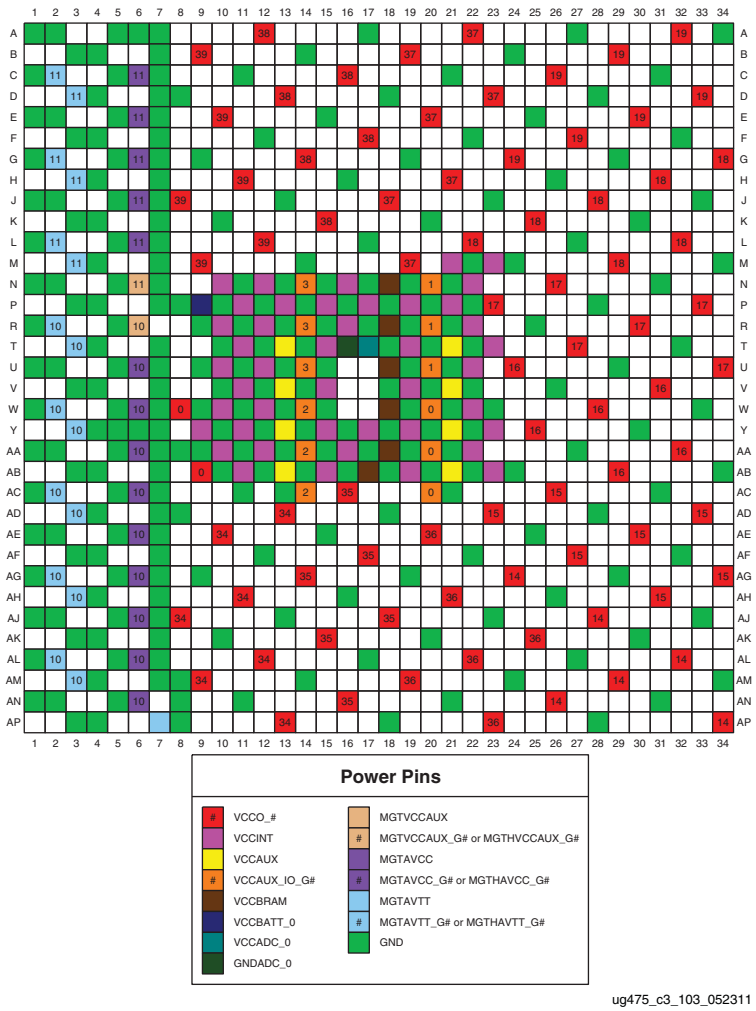


Figure 3-168: **FF1157, FFG1157, and FFV1157 Packages—XC7VX485T Power and GND Placement**

FF1158, FFG1158, and FFV1158 Packages—XC7VX485T

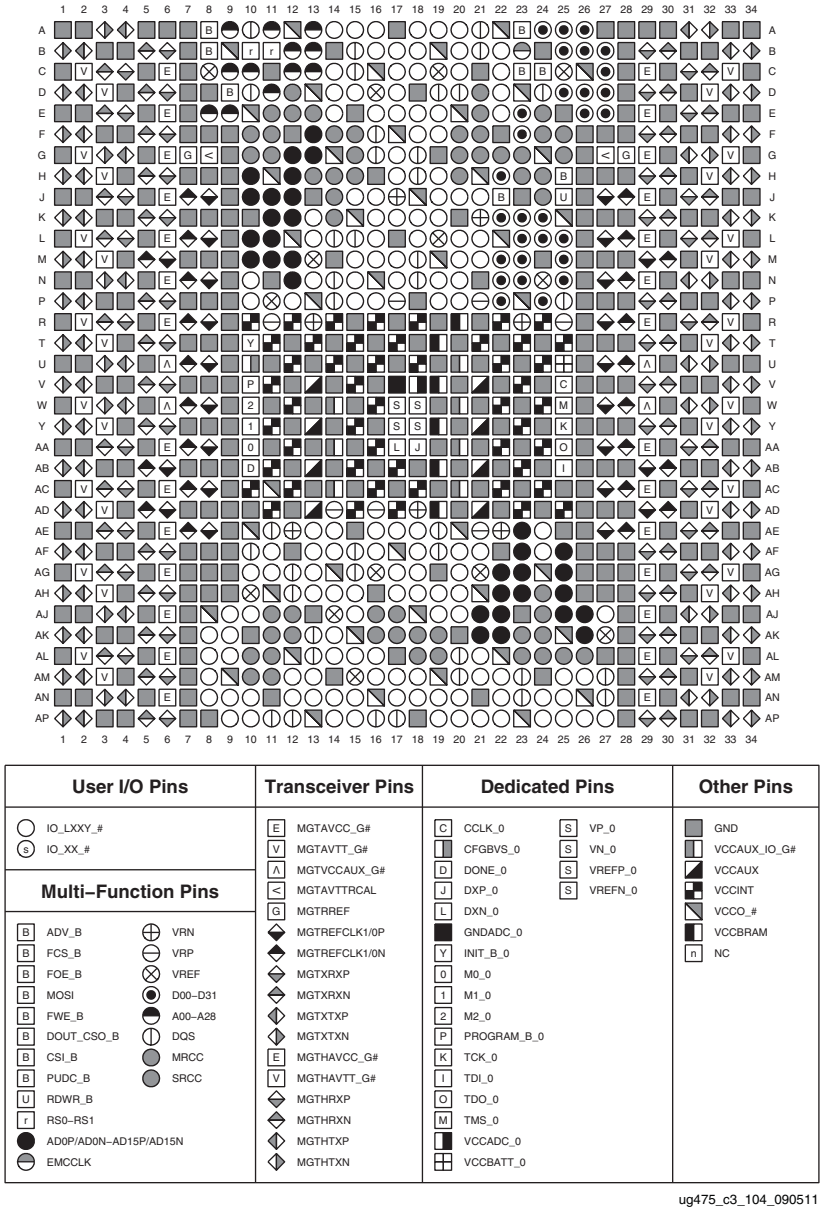


Figure 3-169: **FF1158, FFG1158, and FFV1158 Packages—XC7VX485T Pinout Diagram**

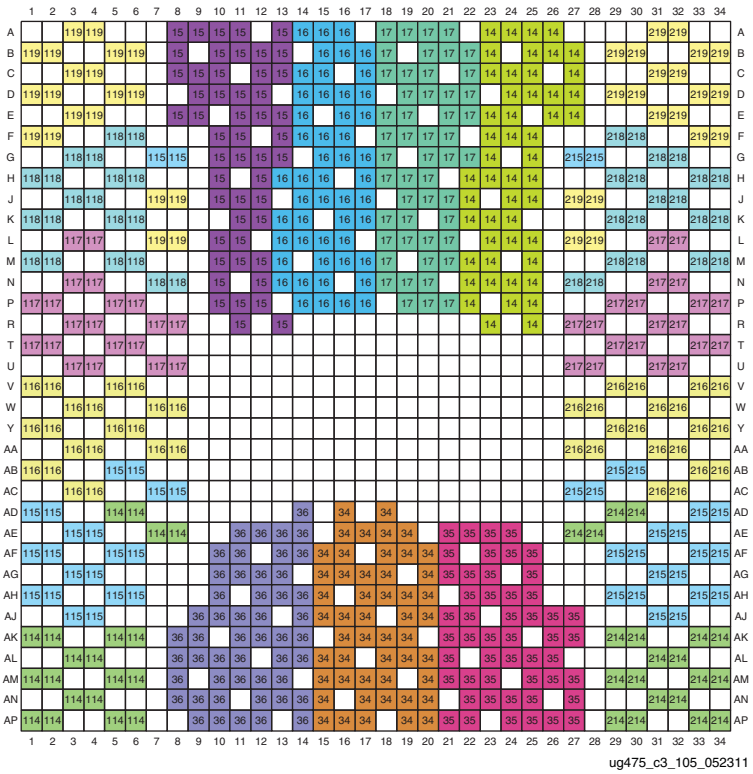


Figure 3-170: **FF1158, FFG1158, and FFV1158 Packages—XC7VX485T I/O Banks**

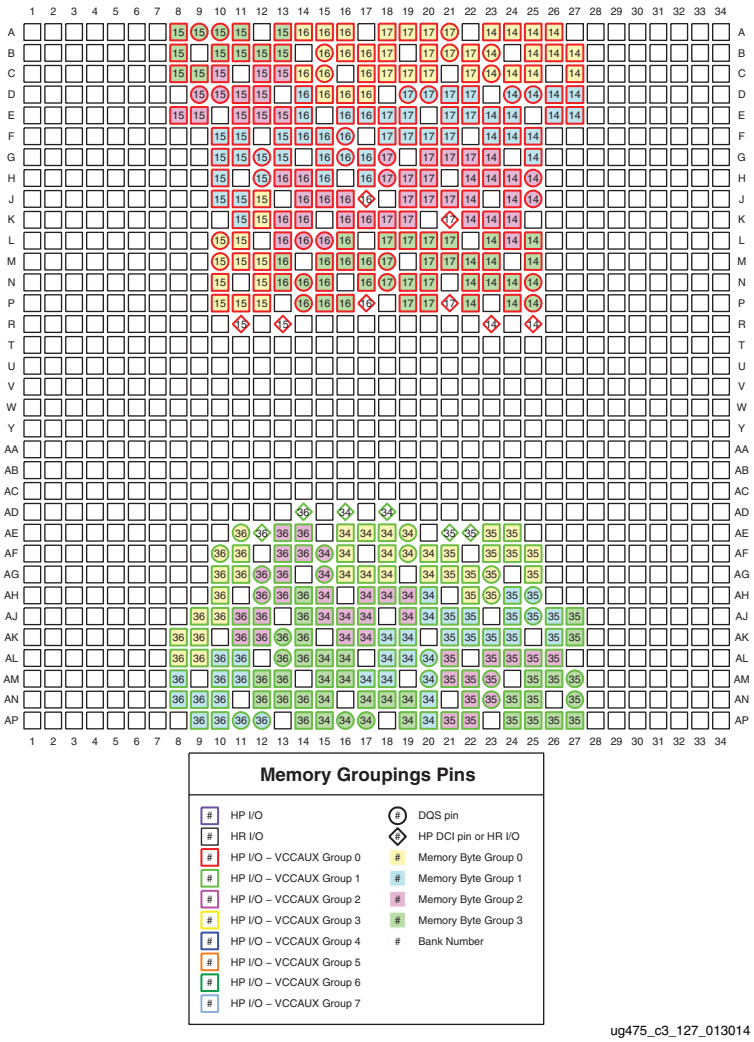


Figure 3-171: **FF1158, FFG1158, and FFV1158 Packages—XC7VX485T Memory Groupings**

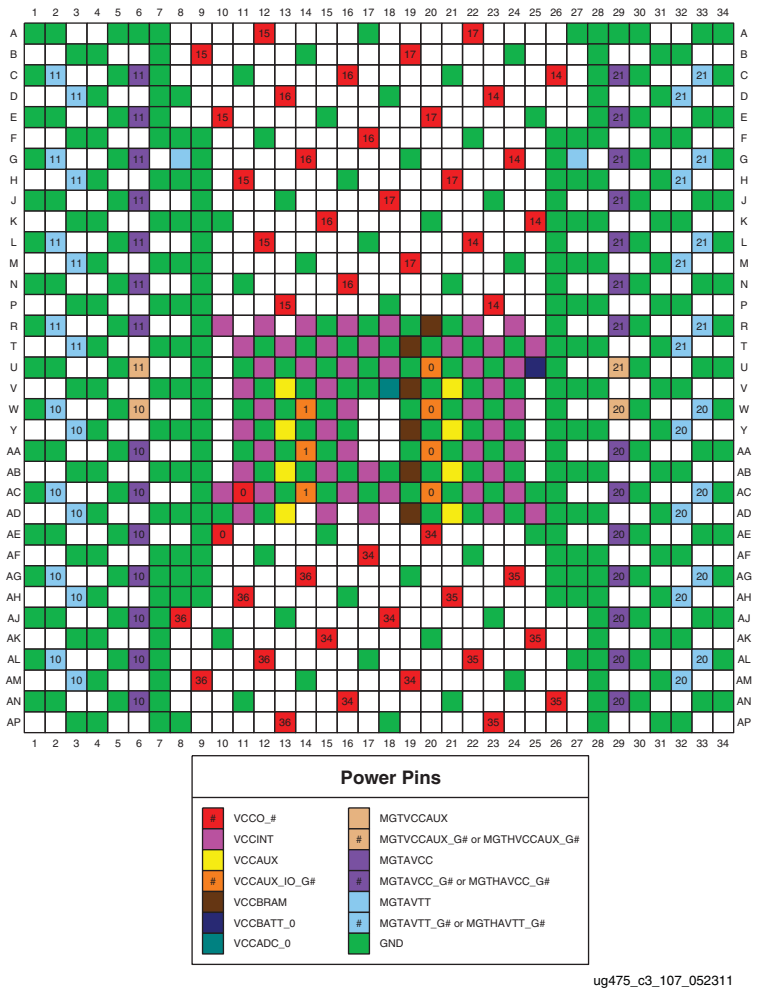


Figure 3-172: **FF1158, FFG1158, and FFV1158 Packages—XC7VX485T Power and GND Placement**

FF1761, FFG1761, and RF1761 Packages—XC7VX485T

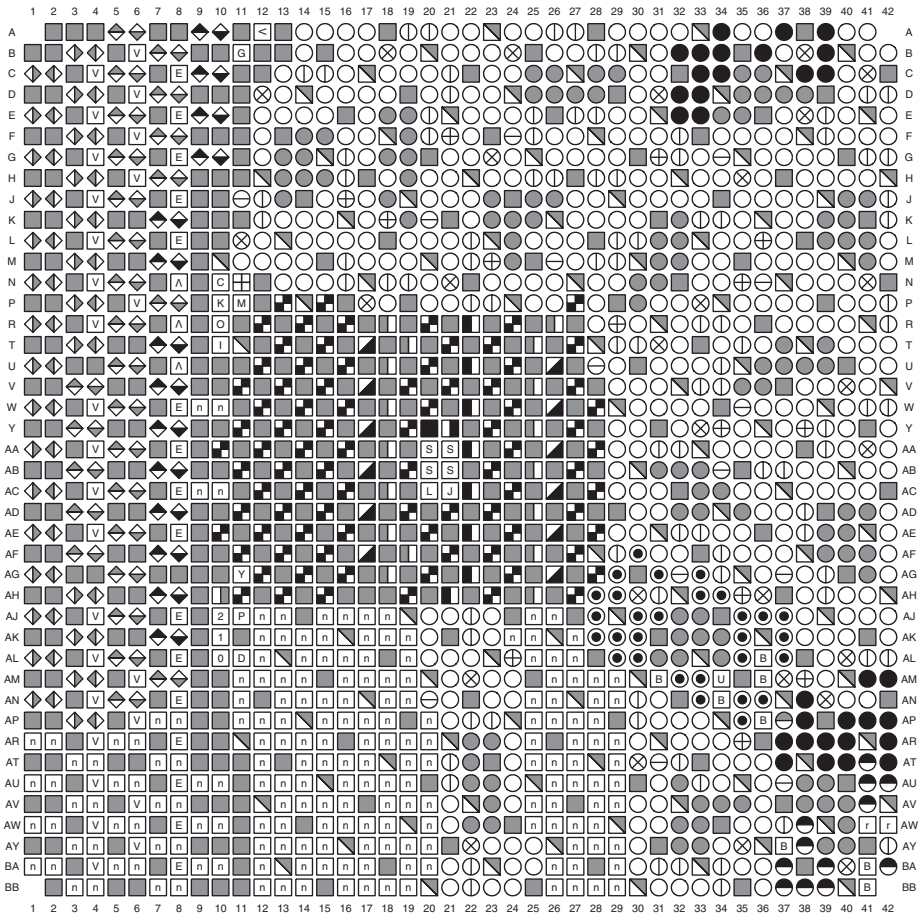


Figure 3-173: **FF1761, FFG1761, and RF1761 Packages—XC7VX485T Pinout Diagram**

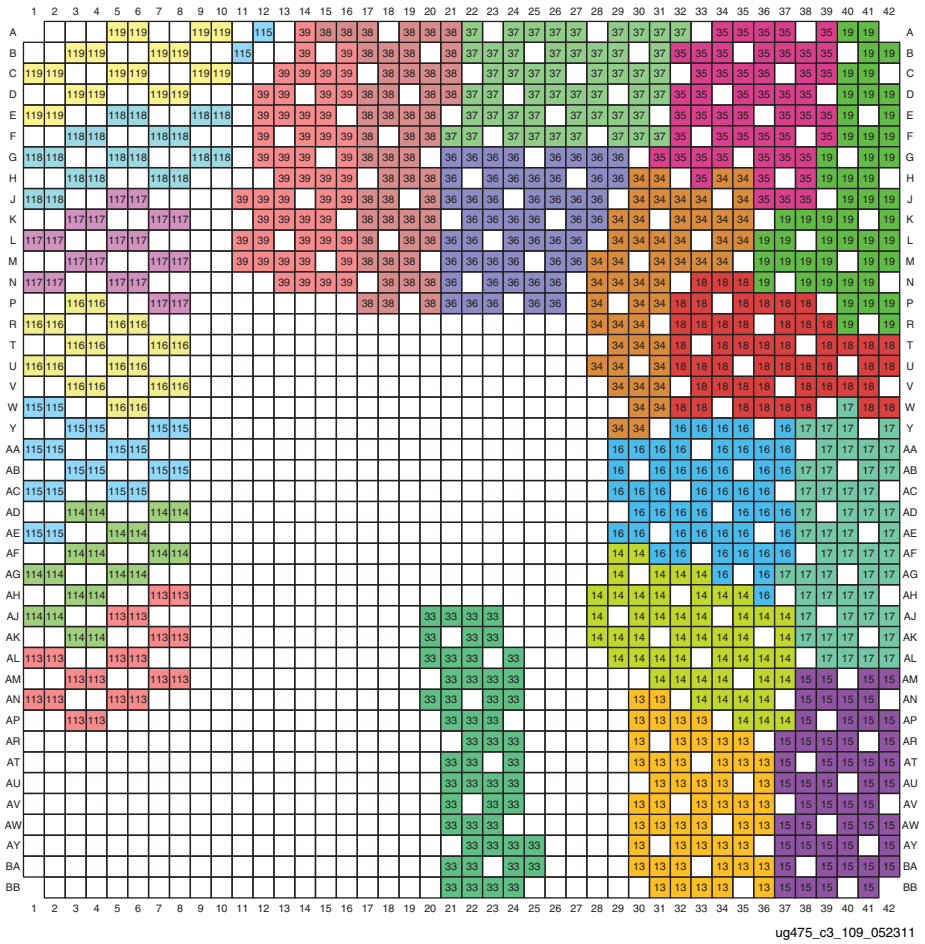


Figure 3-174: **FF1761, FFG1761, and RF1761 Packages—XC7VX485T I/O Banks**

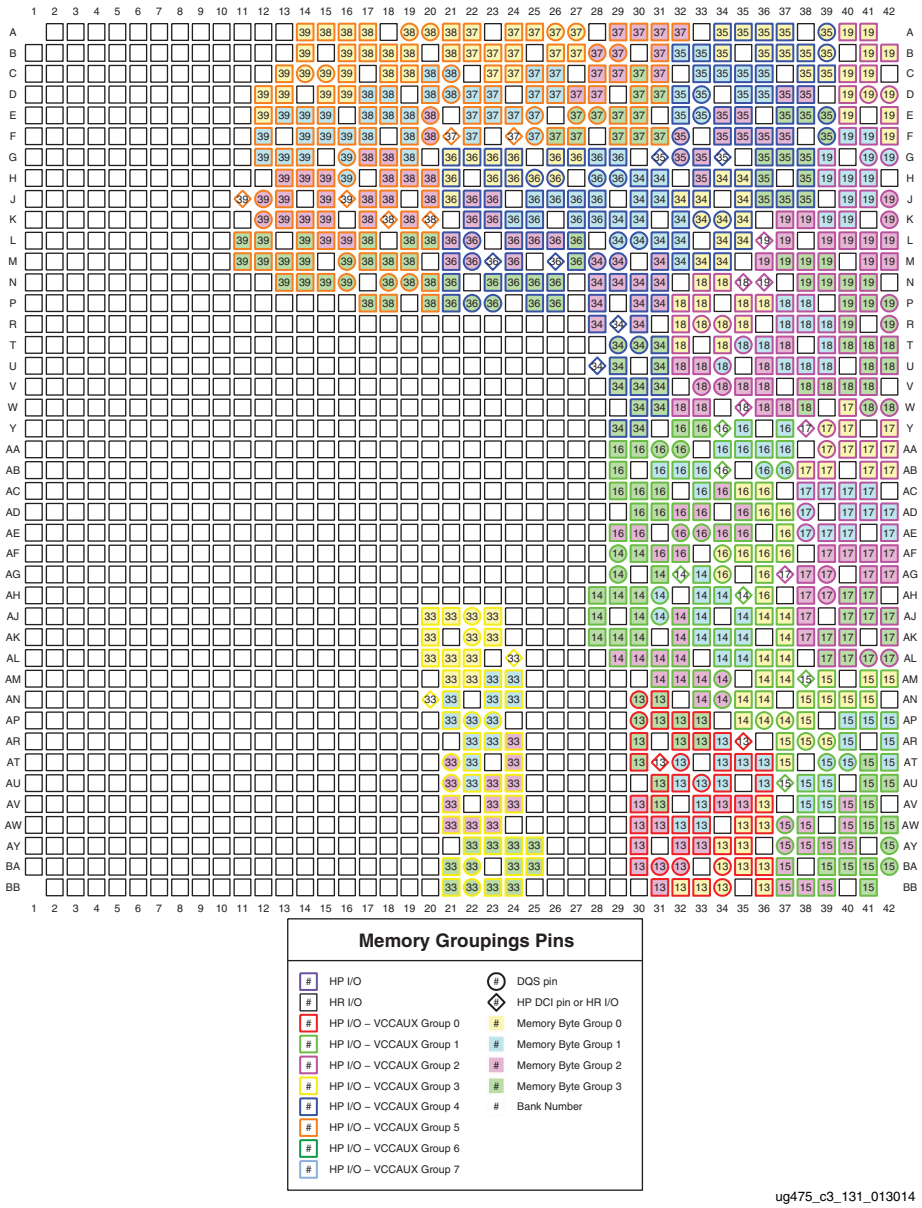


Figure 3-175: **FF1761, FFG1761, and RF1761 Packages—XC7VX485T Memory Groupings**

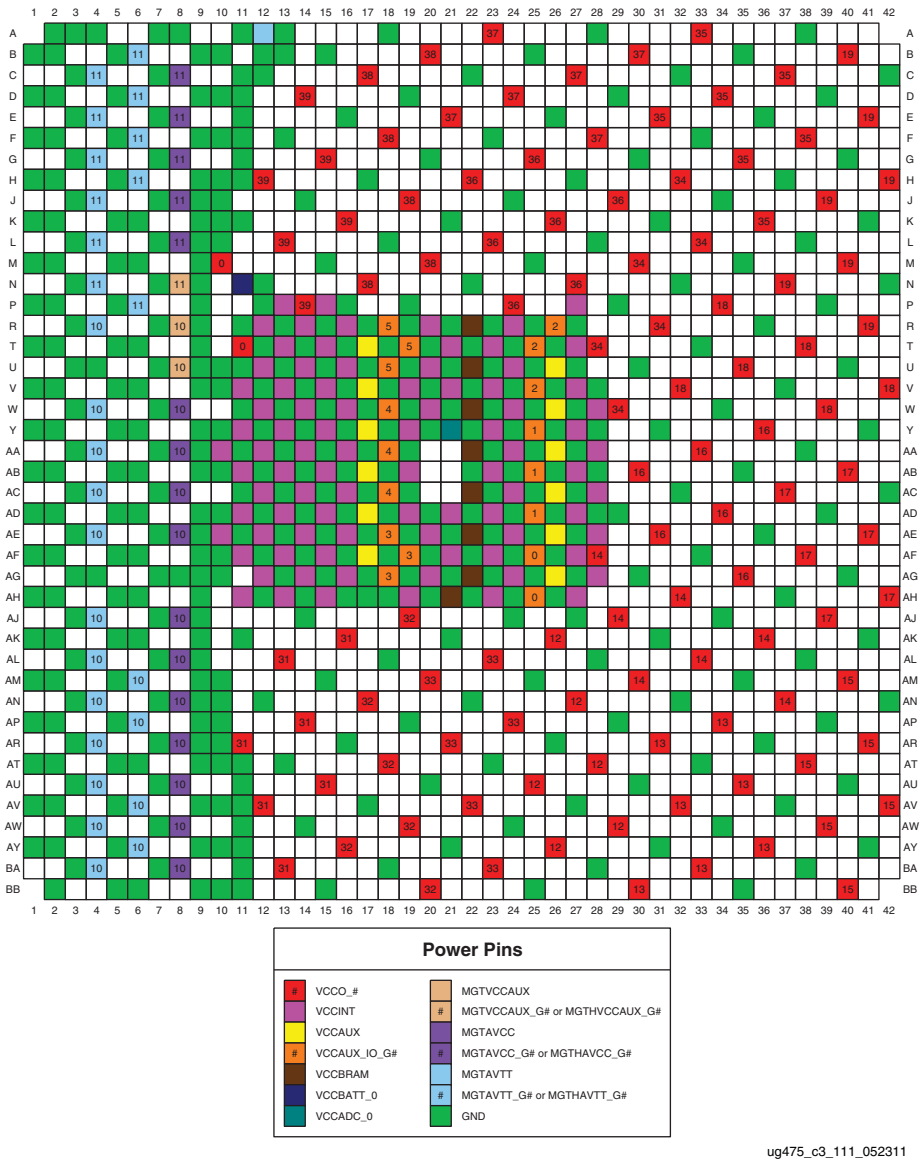


Figure 3-176: **FF1761, FFG1761, and RF1761 Packages—XC7VX485T Power and GND Placement**

FF1927 and FFG1927 Packages—XC7VX485T

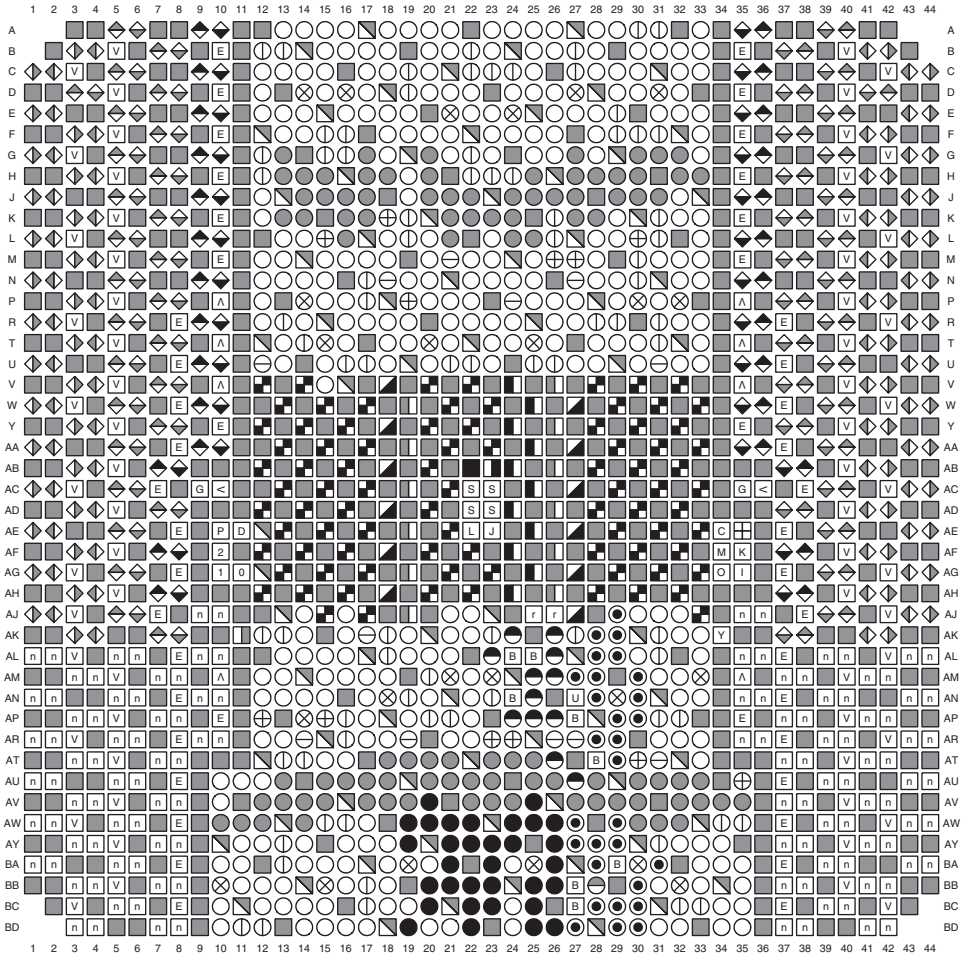


Figure 3-177: **FF1927 and FFG1927 Packages—XC7VX485T Pinout Diagram**

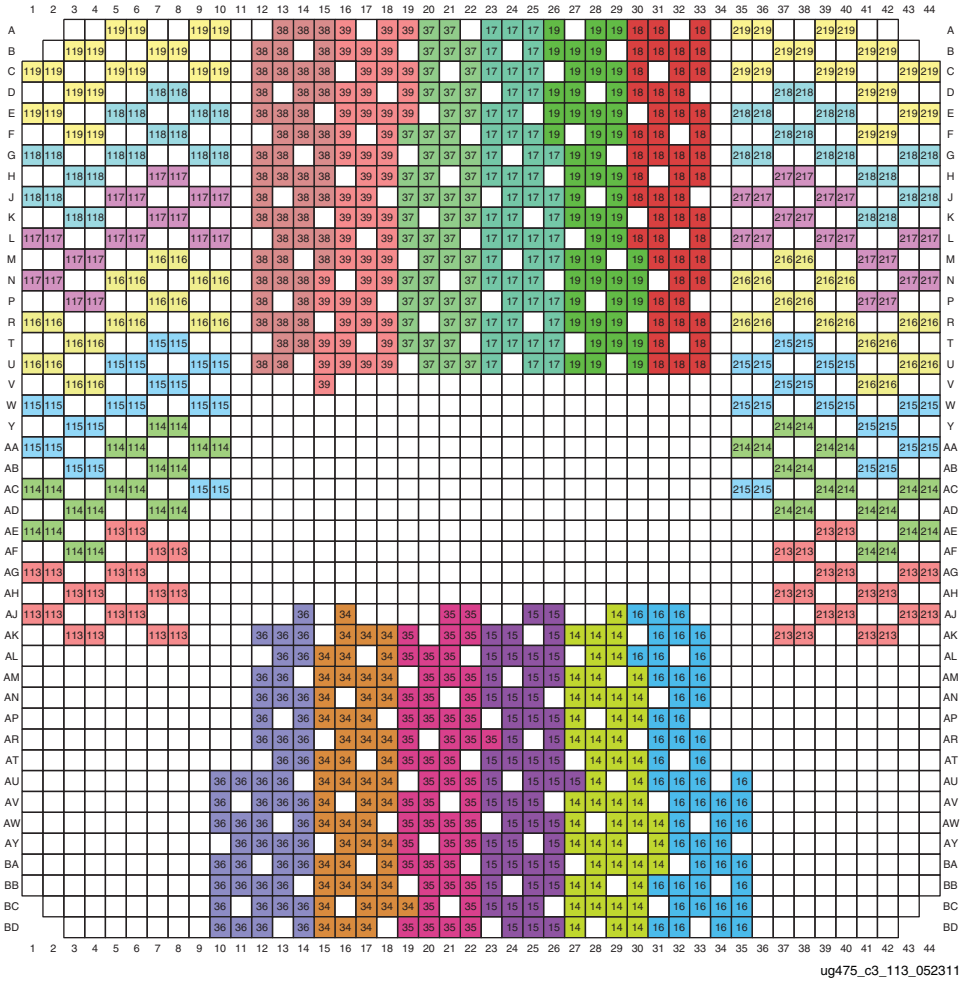


Figure 3-178: **FF1927 and FFG1927 Packages—XC7VX485T I/O Banks**

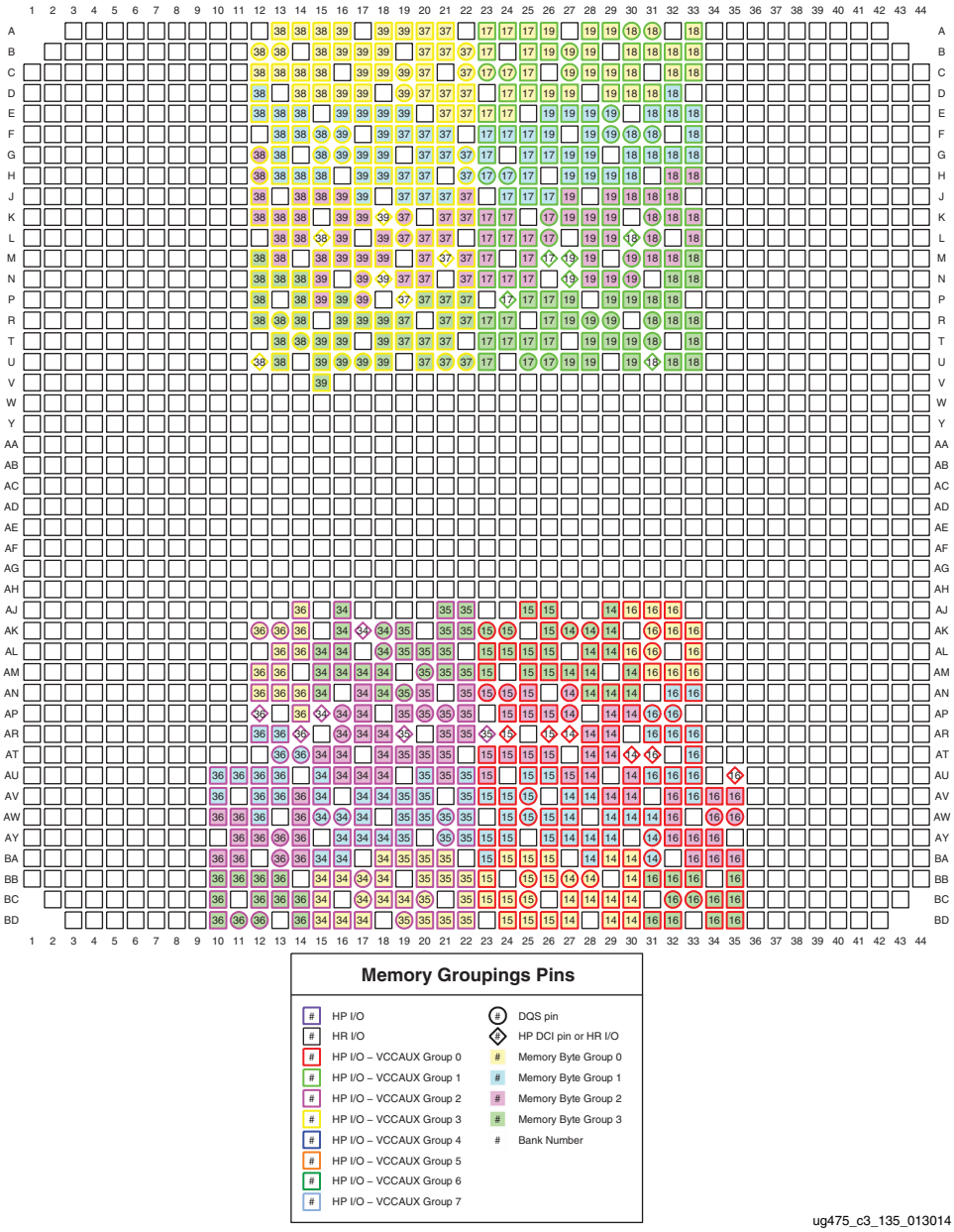


Figure 3-179: **FF1927 and FFG1927 Packages—XC7VX485T Memory Groupings**

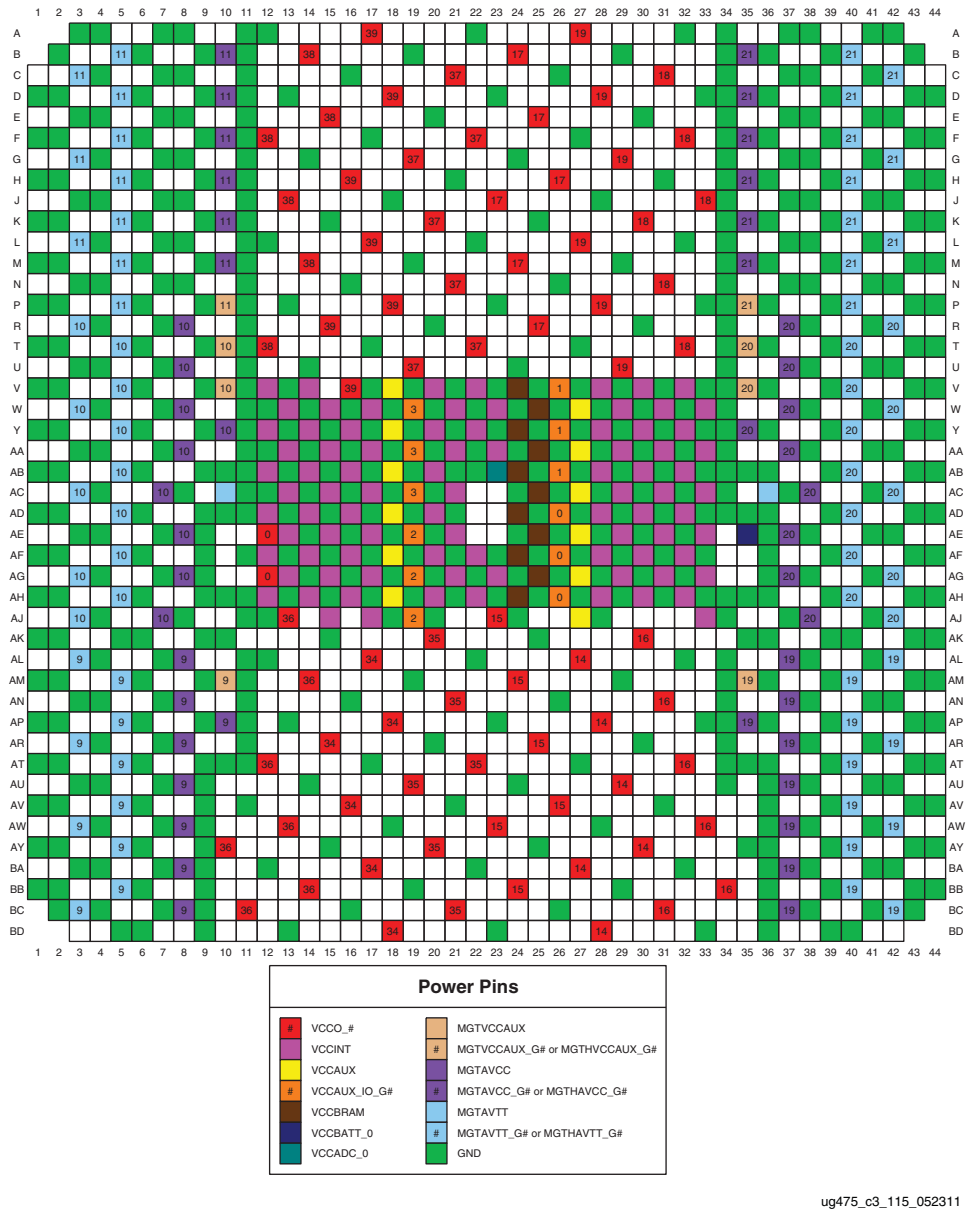


Figure 3-180: **FF1927 and FFG1927 Packages—XC7VX485T Power and GND Placement**

FF1930, FFG1930, and RF1930 Packages—XC7VX485T

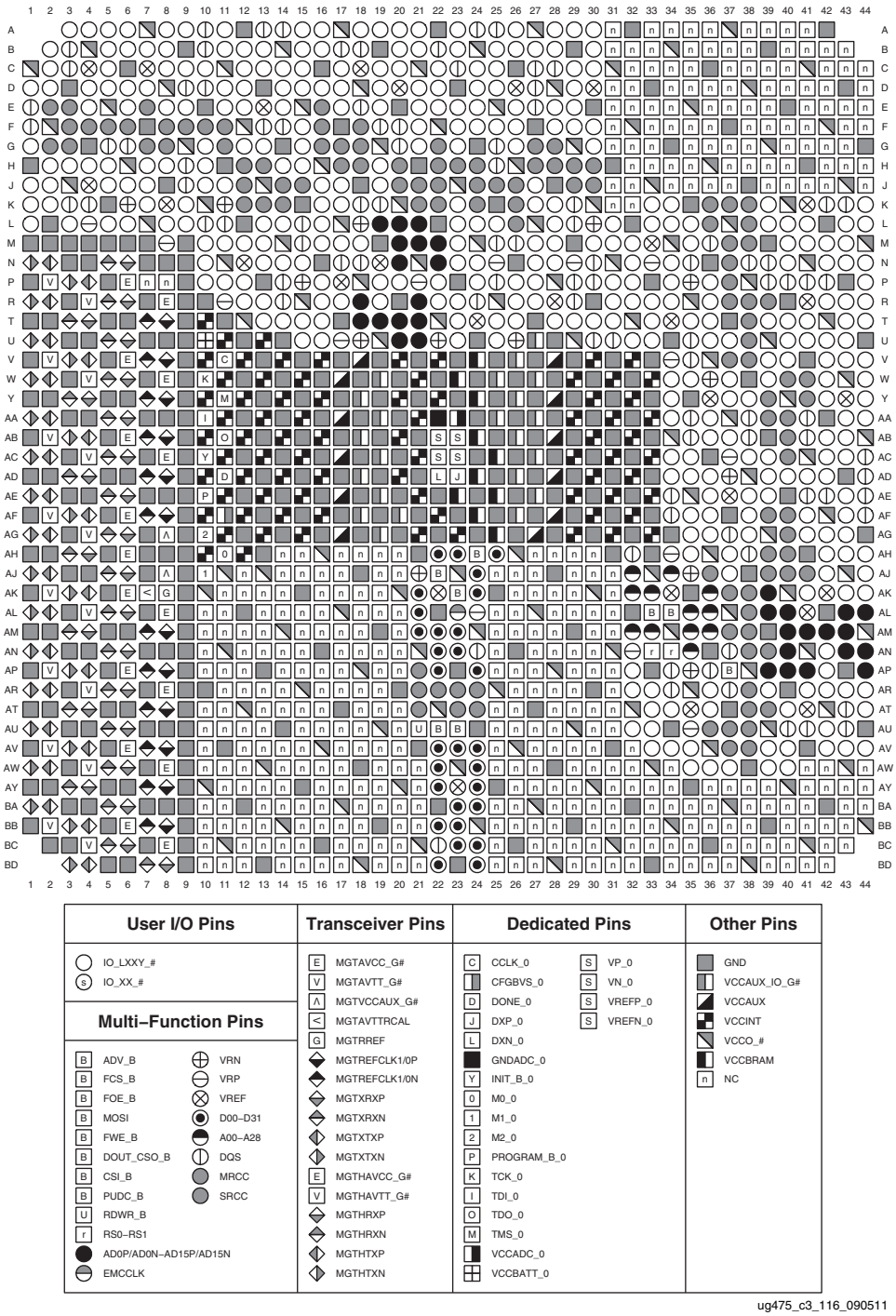


Figure 3-181: **FF1930, FFG1930, and RF1930 Packages—XC7VX485T Pinout Diagram**

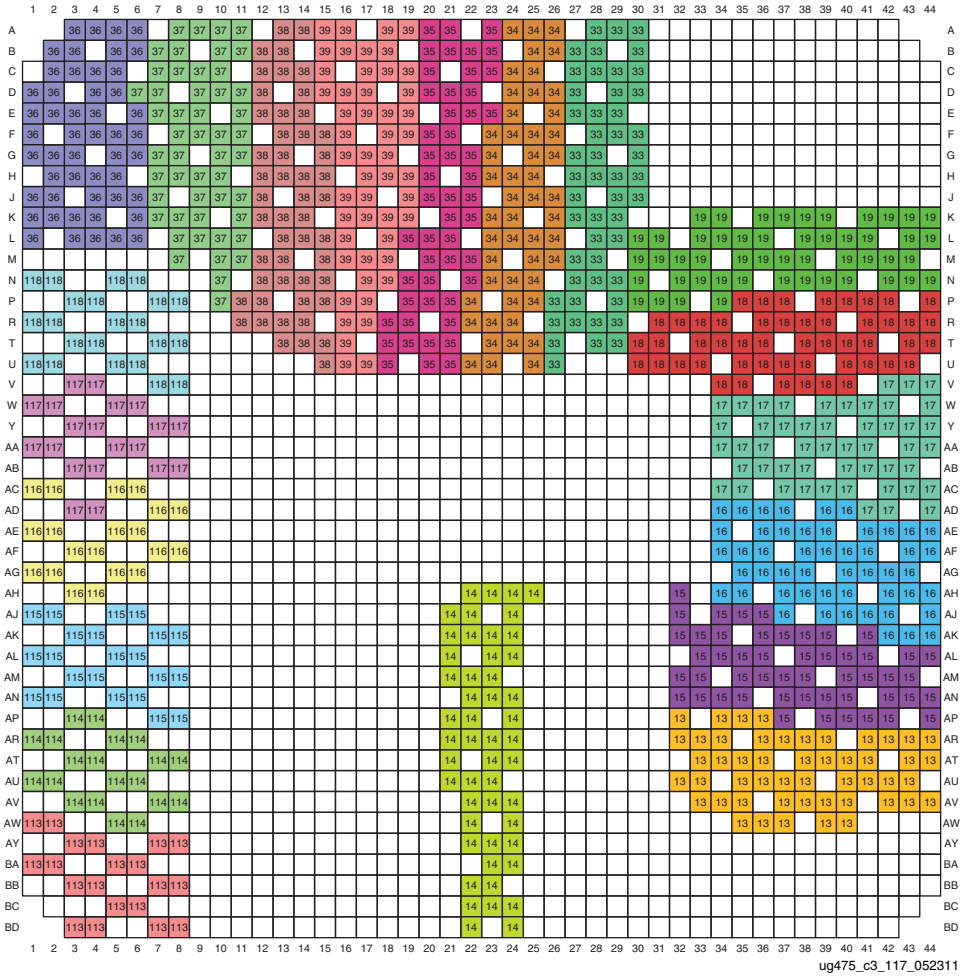


Figure 3-182: **FF1930, FFG1930, and RF1930 Packages—XC7VX485T I/O Banks**

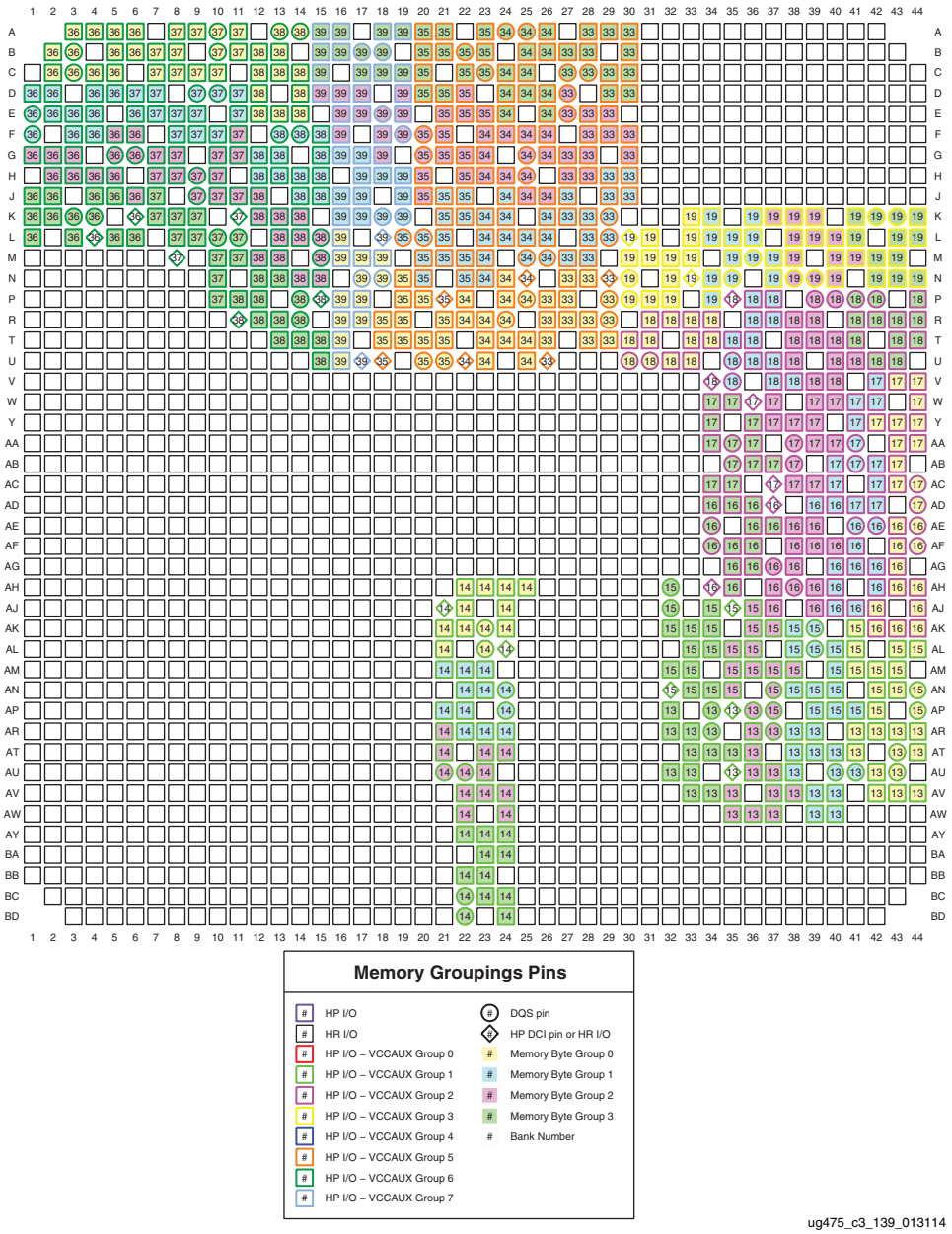


Figure 3-183: **FF1930, FFG1930, and RF1930 Packages—XC7VX485T Memory Groupings**

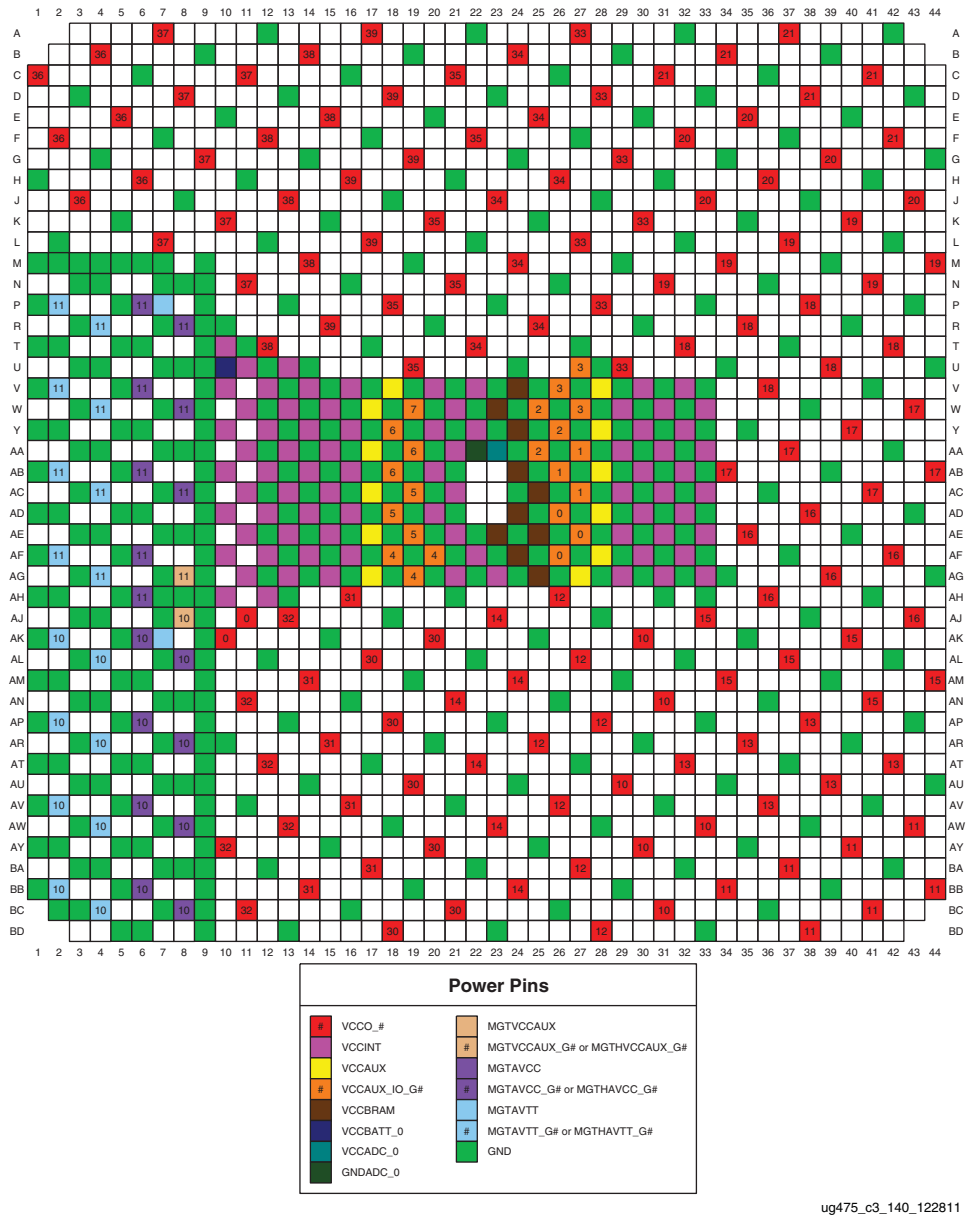


Figure 3-184: **FF1930, FFG1930, and RF1930 Packages—XC7VX485T Power and GND Placement**

FF1761, FFG1761, and RF1761 Packages—XC7VX690T

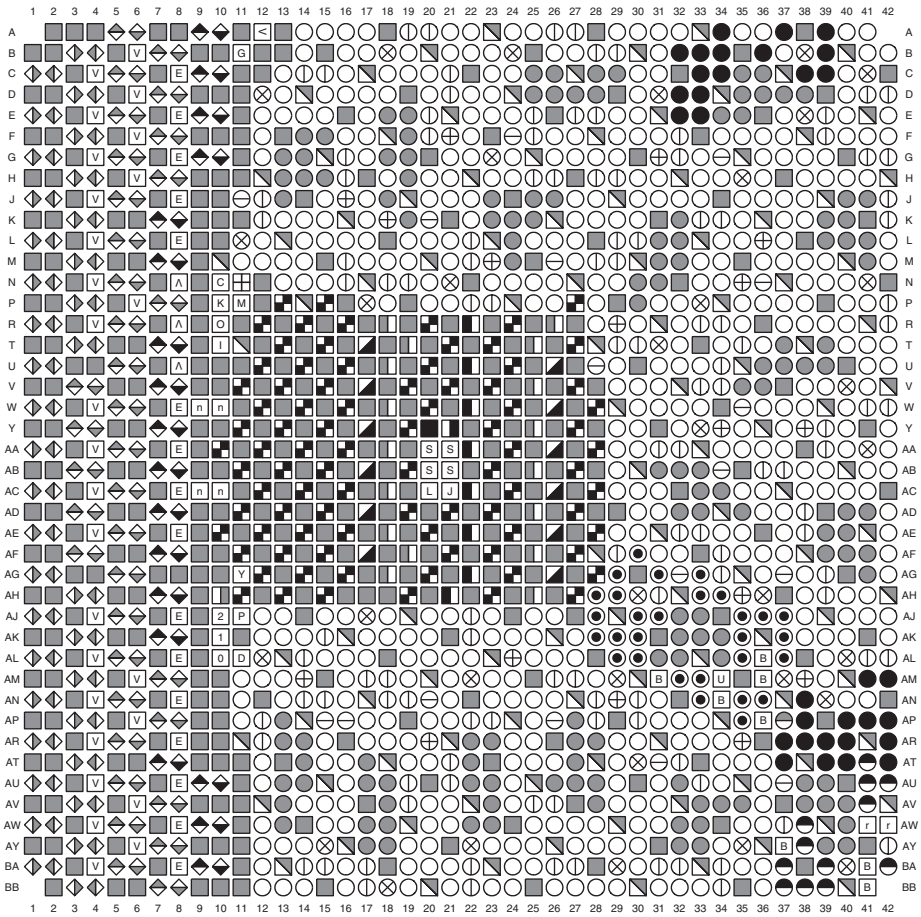


Figure 3-185: **FF1761, FFG1761, and RF1761 Packages—XC7VX690T Pinout Diagram**

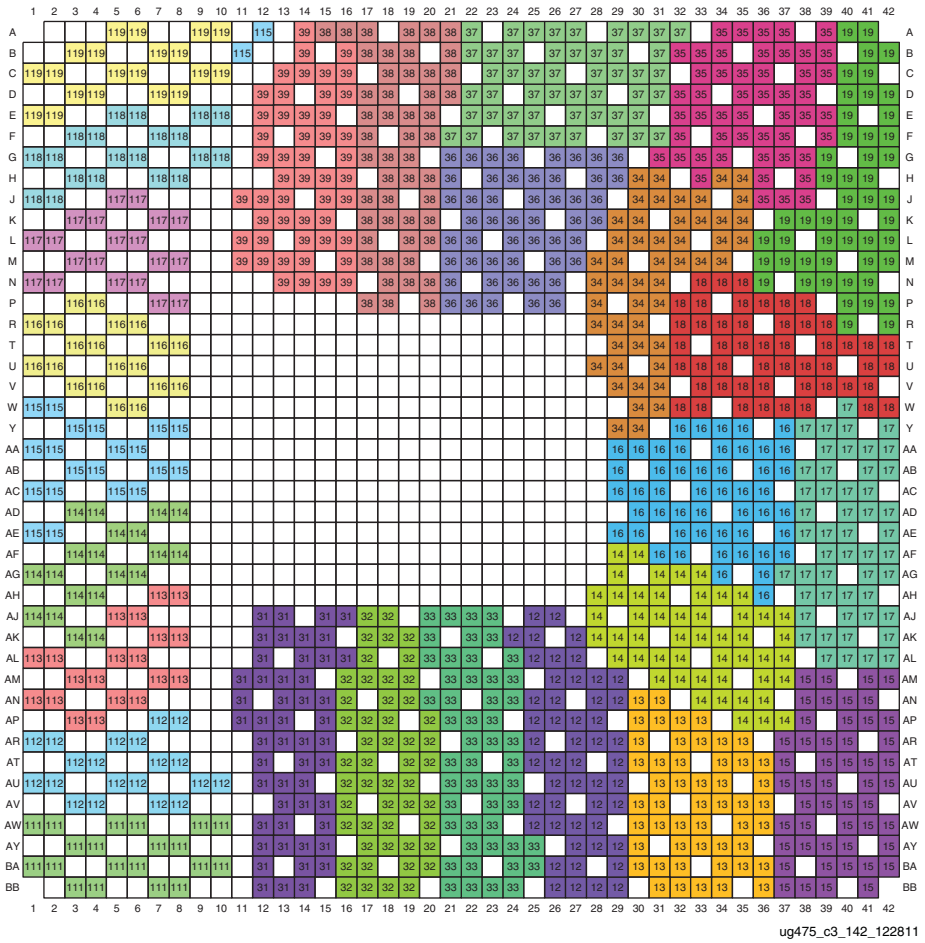


Figure 3-186: **FF1761, FFG1761, and RF1761 Packages—XC7VX690T I/O Banks**

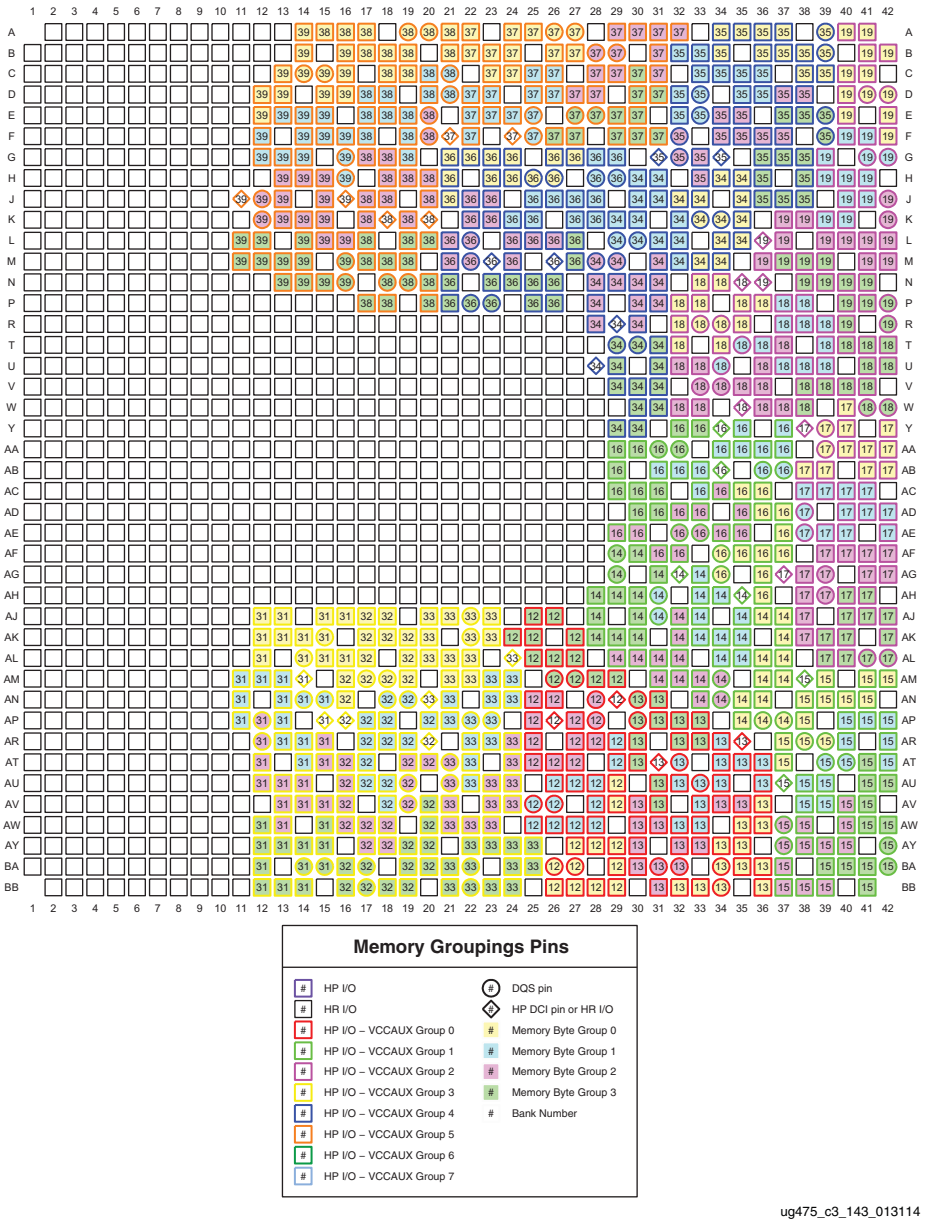


Figure 3-187: **FF1761, FFG1761, and RF1761 Packages—XC7VX690T Memory Groupings**

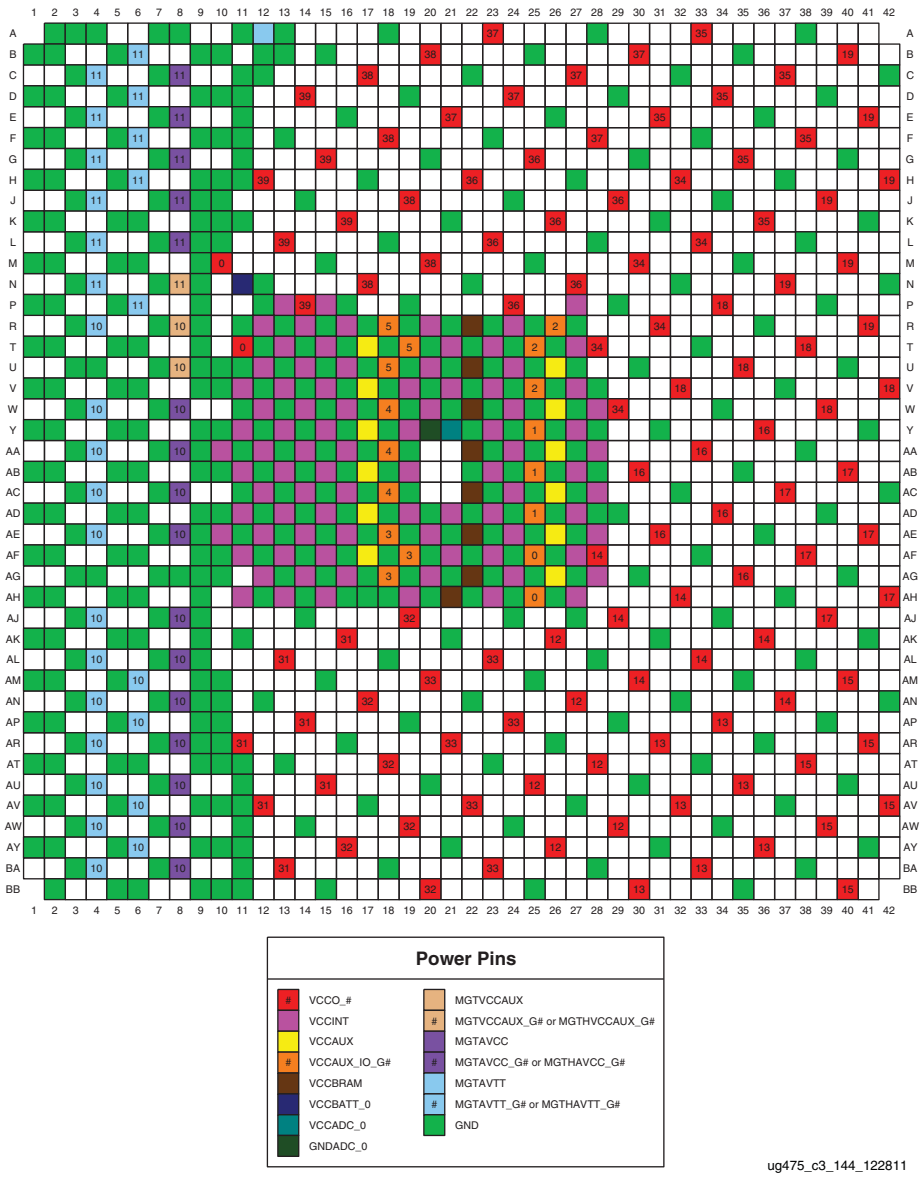


Figure 3-188: **FF1761, FFG1761, and RF1761 Packages—XC7VX690T Power and GND Placement**

FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T

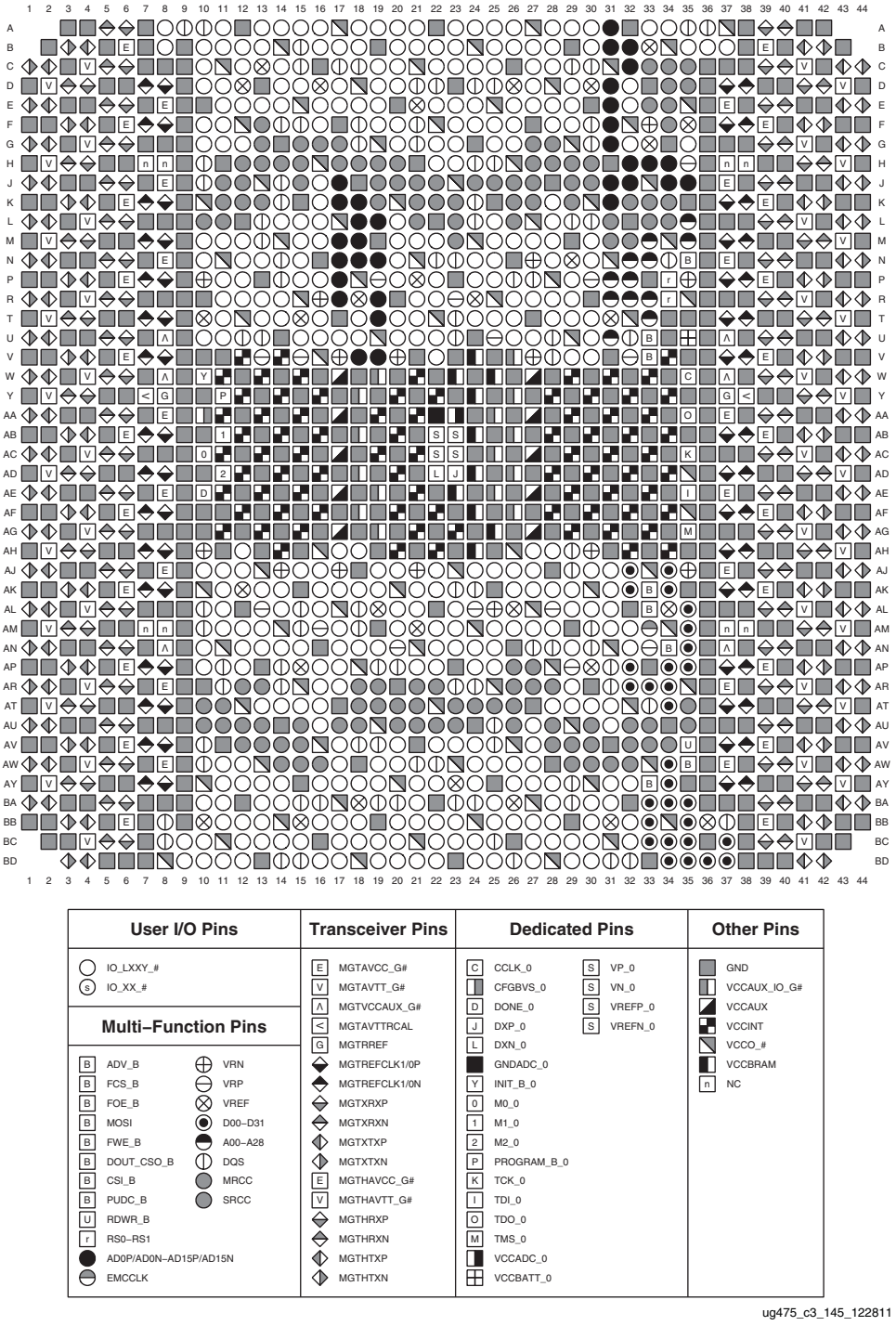


Figure 3-189: **FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T Pinout Diagram**

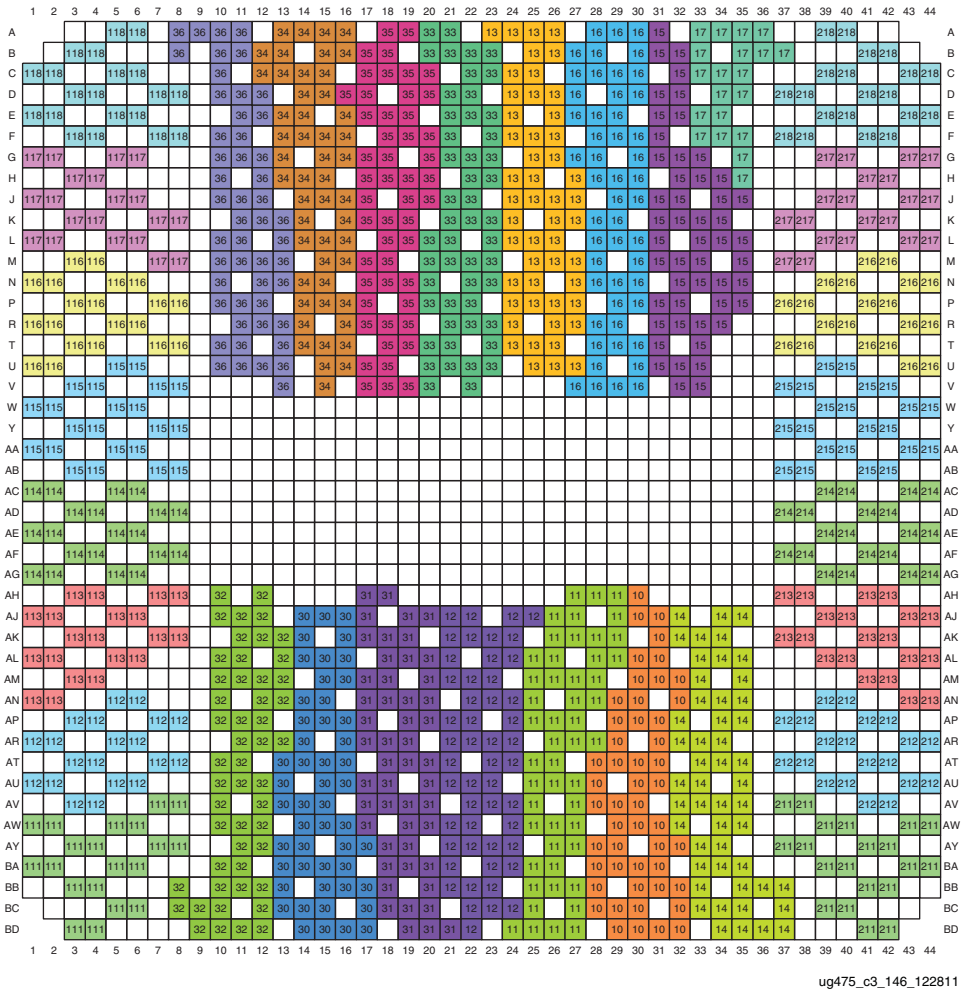


Figure 3-190: **FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T I/O Banks**

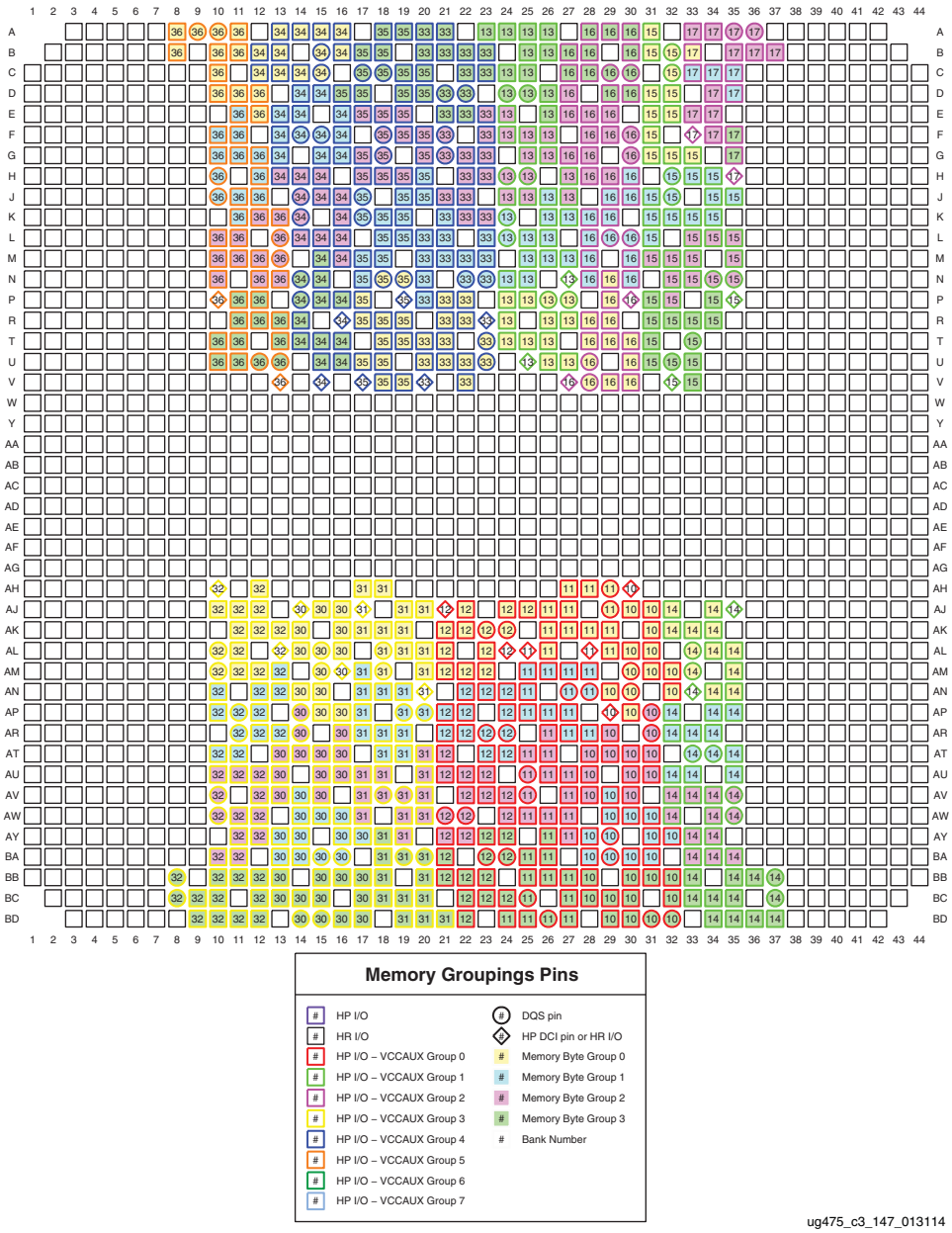


Figure 3-191: **FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T Memory Groupings**

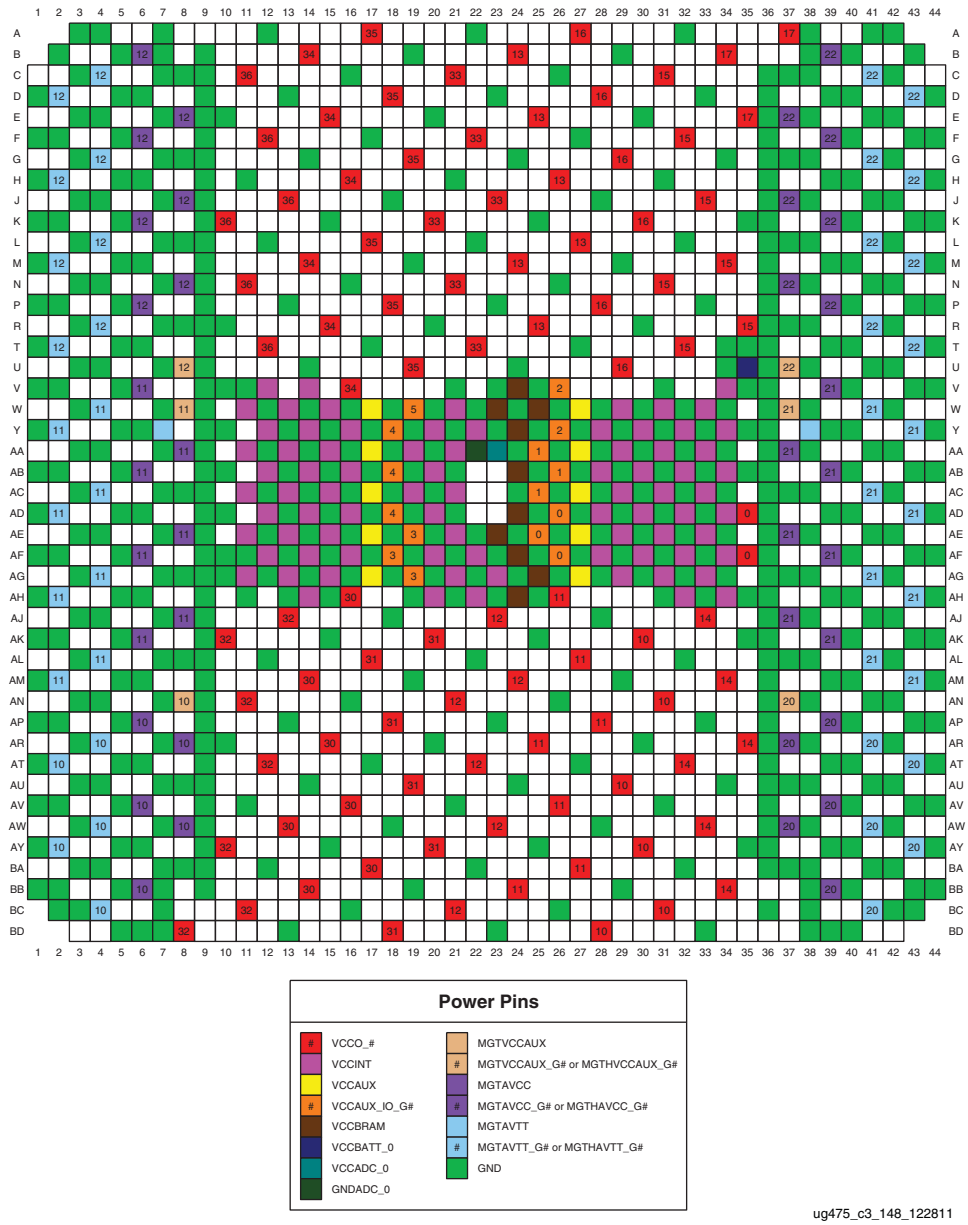


Figure 3-192: **FF1926 and FFG1926 Packages—XC7VX690T and XC7VX980T Power and GND Placement**

FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T

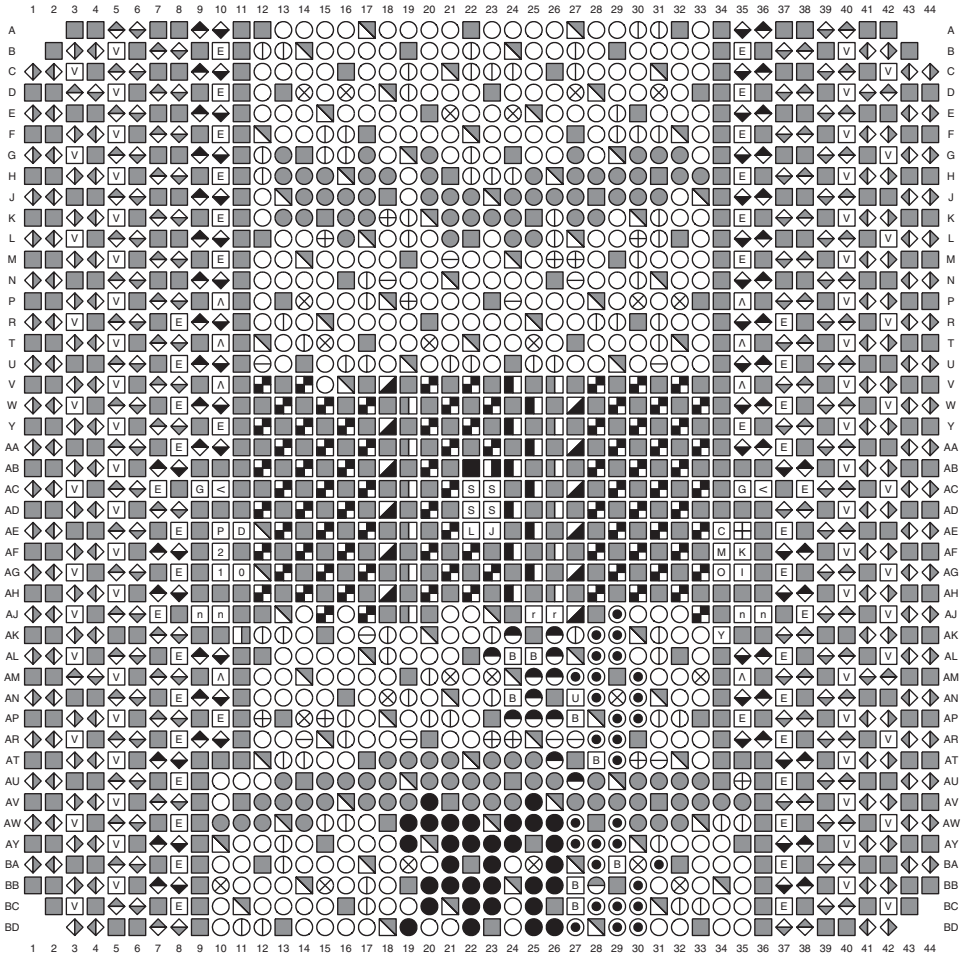


Figure 3-193: **FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T Pinout Diagram**

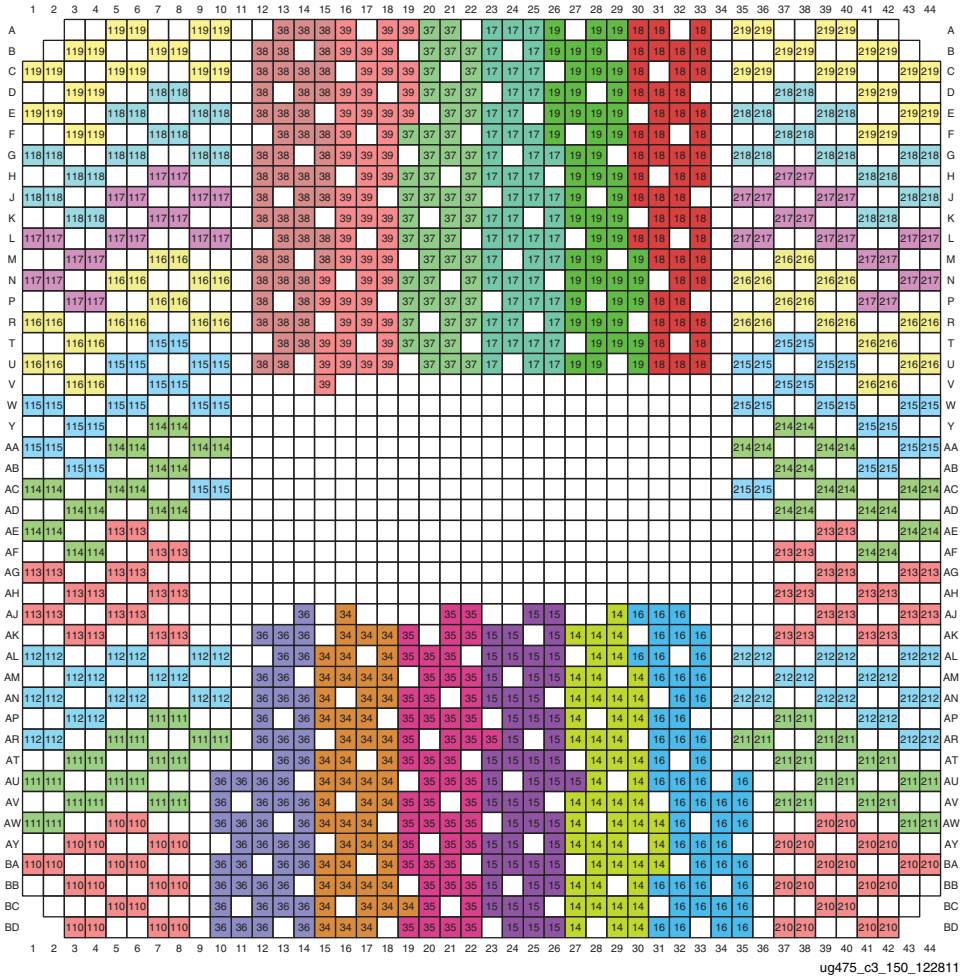


Figure 3-194: **FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T I/O Banks**

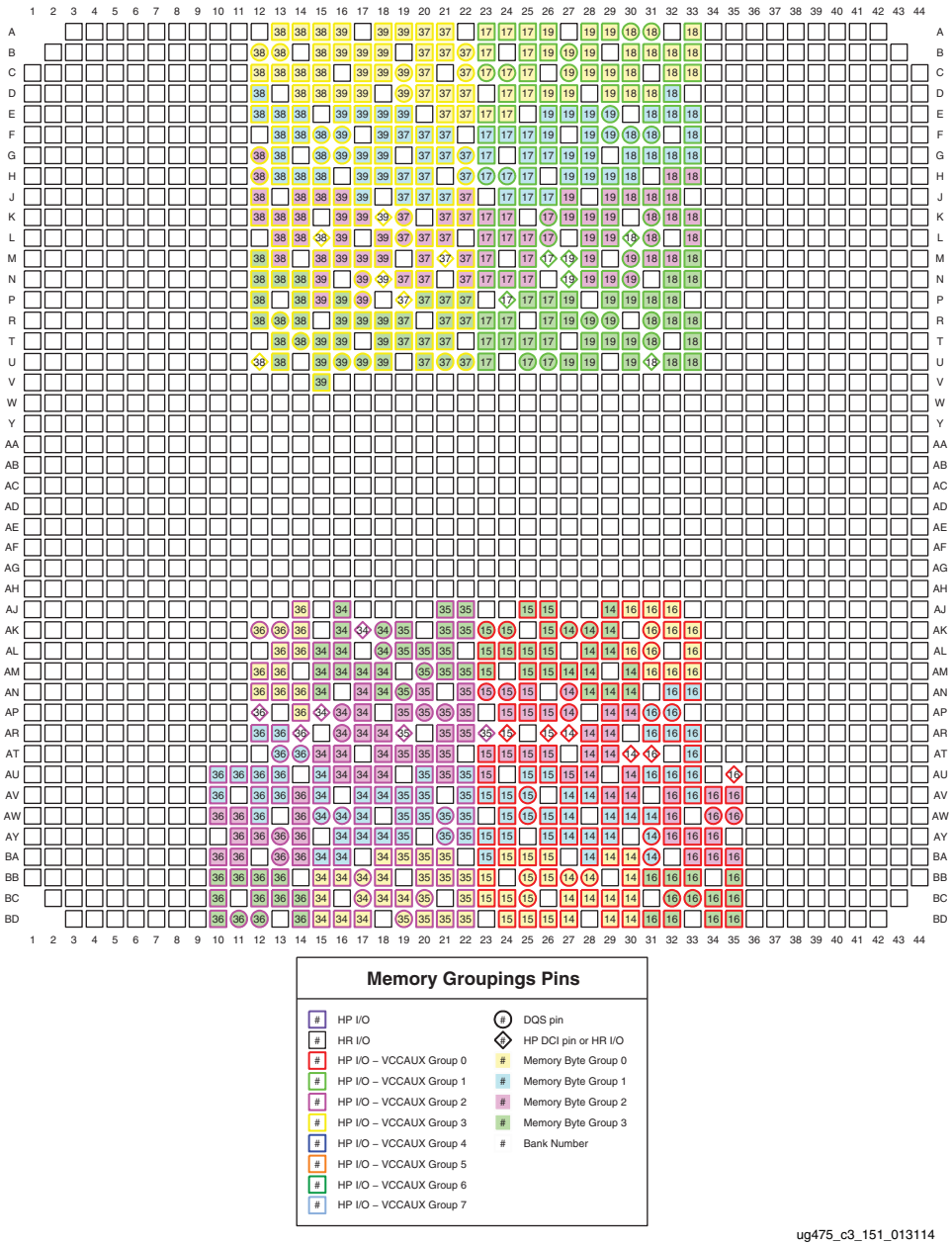


Figure 3-195: **FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T Memory Groupings**

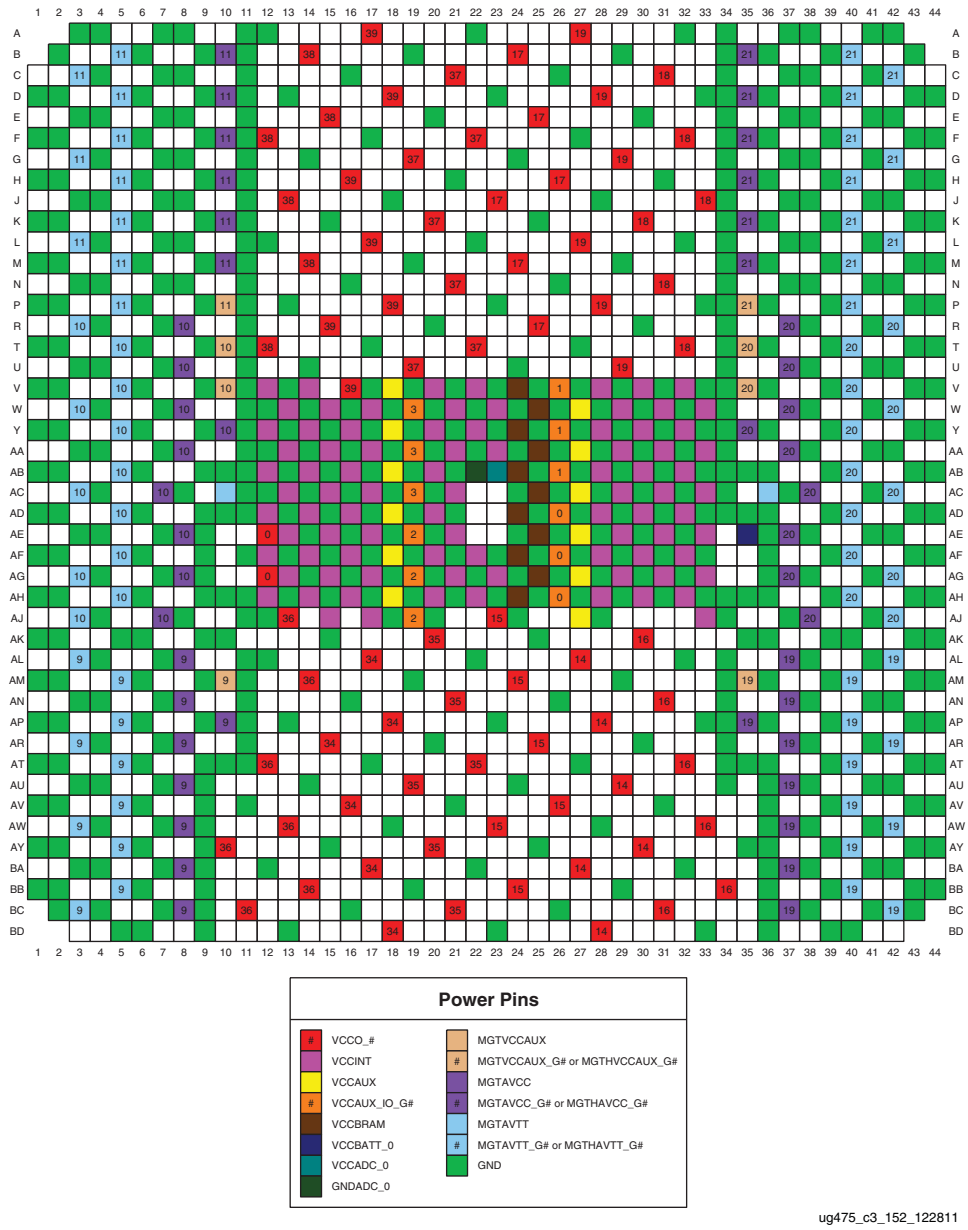


Figure 3-196: **FF1927 and FFG1927 Packages—XC7VX550T and XC7VX690T Power and GND Placement**

FF1930, FFG1930, and RF1930 Packages—XC7VX690T

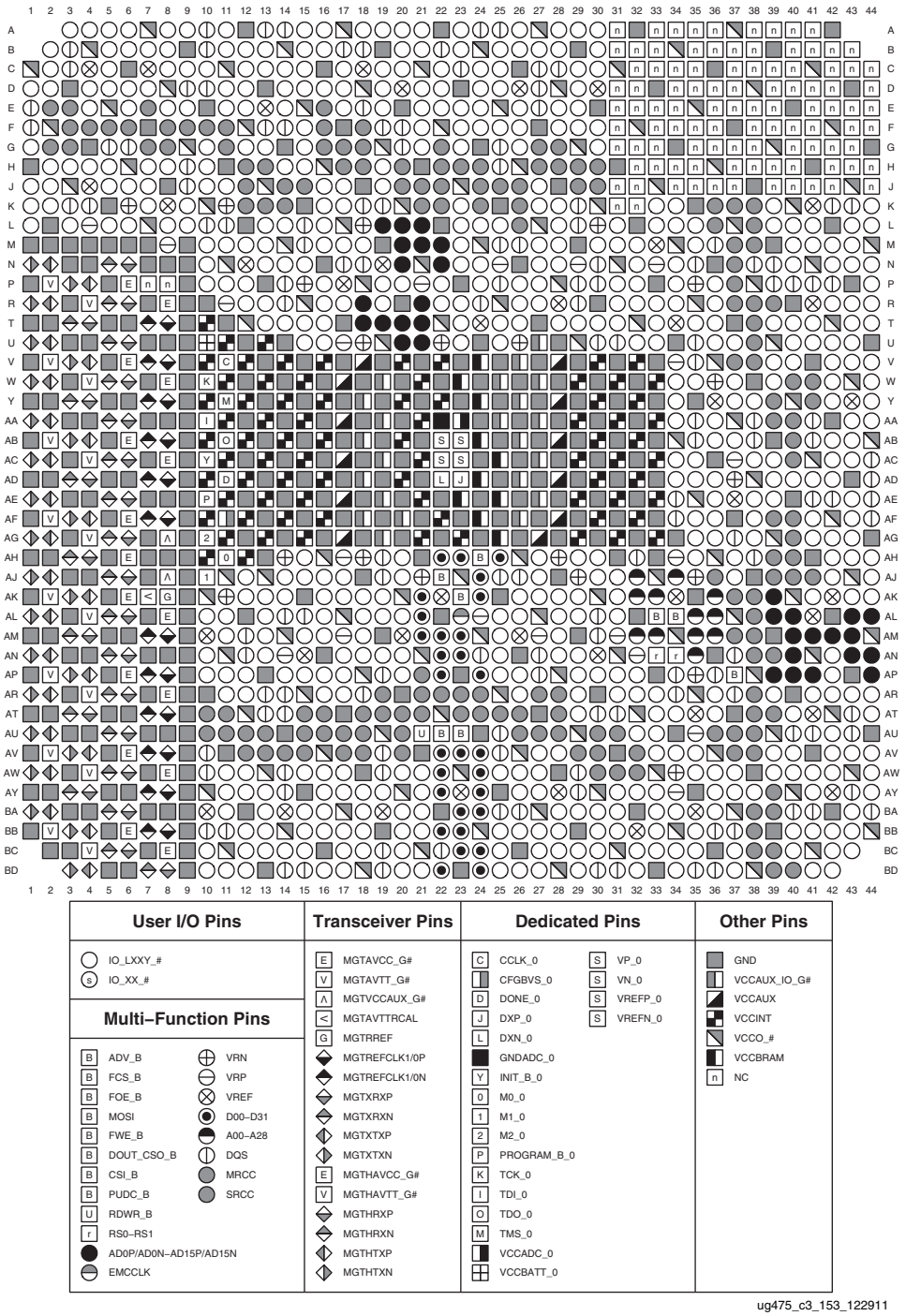


Figure 3-197: **FF1930, FFG1930, and RF1930 Packages—XC7VX690T Pinout Diagram**

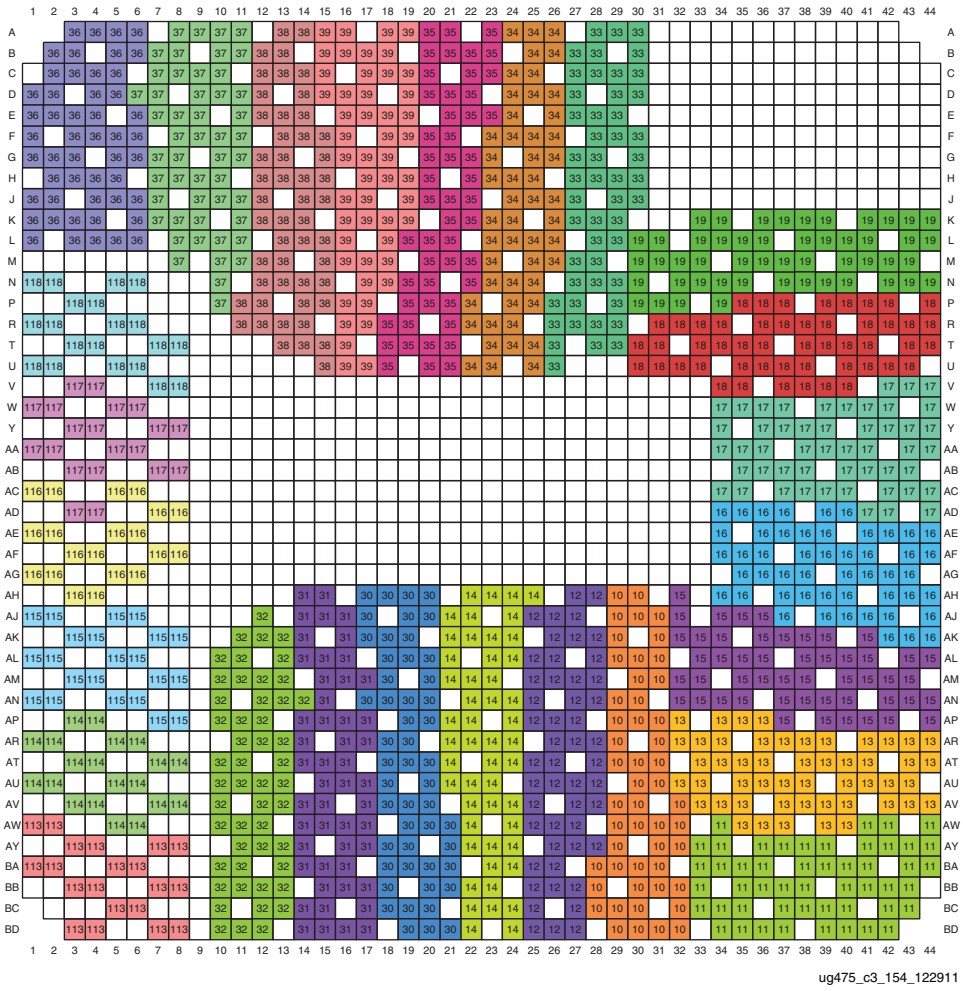


Figure 3-198: **FF1930, FFG1930, and RF1930 Packages—XC7VX690T I/O Banks**

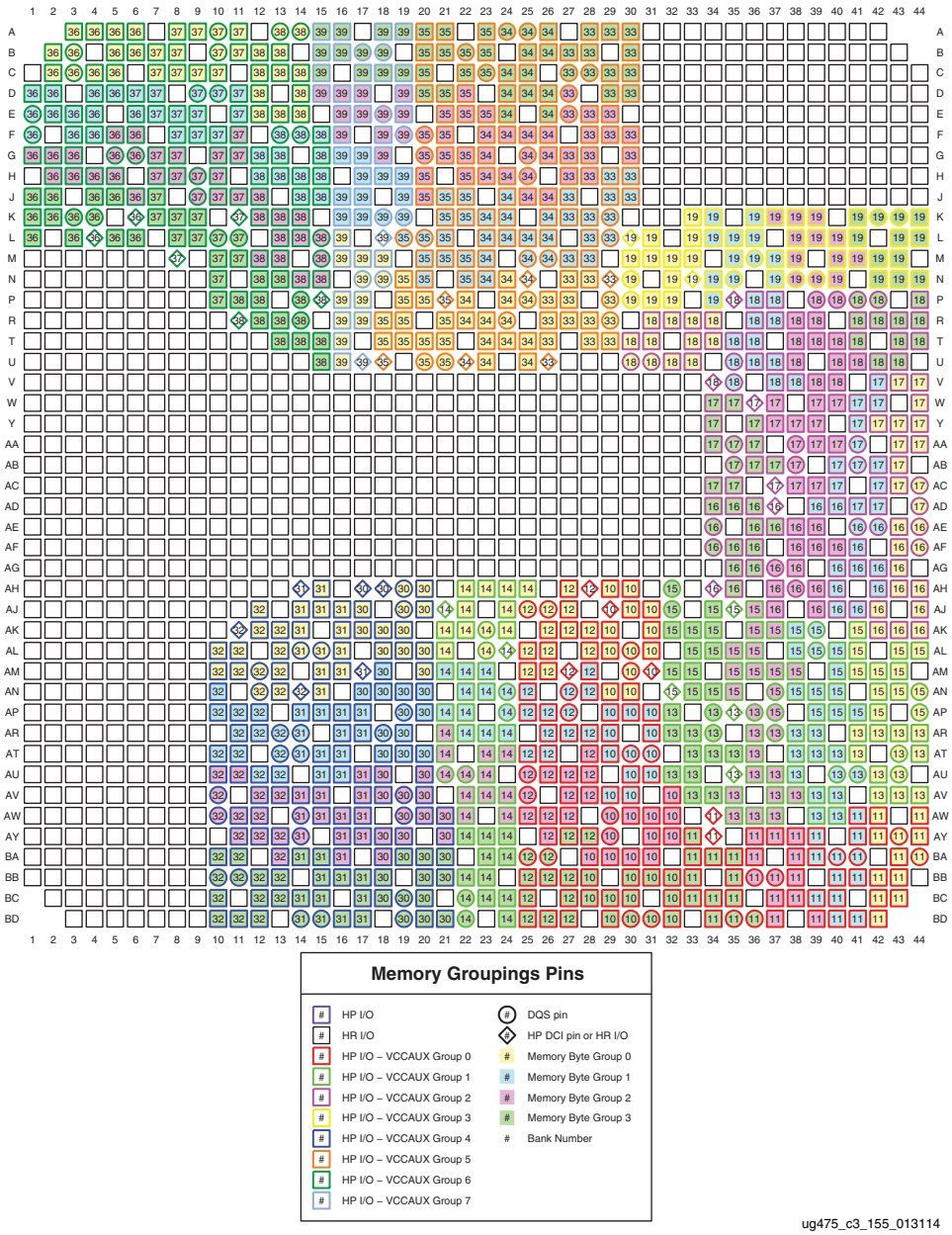


Figure 3-199: **FF1930, FFG1930, and RF1930 Packages—XC7VX690T Memory Groupings**

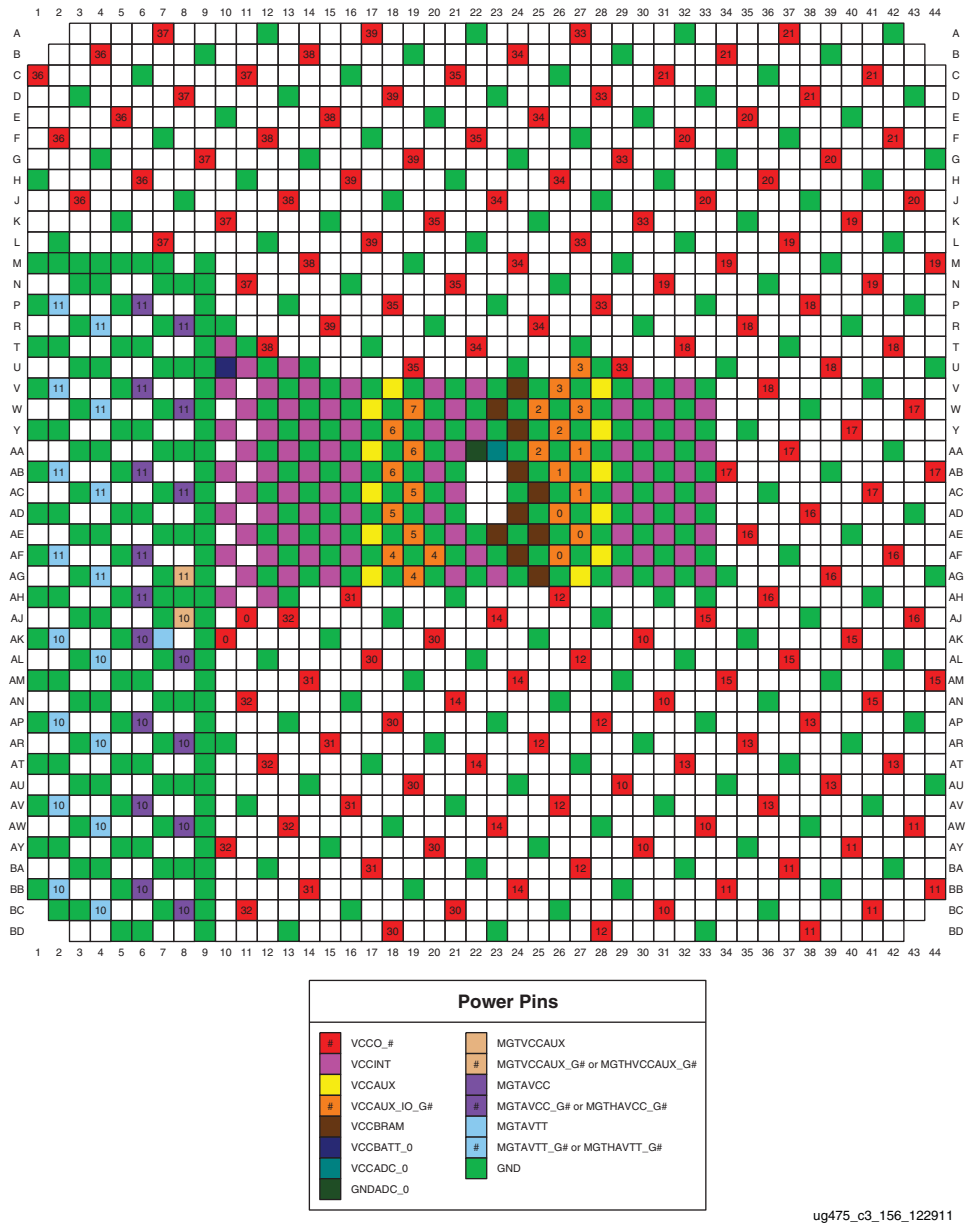


Figure 3-200: **FF1930, FFG1930, and RF1930 Packages—XC7VX690T Power and GND Placement**

FF1928 and FFG1928 Packages—XC7VX980T

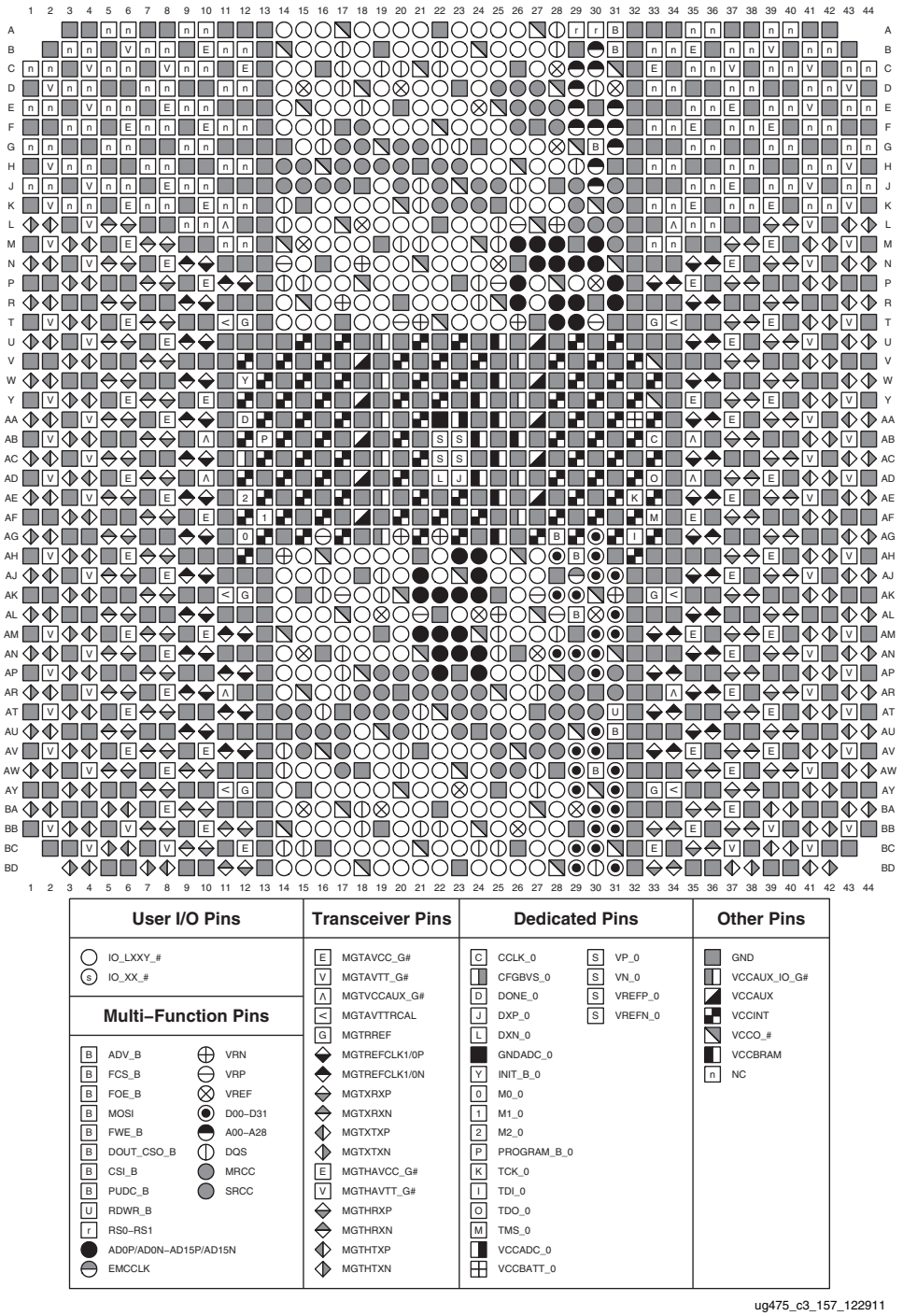


Figure 3-201: **FF1928 and FFG1928 Packages—XC7VX980T Pinout Diagram**

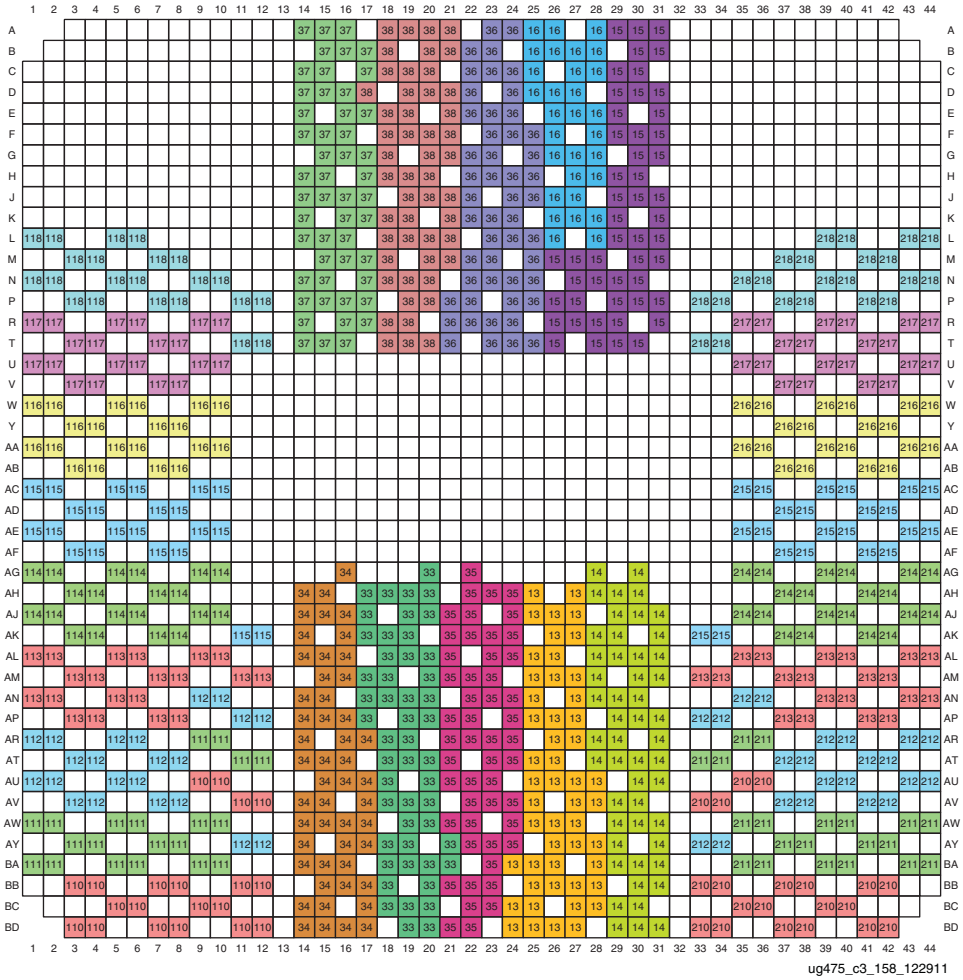


Figure 3-202: **FF1928 and FFG1928 Packages—XC7VX980T I/O Banks**

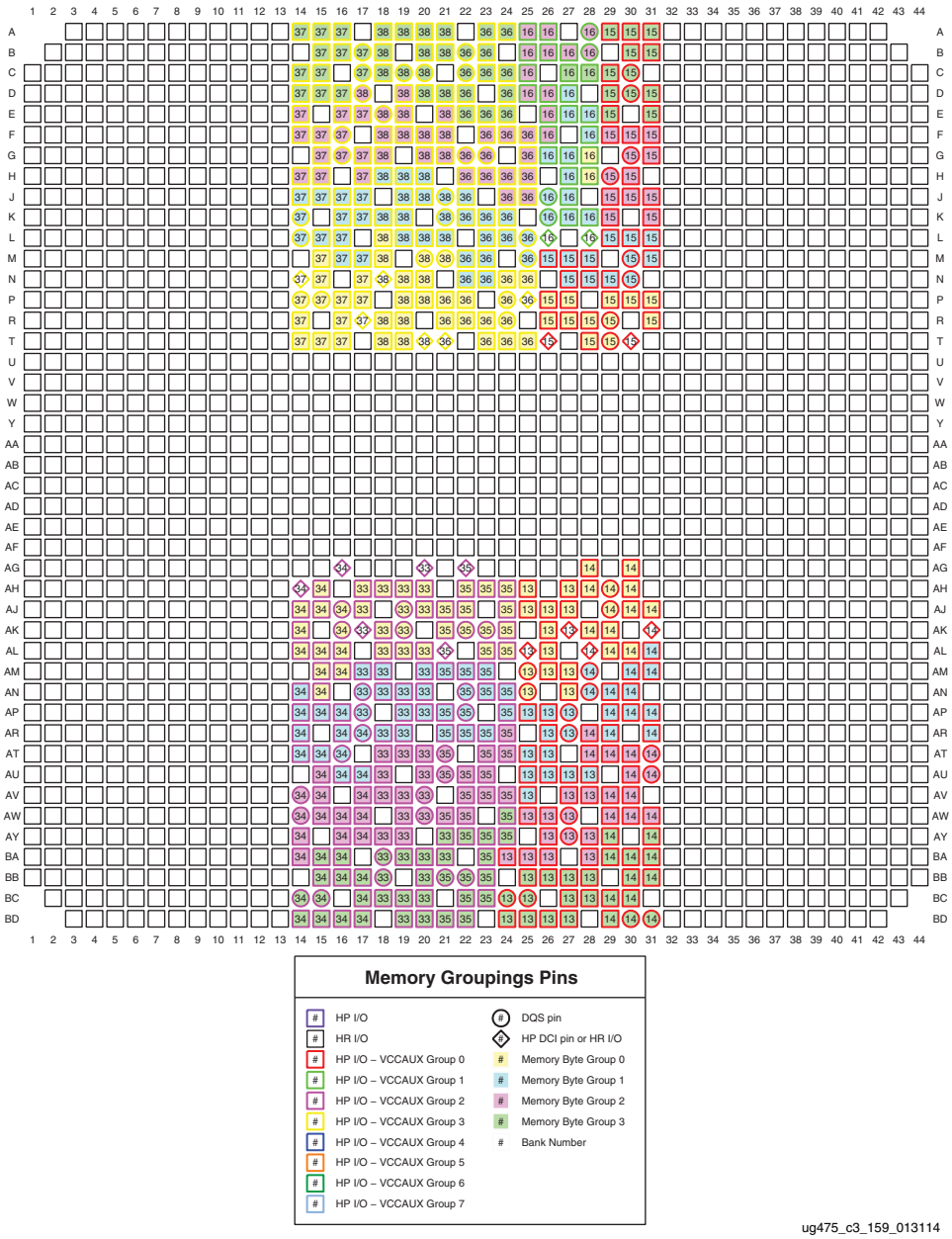


Figure 3-203: **FF1928 and FFG1928 Packages—XC7VX980T Memory Groupings**

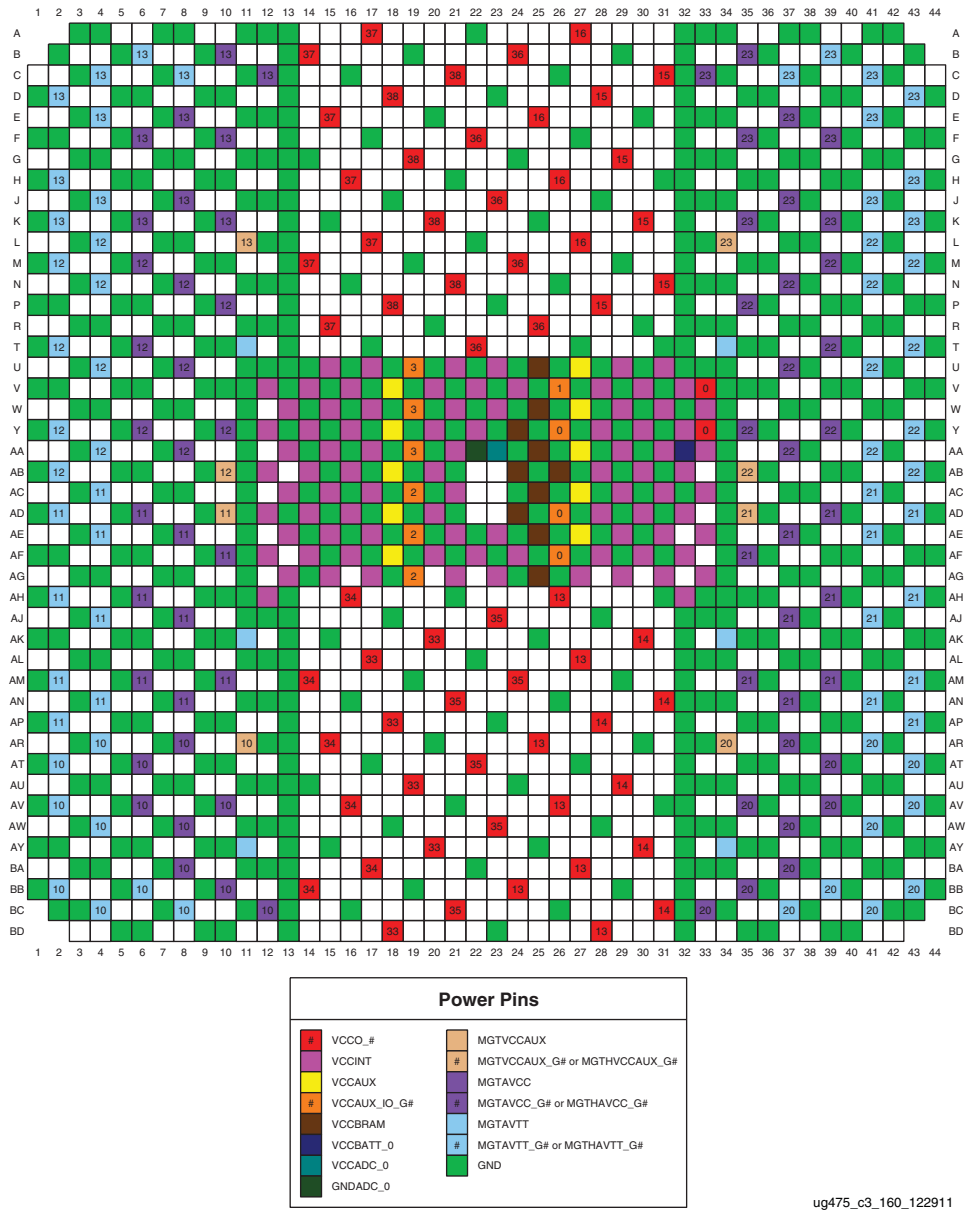


Figure 3-204: **FF1928 and FFG1928 Packages—XC7VX980T Power and GND Placement**

FF1930, FFG1930, and RF1930 Packages—XC7VX980T

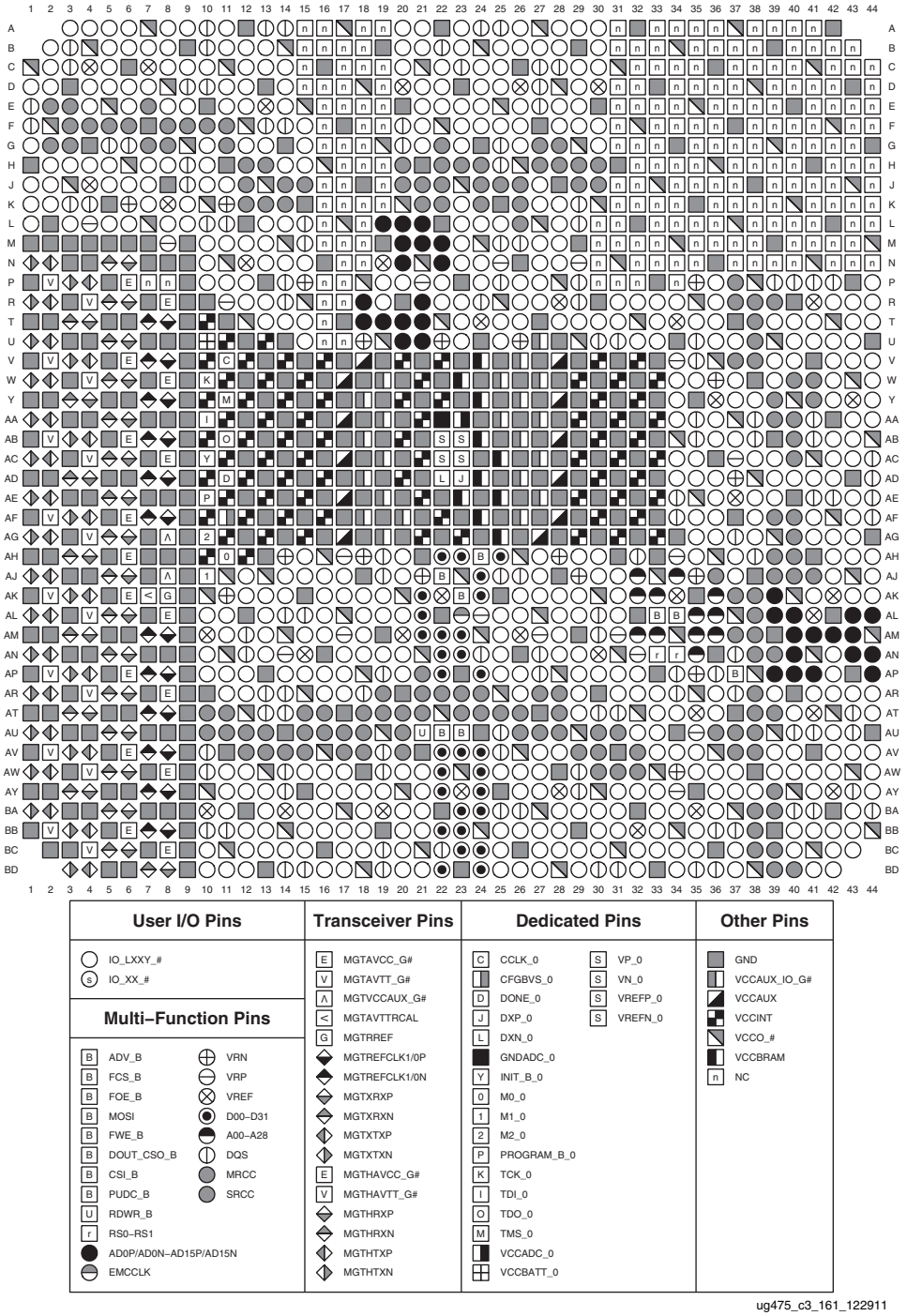


Figure 3-205: **FF1930, FFG1930, and RF1930 Packages—XC7VX980T Pinout Diagram**

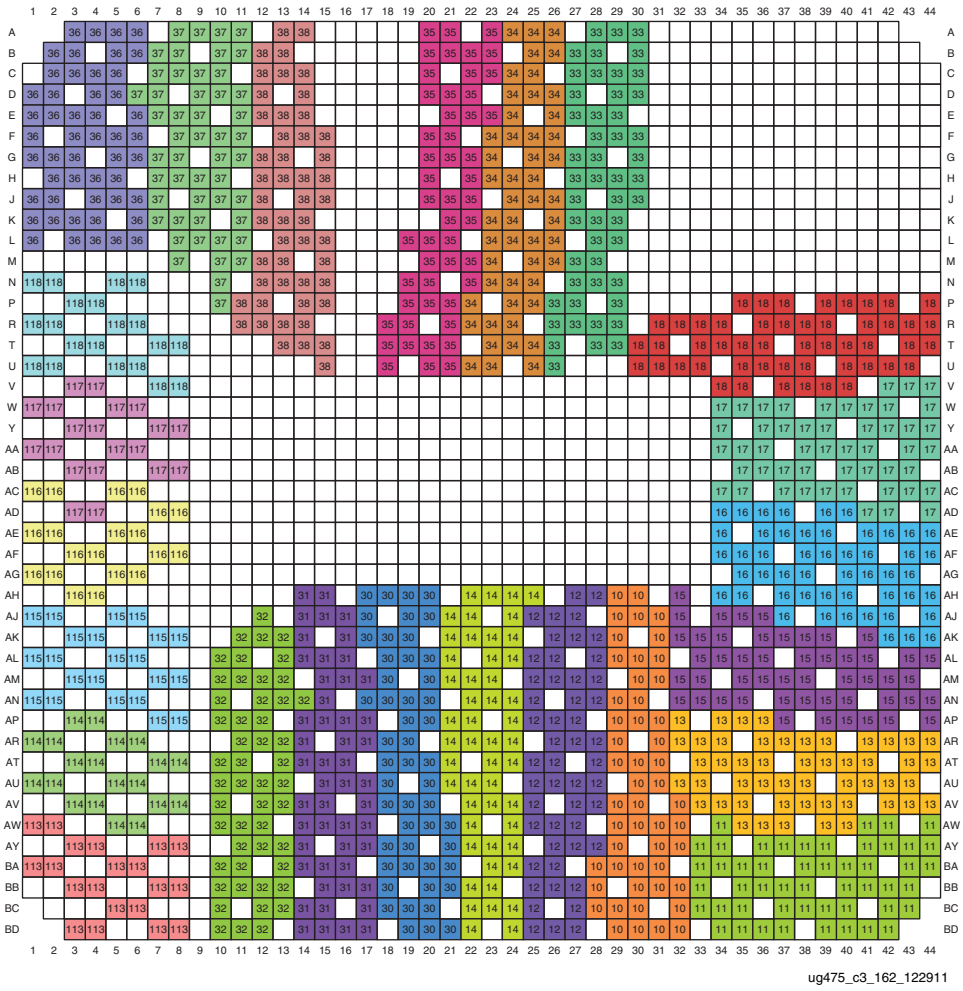


Figure 3-206: **FF1930, FFG1930, and RF1930 Packages—XC7VX980T I/O Banks**

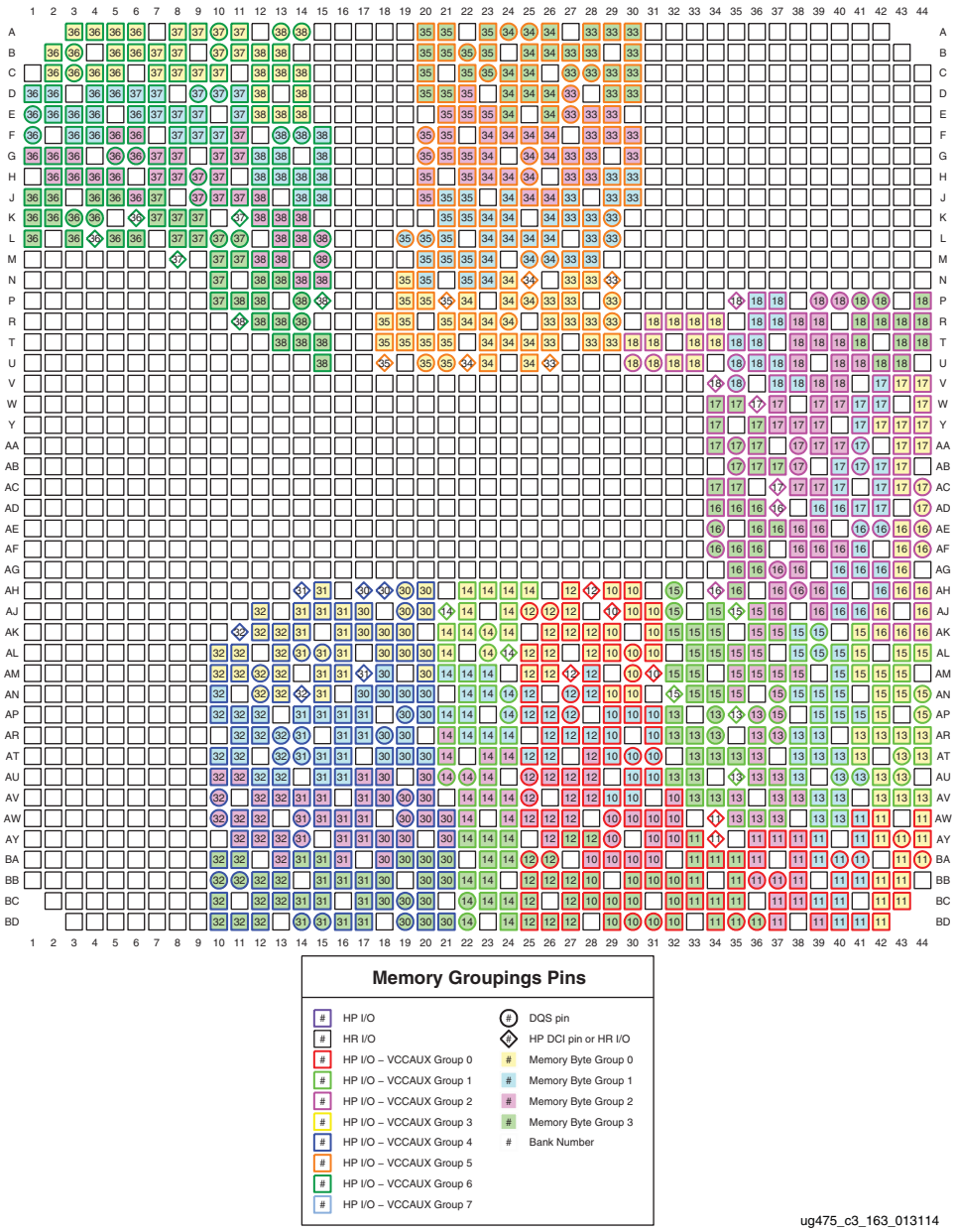


Figure 3-207: **FF1930, FFG1930, and RF1930 Packages—XC7VX980T Memory Groupings**

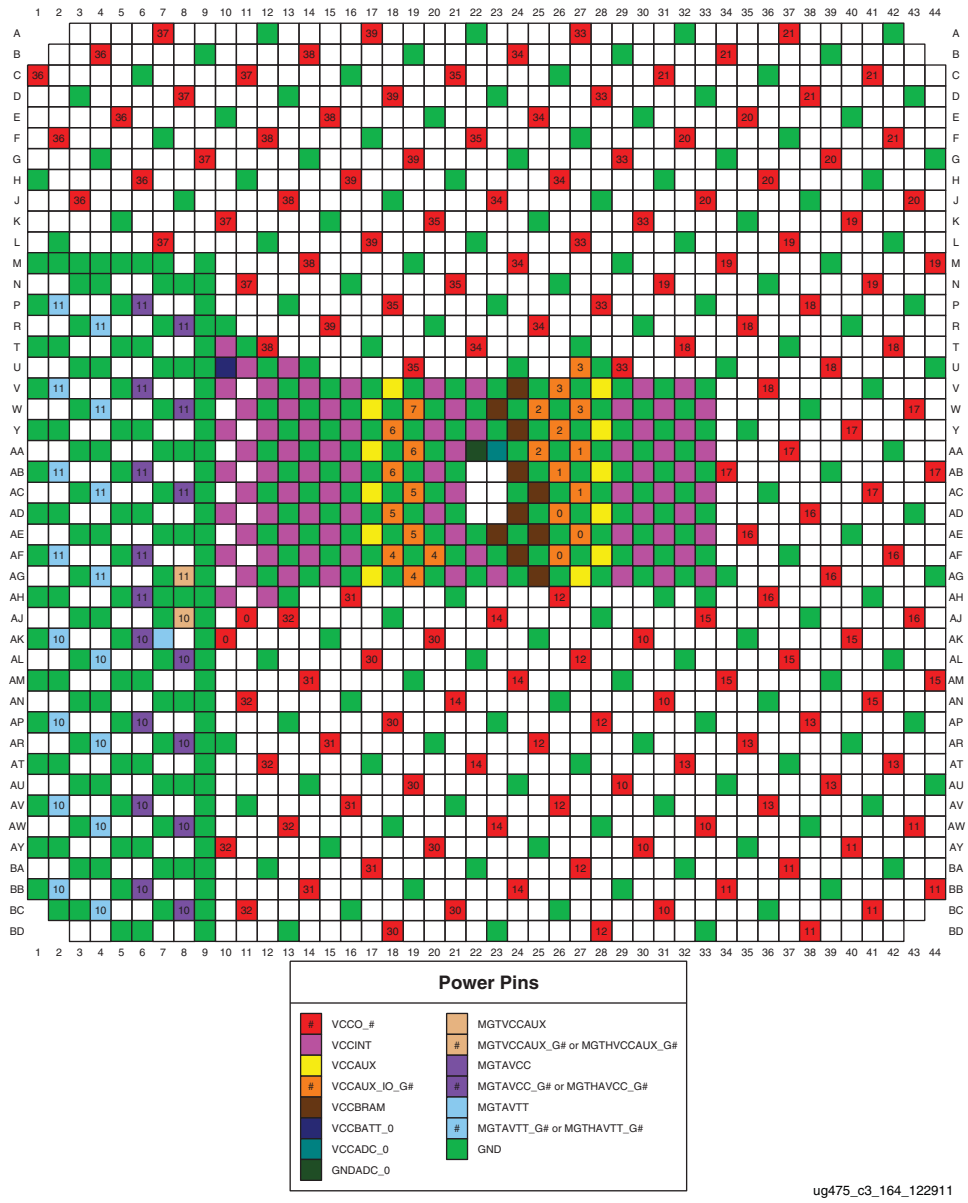


Figure 3-208: **FF1930, FFG1930, and RF1930 Packages—XC7VX980T Power and GND Placement**

FL1926 and FLG1926 Packages—XC7VX1140T

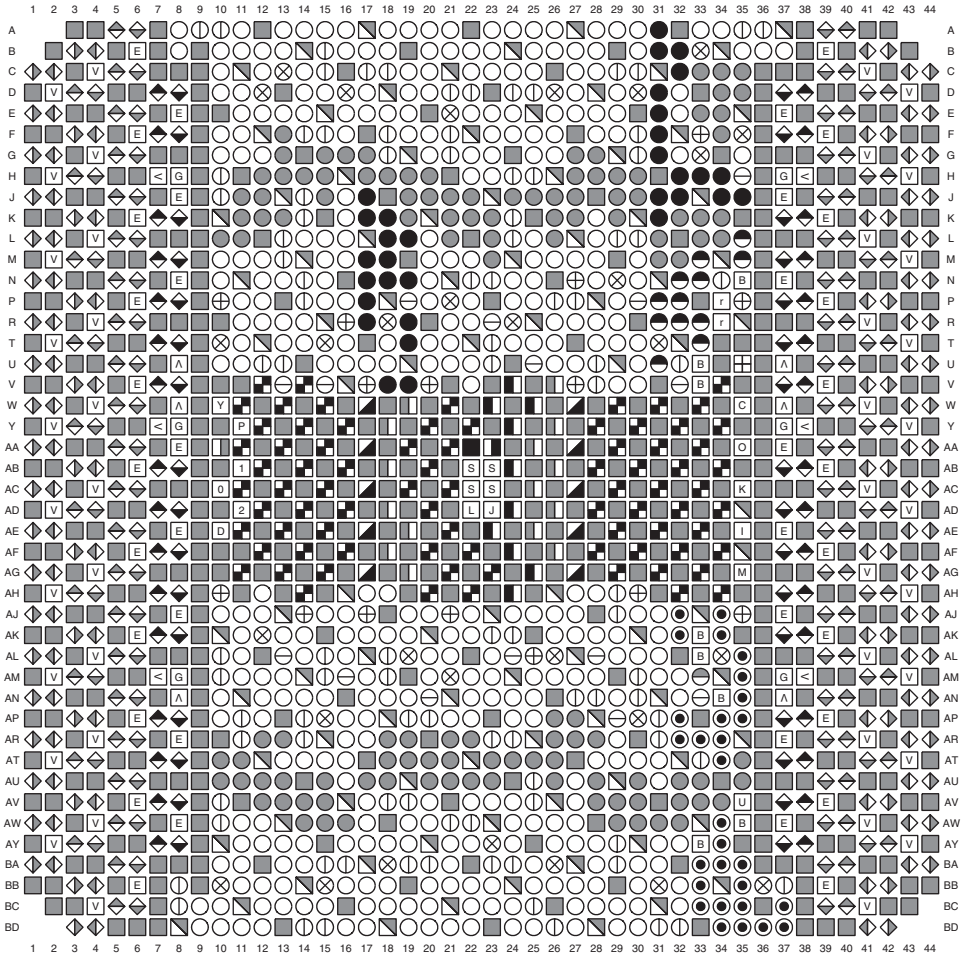


Figure 3-209: **FL1926 and FLG1926 Packages—XC7VX1140T Pinout Diagram**

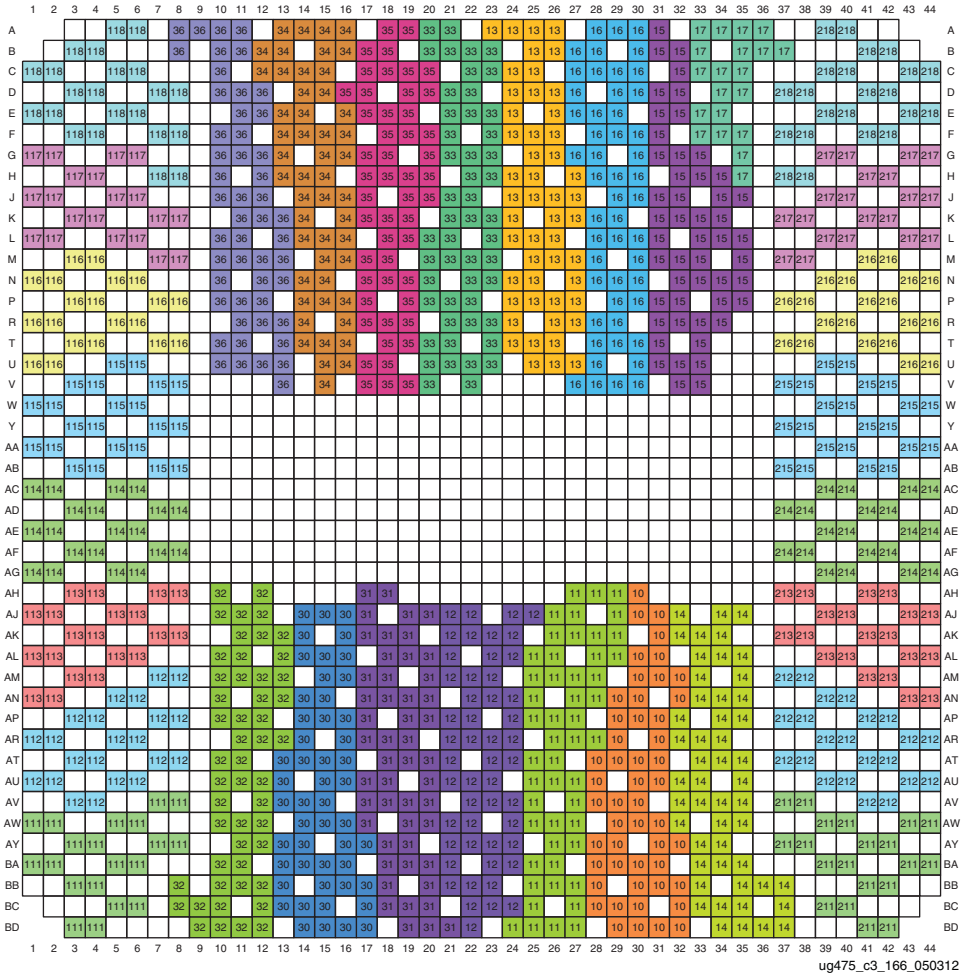


Figure 3-210: **FL1926 and FLG1926 Packages—XC7VX1140T I/O Banks**

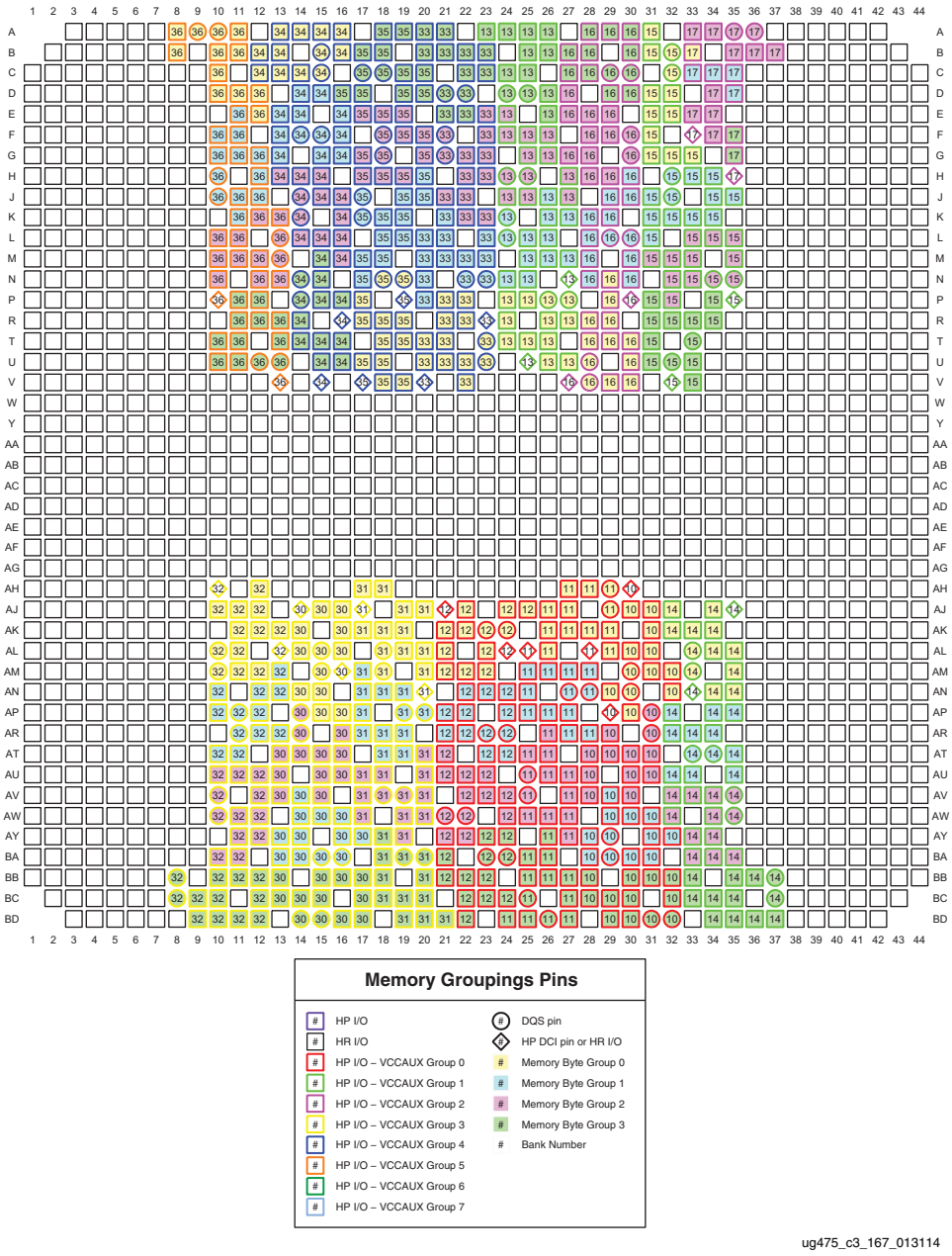


Figure 3-211: **FL1926 and FLG1926 Packages—XC7VX1140T Memory Groupings**

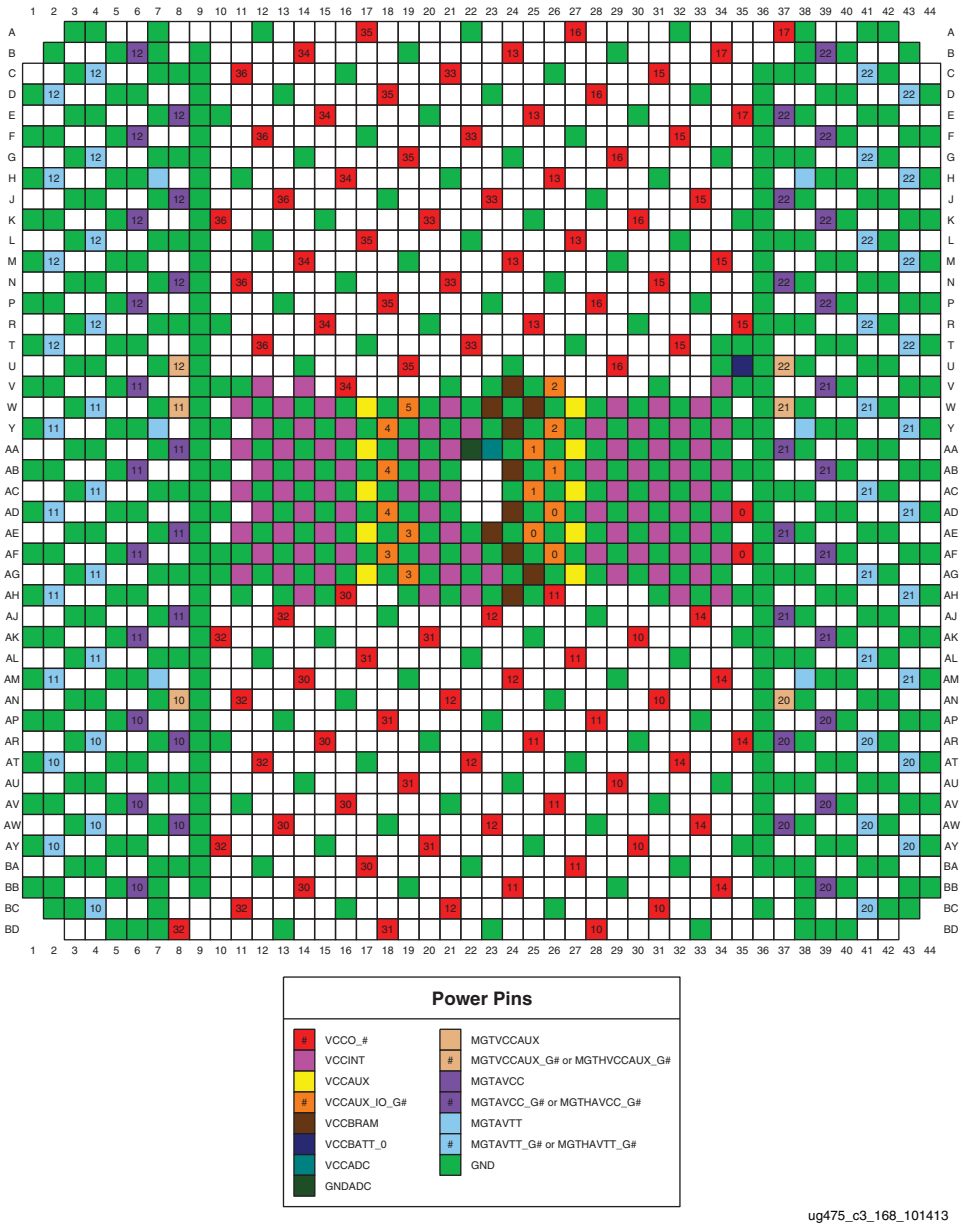


Figure 3-212: **FL1926 and FLG1926 Packages—XC7VX1140T Power and GND Placement**

FL1928 and FLG1928 Packages—XC7VX1140T

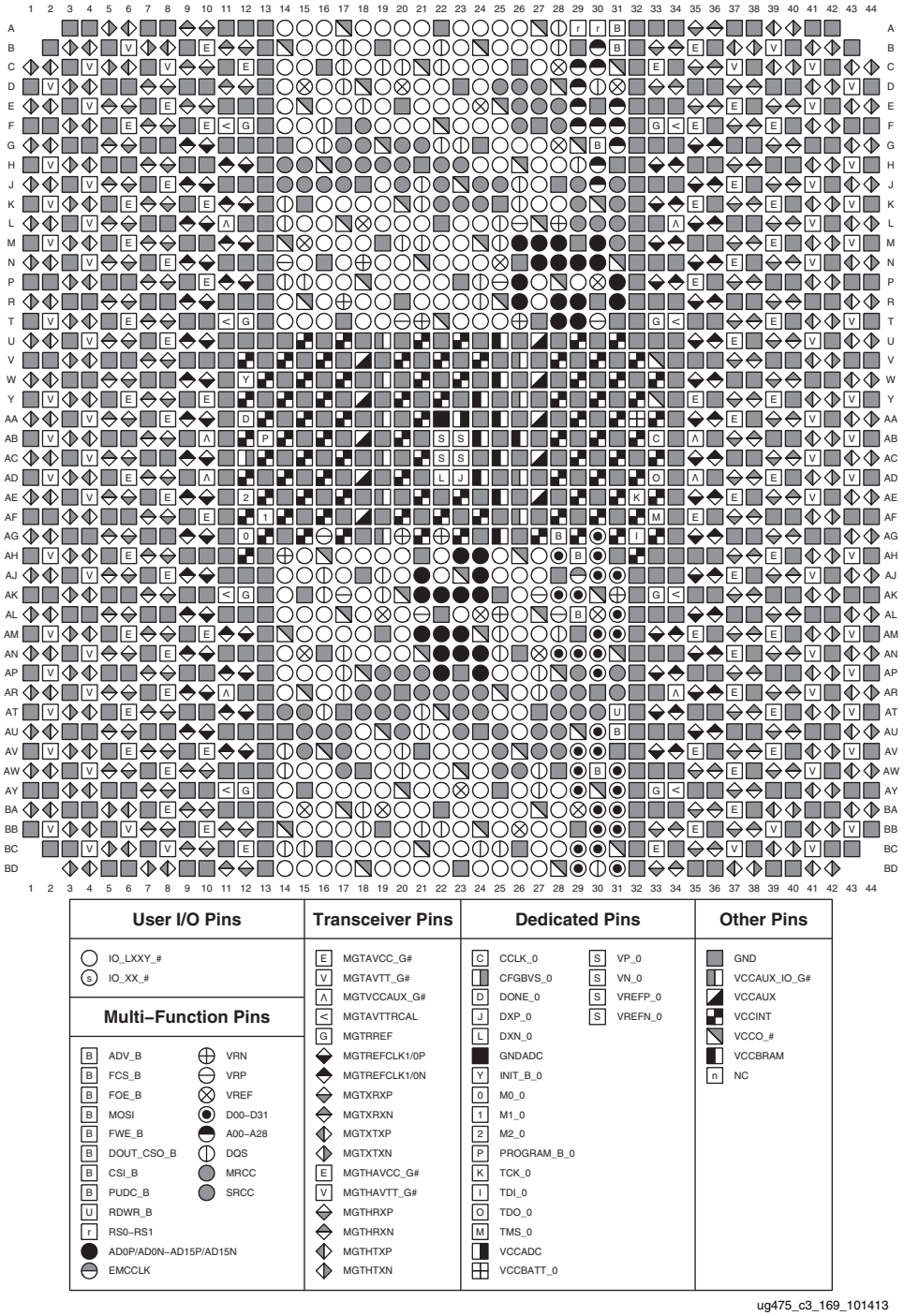


Figure 3-213: **FL1928 and FLG1928 Packages—XC7VX1140T Pinout Diagram**

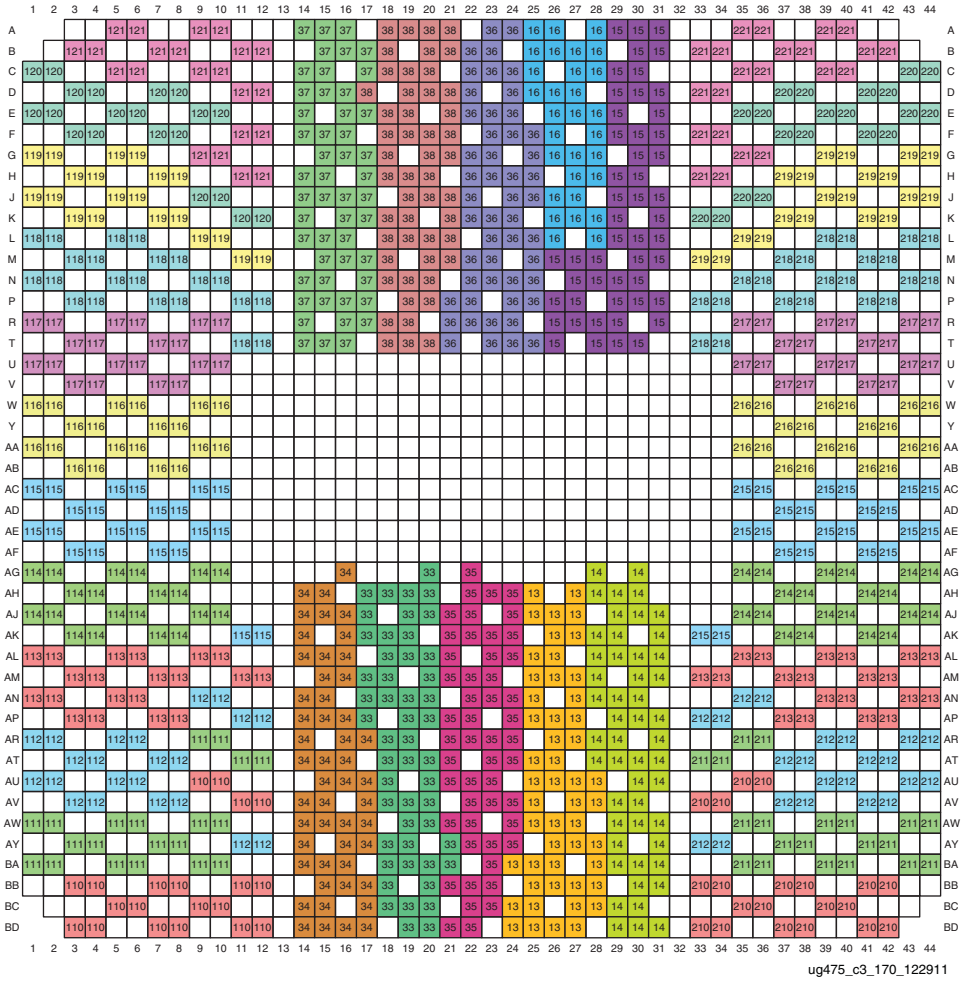


Figure 3-214: **FL1928 and FLG1928 Packages—XC7VX1140T I/O Banks**

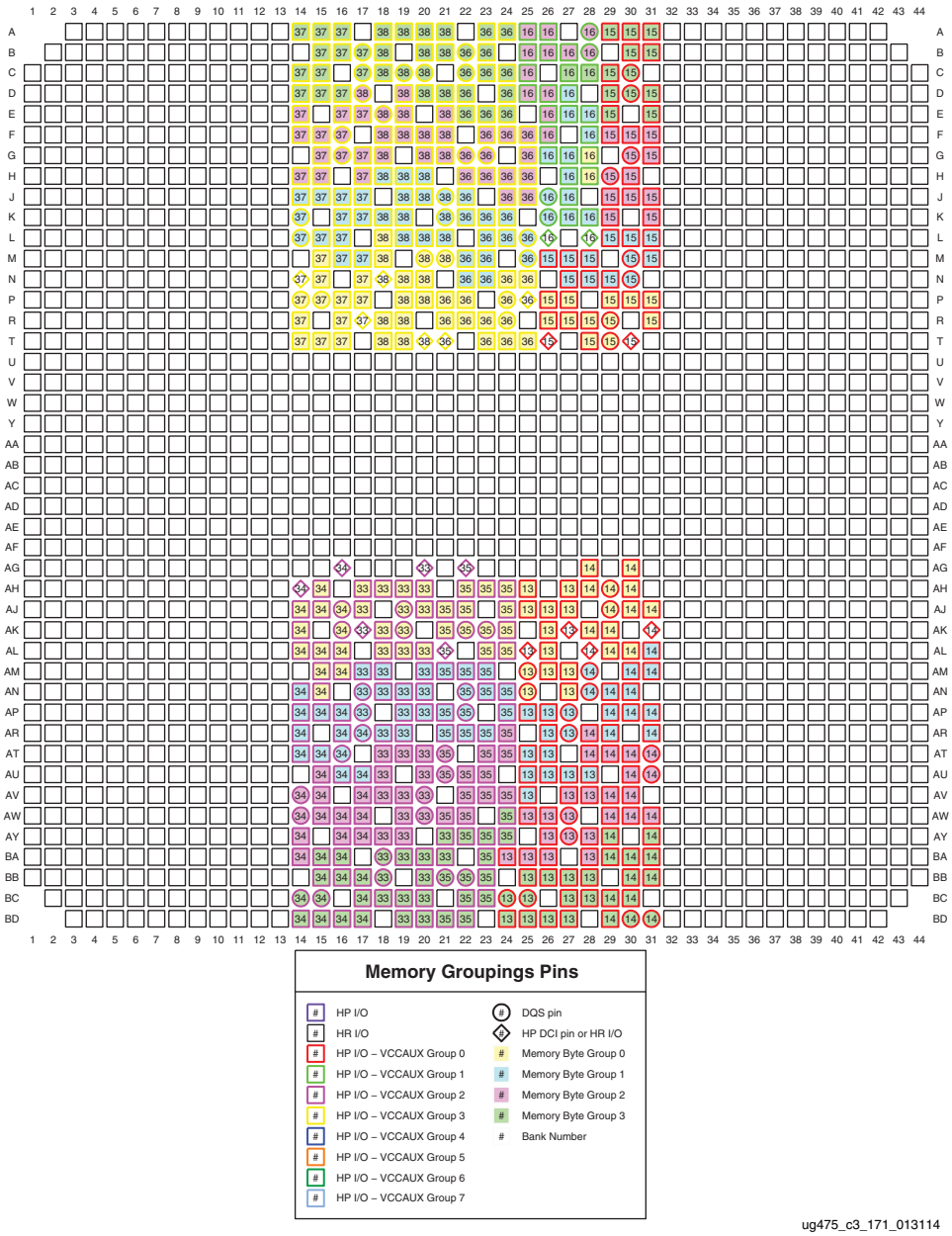


Figure 3-215: **FL1928 and FLG1928 Packages—XC7VX1140T Memory Groupings**

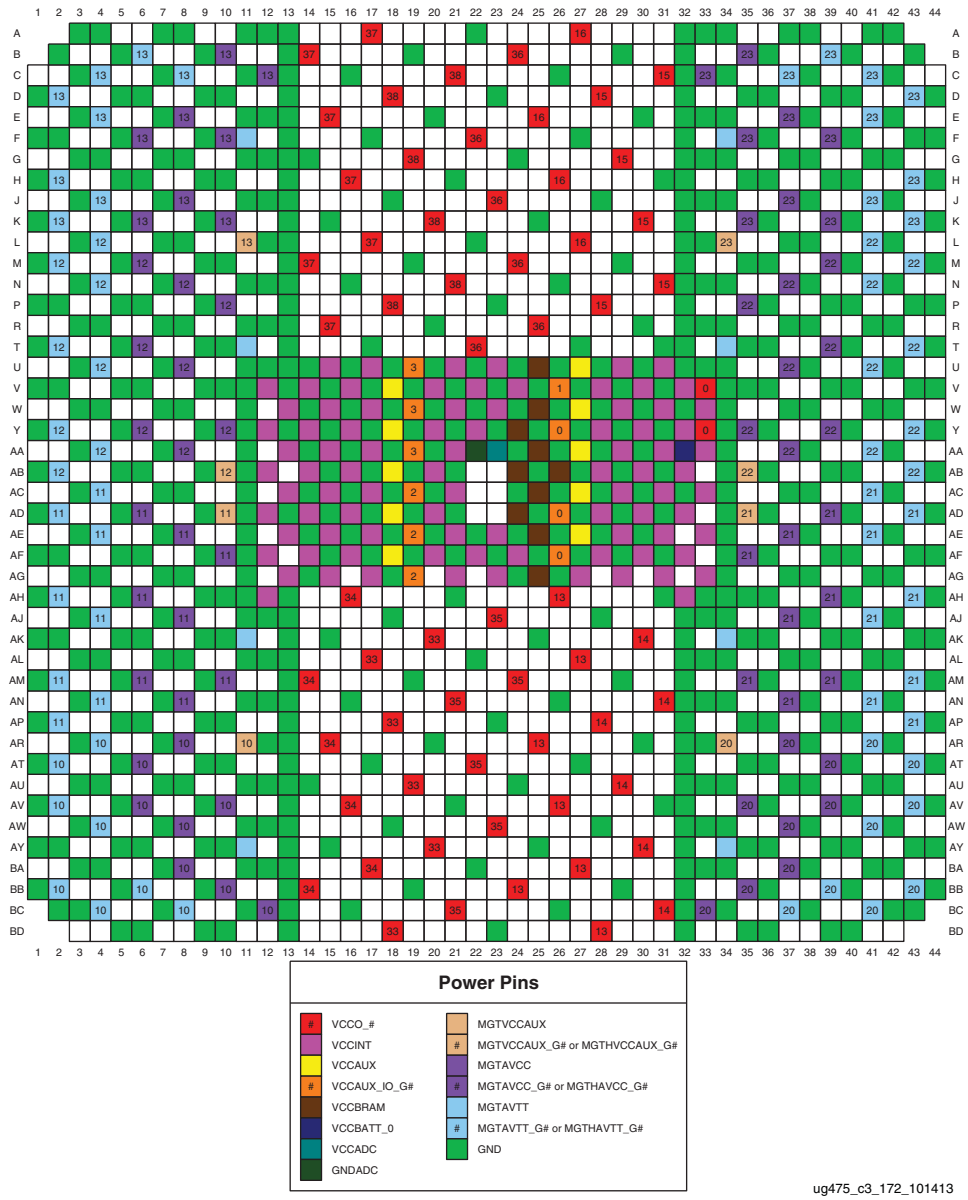


Figure 3-216: **FL1928 and FLG1928 Packages—XC7VX1140T Power and GND Placement**

FL1930 and FLG1930 Packages—XC7VX1140T

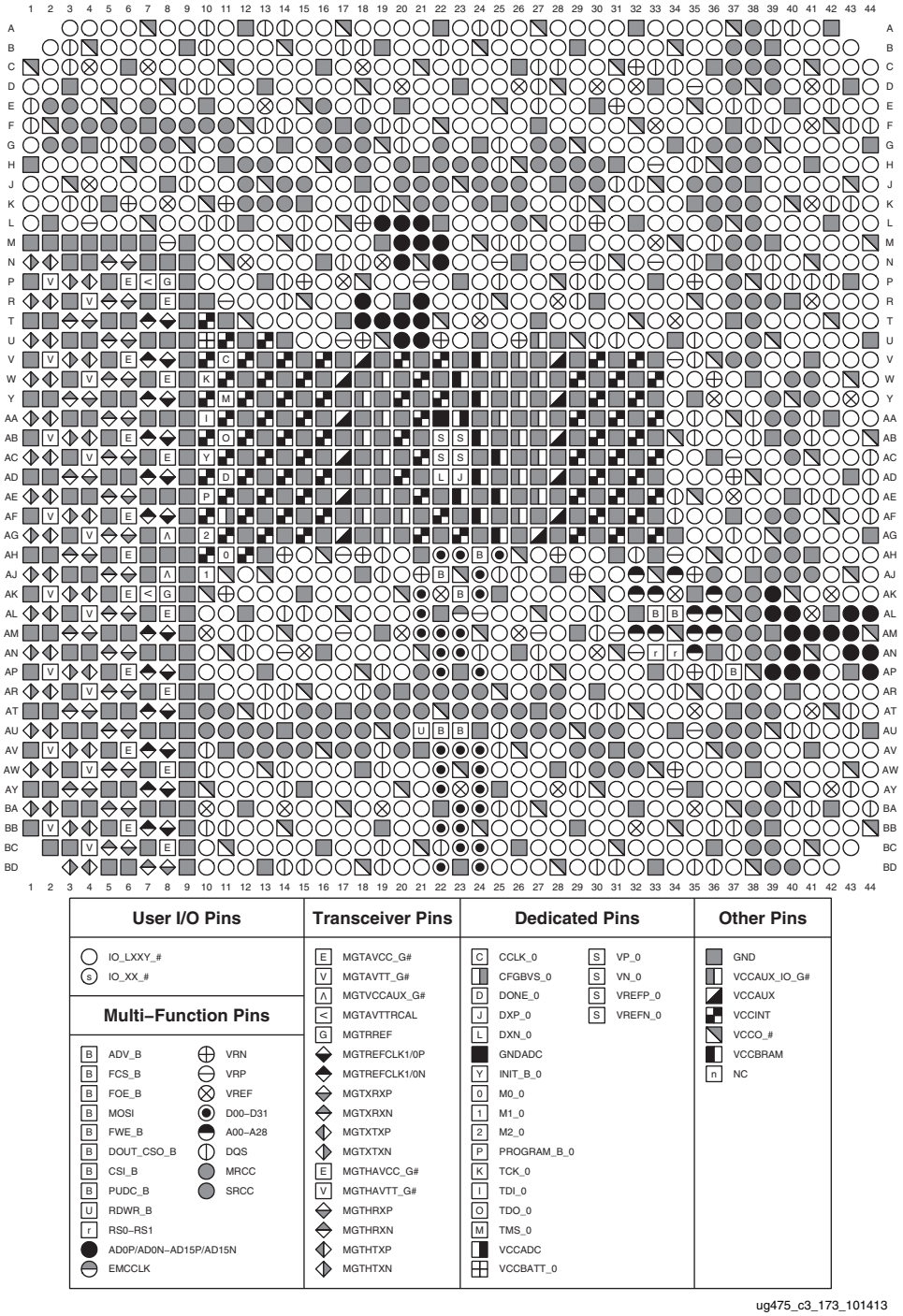


Figure 3-217: **FL1930 and FLG1930 Packages—XC7VX1140T Pinout Diagram**

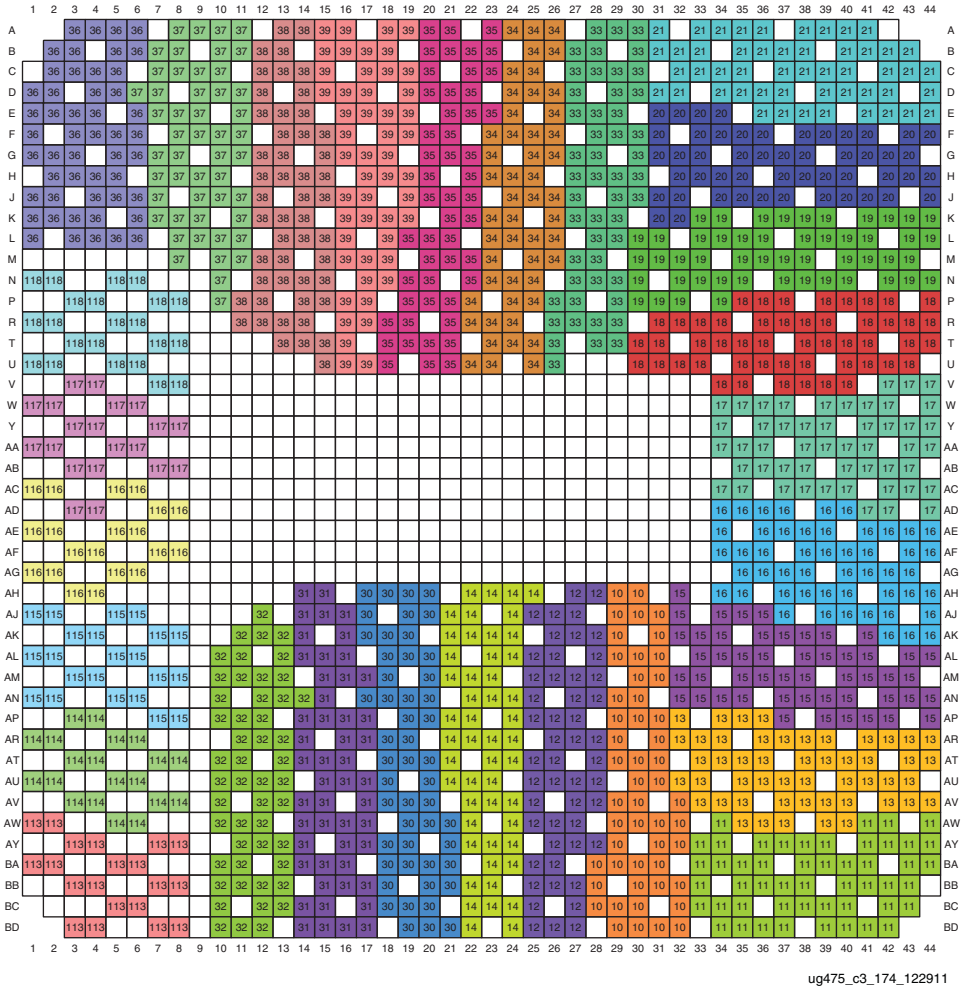


Figure 3-218: **FL1930 and FLG1930 Packages—XC7VX1140T I/O Banks**

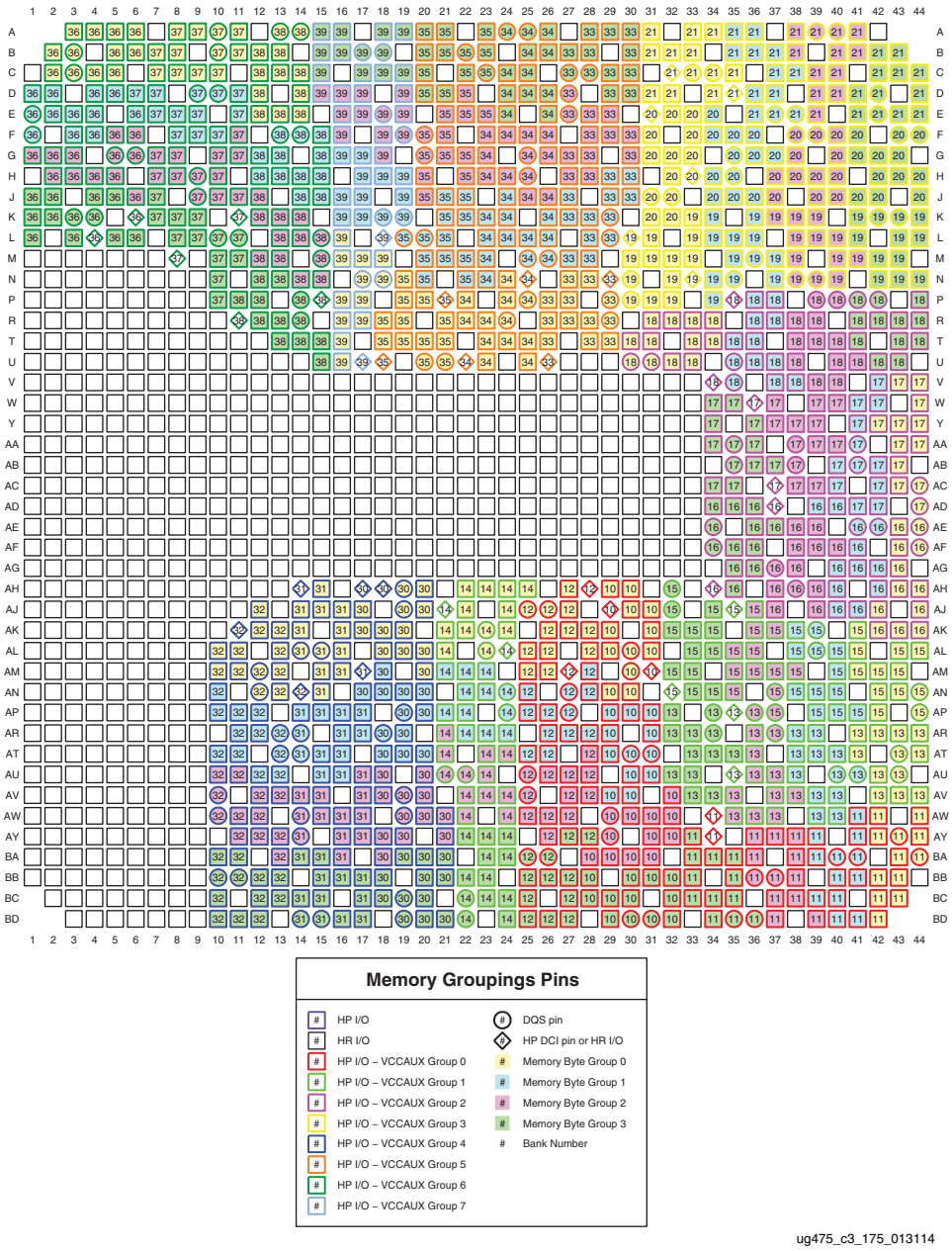


Figure 3-219: **FL1930 and FLG1930 Packages—XC7VX1140T Memory Groupings**

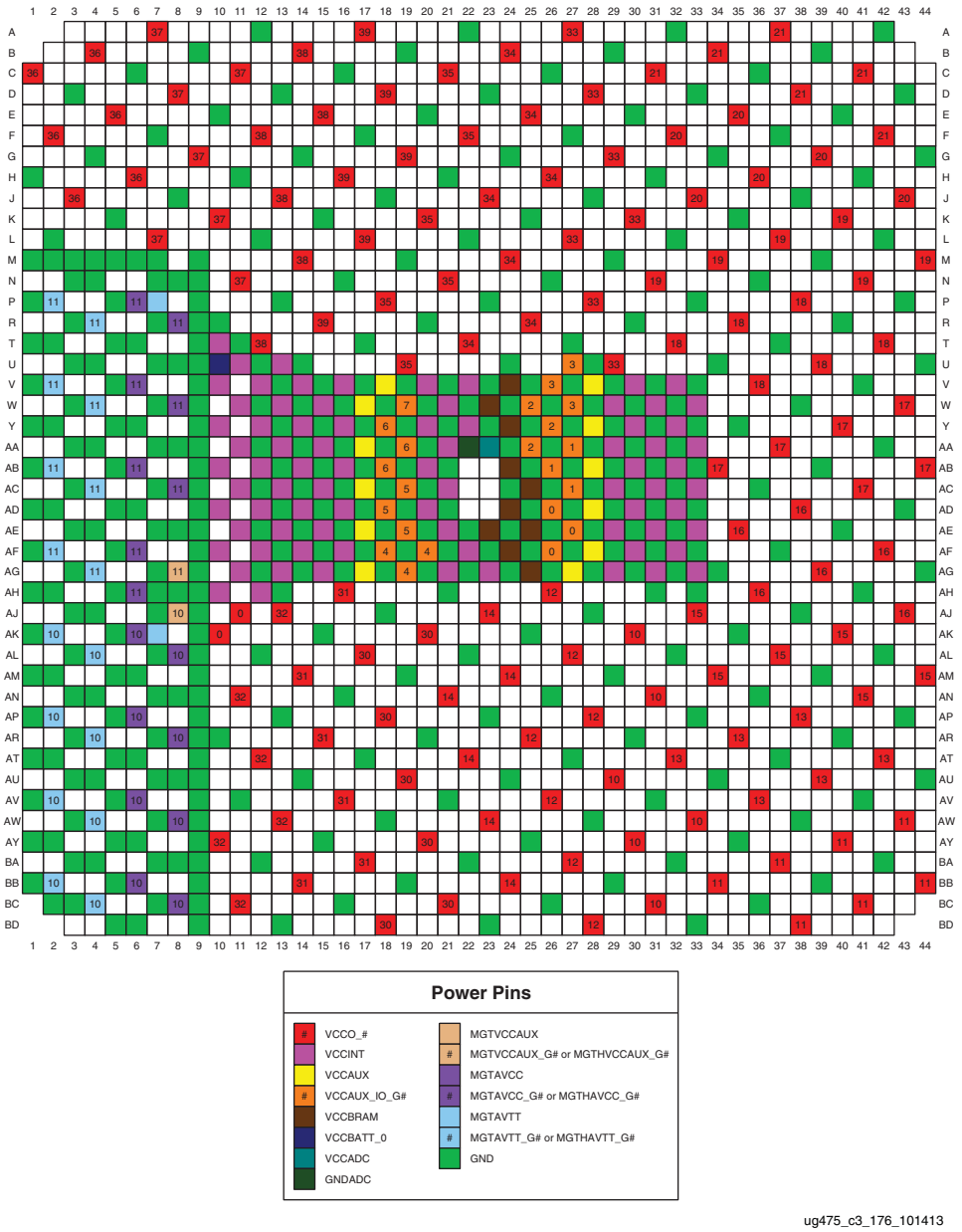


Figure 3-220: **FL1930 and FLG1930 Packages—XC7VX1140T Power and GND Placement**

Mechanical Drawings

Summary

This chapter provides mechanical drawings (package specifications) of the following 7 series (Artix®-7, Kintex®-7, Spartan®-7, and Virtex®-7 FPGA) packages.

Spartan-7 FPGAs

- CPGA196 (Spartan-7 FPGAs) Wire-Bond Chip-Scale BGA (0.5 mm Pitch), page 258
- FTGB196 (Spartan-7 FPGAs) Wire-Bond Chip-Scale BGA (1.0 mm Pitch), page 259
- CSGA225 (Spartan-7 FPGAs) Wire-Bond Chip-Scale BGA (0.8 mm Pitch), page 260
- CSGA324 (Spartan-7 FPGAs) Wire-Bond Chip-Scale BGA (0.8 mm Pitch), page 261
- FGGA484 (Spartan-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch), page 262
- FGGA676 (Spartan-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch), page 263

Artix-7 FPGAs

- CP236 and CPG236 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.5 mm Pitch), page 264
- CPG238 (Artix-7 FPGAs: XC7A12T and XC7A25T) Wire-Bond Chip-Scale BGA (0.5 mm Pitch), page 265
- CS/CSG324 and CS/CSG325 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.8 mm Pitch), page 266
- FT/FTG256 (Artix-7 FPGAs) Wire-Bond Fine-Pitch Thin BGA (1.0 mm Pitch), page 267
- SB484, SBG484, and SBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (0.8 mm Pitch), page 268
- FB484, FBG484, and FBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 269
    - XC7A200T FB484, FBG484, and FBV484 Die Dimensions, page 270

- FB676, FBG676, and FBV676 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 271
  - XC7A200T FB676, FBG676, and FBV676 Die Dimensions, page 272
- FG484 and FGG484 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch), page 273
- FG676 and FGG676 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch), page 274
- FF1156, FFG1156, and FFV1156 (Artix-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 275
- RB484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 276
- RS484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (0.8 mm Pitch), page 277
- RB676 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch), page 278

Kintex-7 FPGAs

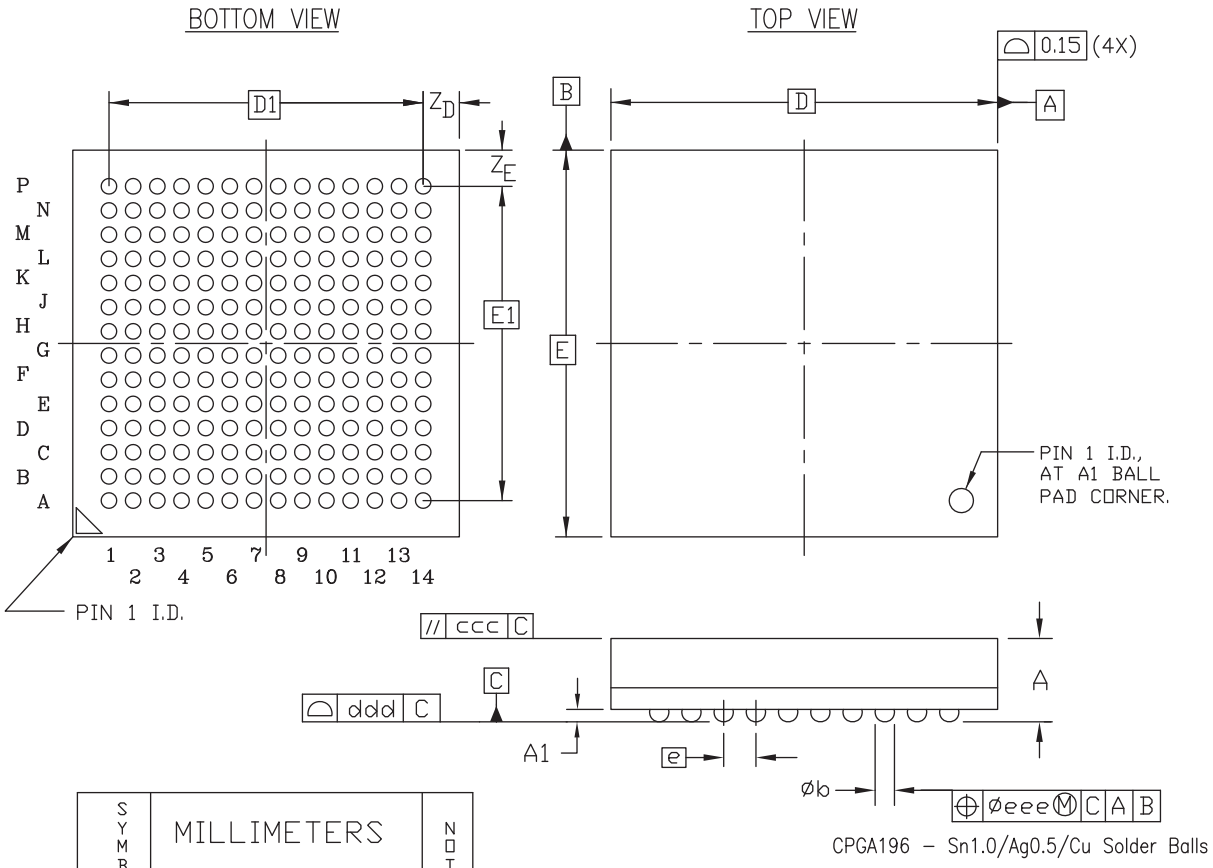
- FB484, FBG484, and FBV484 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 279
  - XC7K70T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations, page 280
  - XC7K160T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations, page 281
- FB676, FBG676, and FBV676 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 282
  - XC7K70T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 283
  - XC7K160T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 284
  - XC7K325T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 285
  - XC7K410T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations, page 286
- FB900, FBG900, and FBV900 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch), page 287
  - XC7K325T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations, page 288
  - XC7K410T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations, page 289
- FF676, FFG676, and FFV676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 290

- There are two drawings for FF900 and FFG900 packages. They are device dependent:
  - FF900 and FFG900 (XC7K325T and XC7K410T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid, page 291
  - FF900, FFG900, FFV900, FF901, FFG901, and FFV901 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 292
- There are two drawings for FF1156 and FFG1156 packages. They are device dependent:
  - FF1156 and FFG1156 (XC7K420T and XC7K480T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid, page 293
  - FF1156, FFG1156, and FFV1156 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 294
- RF676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 295
- RF900 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 296

Virtex-7 FPGAs

- FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 297
- FF1761 and FFG1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 298
- FFV1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 299
- FH1761 and FHG1761 (Virtex-7 T FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 300
- FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 (Virtex-7 XT FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 301
- FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch), page 302
- RF1157 and RF1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch), page 303
- RF1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch), page 304
- RF1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch), page 305

CPGA196 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.5 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		1.00	1.10	
A_1	0.15	0.20	0.25	
D/E	7.90	8.00	8.10	
D_1/E_1	6.50 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc			0.10	
ddd			0.08	
eee			0.15	
Z_D/Z_E	0.60	0.75	0.90	
M	14			2

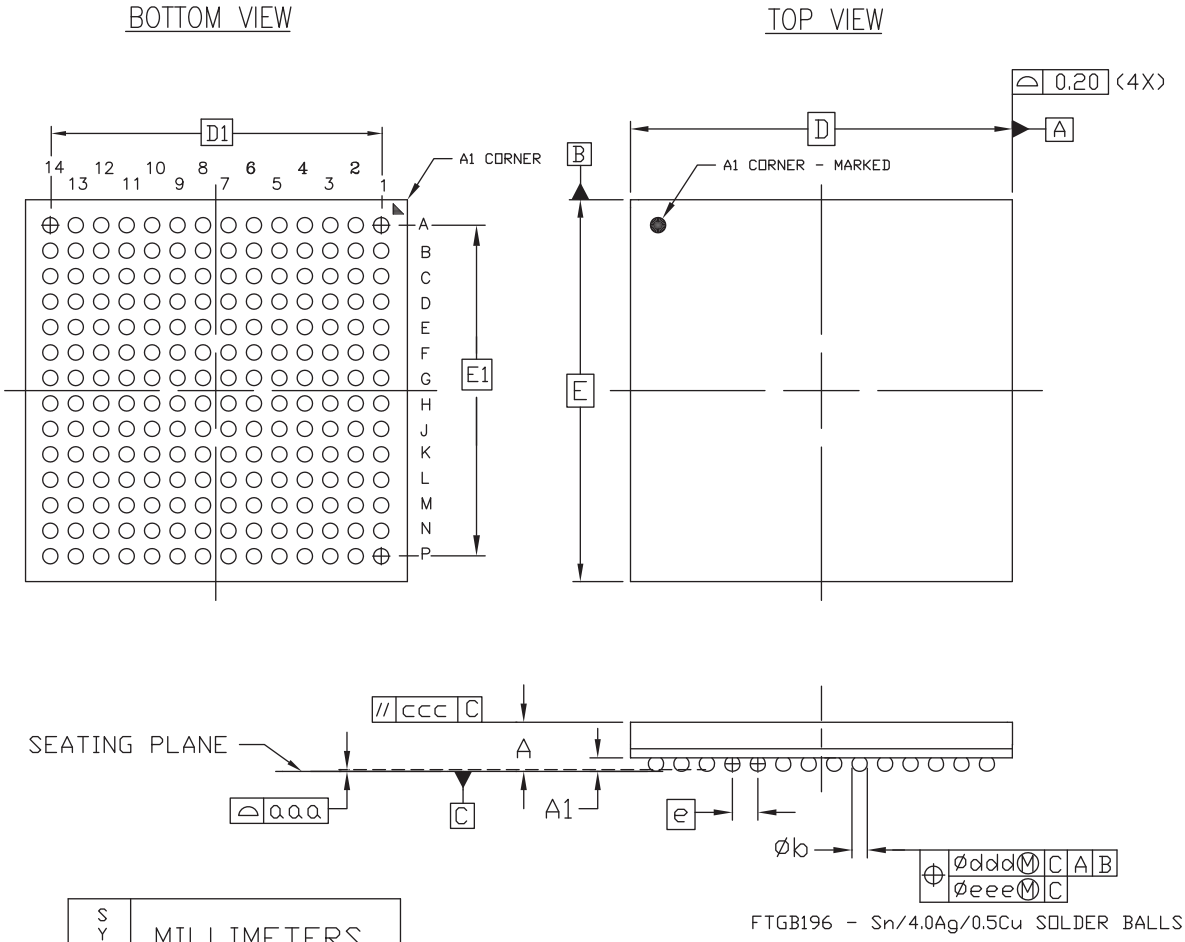
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–275

ug475_c4_cpga196_s7_042617

Figure 4-1: **CPGA196 Wire-Bond Chip-Scale BGA Package Specifications for Spartan-7 FPGAs**

FTGB196 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.46	1.55
A_1	0.30	0.40	0.50
D/E	15.00 BSC		
D_1/E_1	13.00 BSC		
e	1.00 BSC		
øb	0.40	0.50	0.60
aaa			0.20
ccc			0.15
ddd			0.25
eee			0.10
M	14		

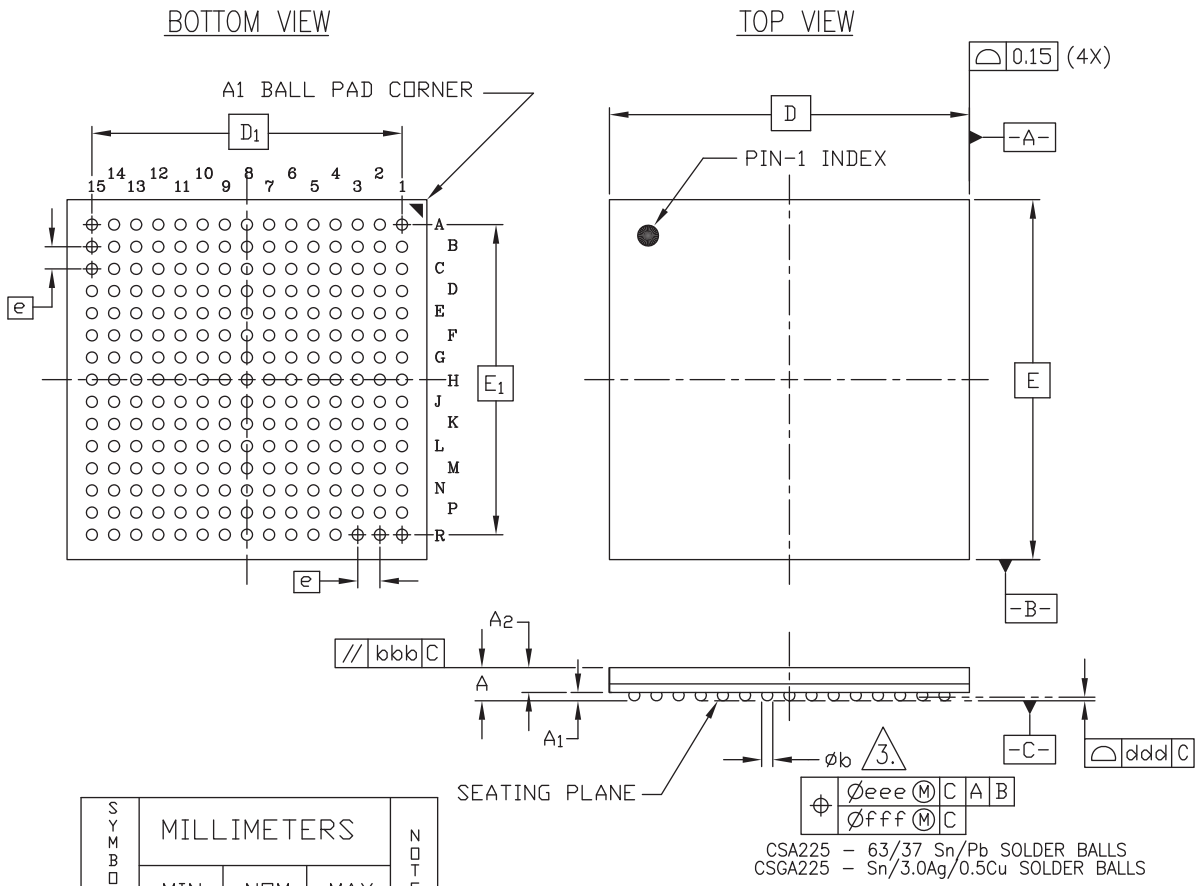
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAE–1 EXCEPT FOR THE SOLDER BALL SIZE.

ug475_c4_ftgb196_s7_061517

Figure 4-2: **FTGB196 Wire-Bond Chip-Scale BGA Package Specifications for Spartan-7 FPGAs**

CSGA225 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00	~	1.40	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.00	
D/E	13.00 BSC			
D_1/E_1	11.20 BSC			
e	0.80 BSC			
øb	0.35	0.40	0.45	3
bbb	~	~	0.20	
ddd	~	~	0.10	
eee	~	~	0.15	
fff	~	~	0.08	
M	15			2

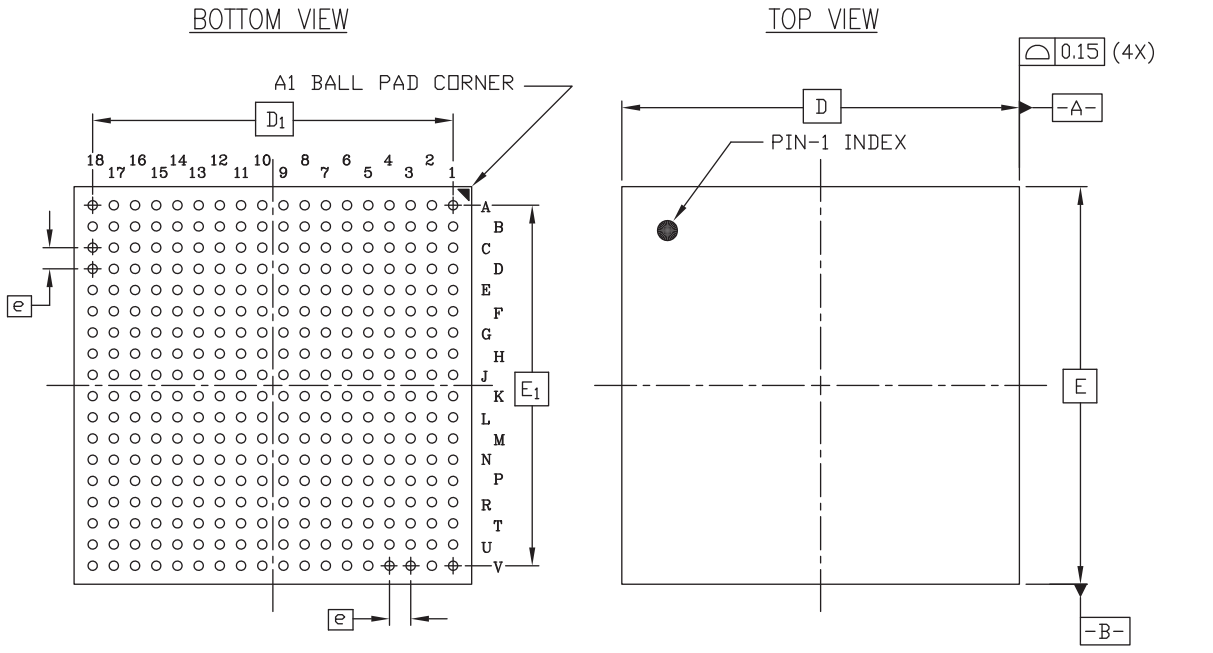
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. CONFORMS TO JEDEC MO–275–HHAC–1.

ug475_c4_csga225_s7_042617

Figure 4-3: **CSGA225 Wire-Bond Chip-Scale BGA Package Specifications for Spartan-7 FPGAs**

CSGA324 (Spartan-7 FPGAs)
Wire-Bond Chip-Scale BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.00		1.50	
A_1	0.25	0.30	0.40	
A_2	0.75	0.90	1.10	
D/E	15.00 BSC			
D_1/E_1	13.60 BSC			
e	0.80 BSC			
øb	0.40	0.45	0.50	3
bbb			0.20	
ddd			0.20	
eee			0.15	
fff			0.08	
M	18			2

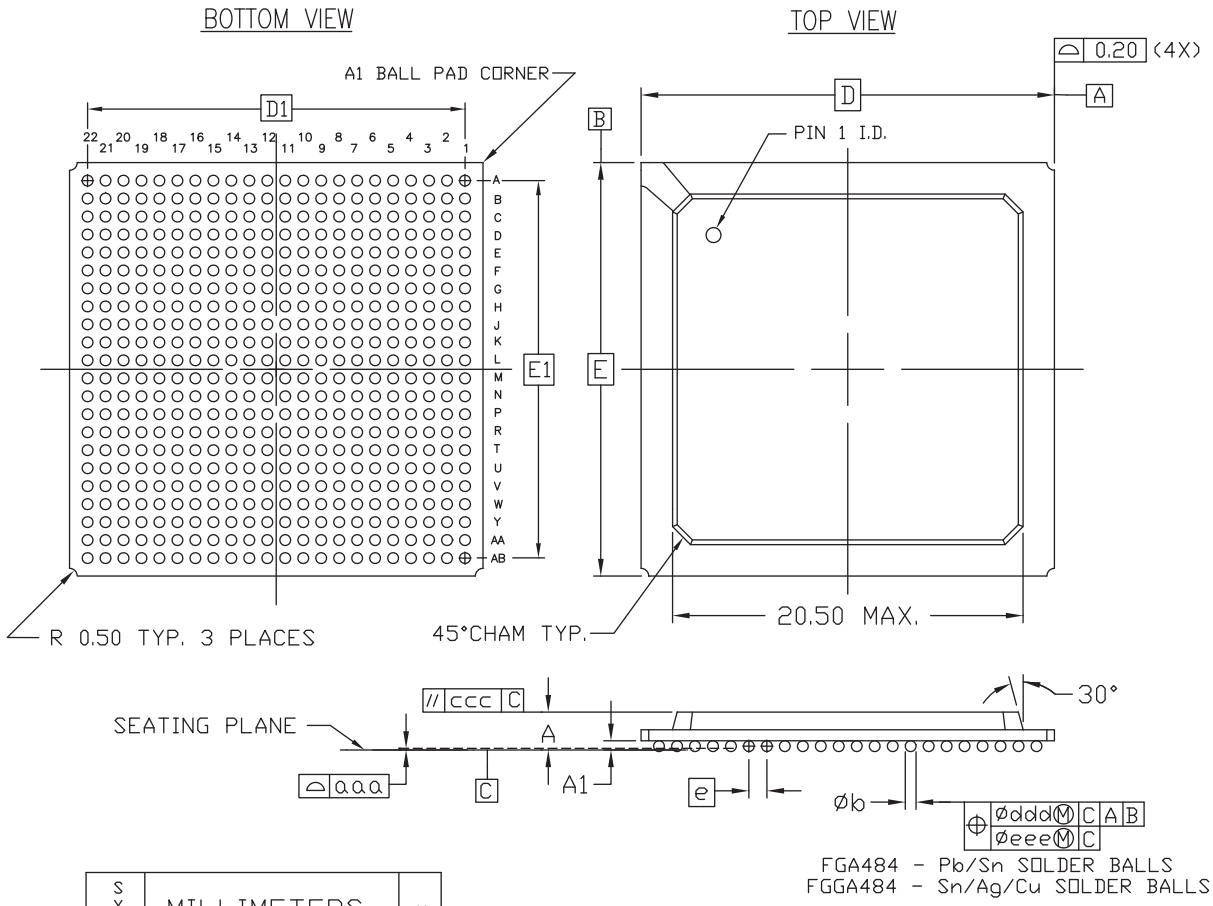
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. ACTUAL SOLDER BALL COUNT IS 324
6. CONFORMS TO JEDEC MO–275–KKAB–1.

ug475_c4_csga324_s7_042617

Figure 4-4: **CSGA324 Wire-Bond Chip-Scale BGA Package Specifications for Spartan-7 FPGAs**

FGGA484 (Spartan-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	2.20	2.44	3
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	22			2

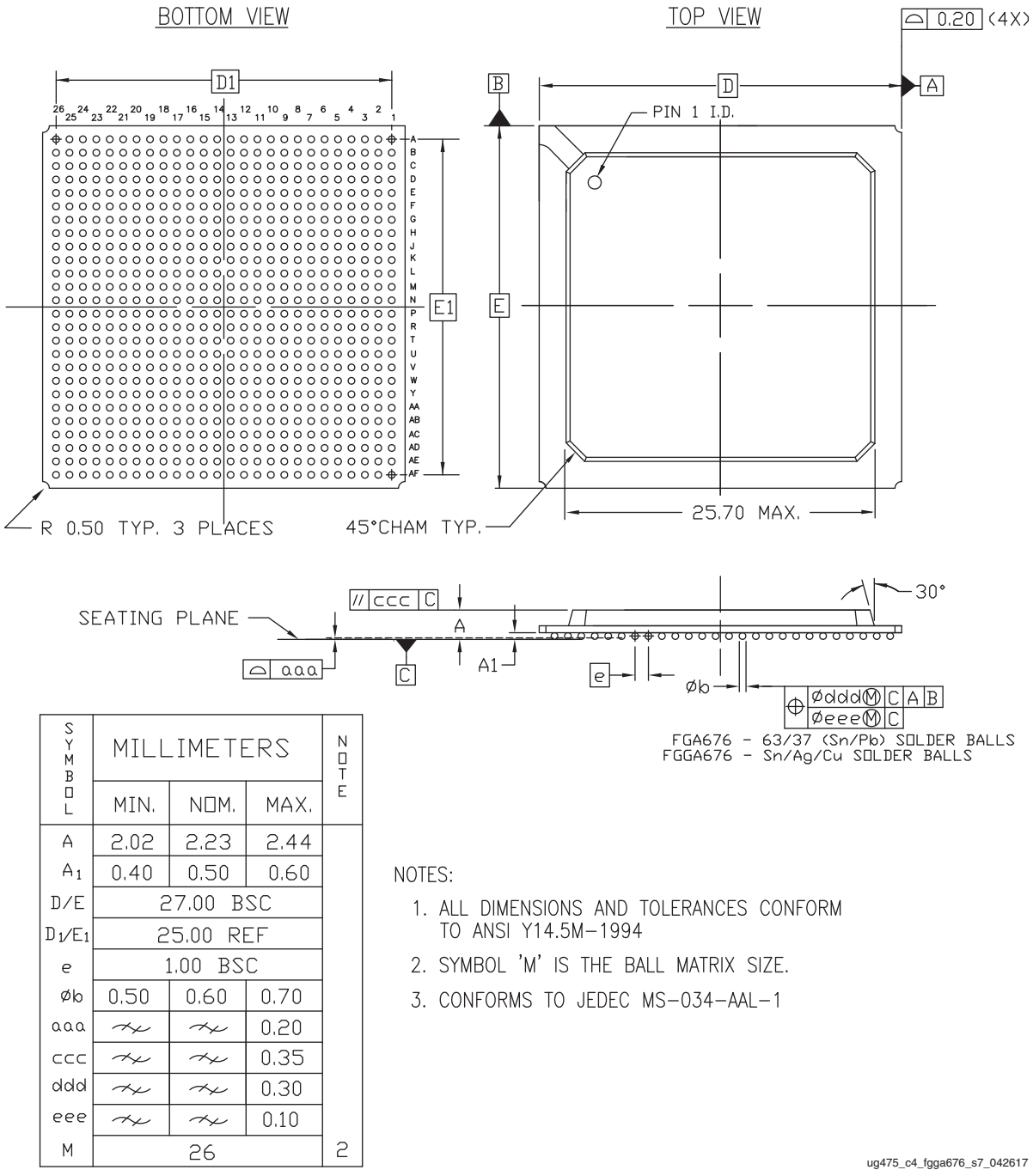
NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAJ–1.

ug475_c4_fgga484_s7_042617

Figure 4-5: **FGGA484 Wire-bond Fine-Pitch BGA Package Specification for Spartan-7 FPGAs**

FGGA676 (Spartan-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.02	2.23	2.44	
A_1	0.40	0.50	0.60	
D/E	27.00 BSC			
D_1/E_1	25.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	26			2

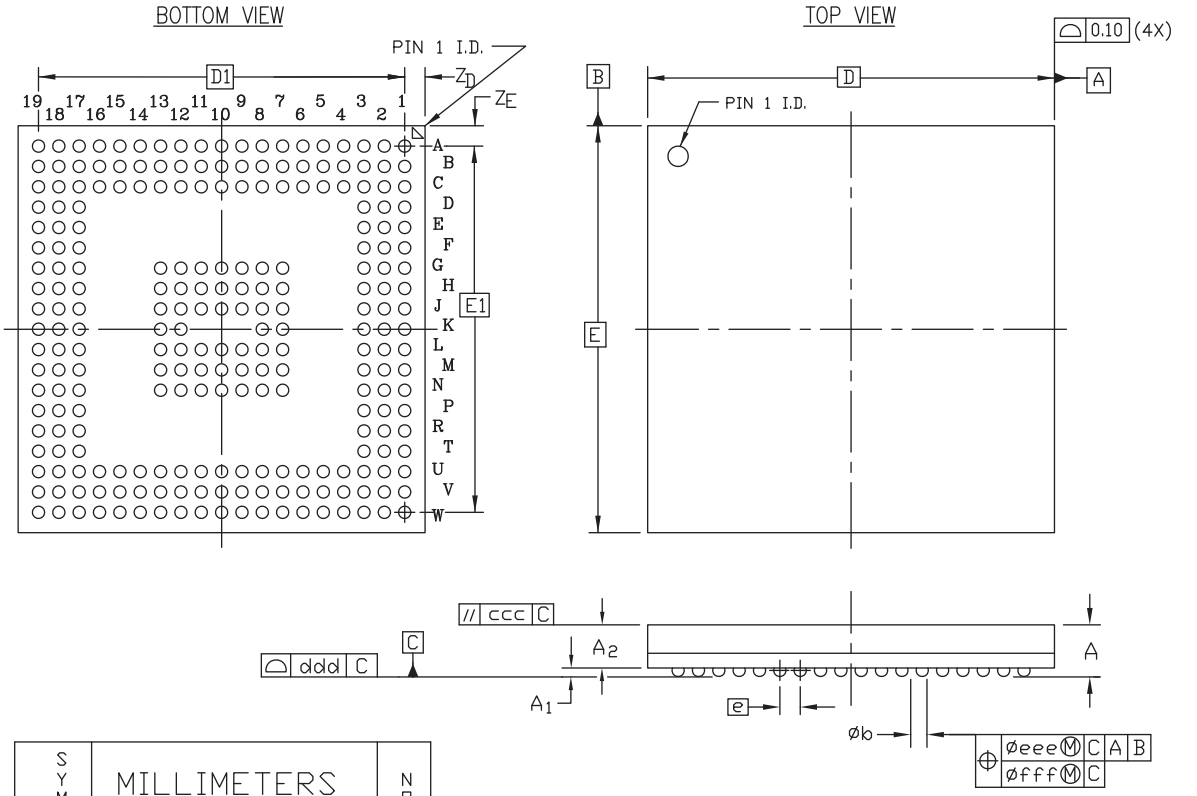
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug475_c4_fgga676_s7_042617

Figure 4-6: **FGGA676 Wire-bond Fine-Pitch BGA Package Specification for Spartan-7 FPGAs**

CP236 and CPG236 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.5 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.18	1.28	1.38	
A_1	0.17	0.22	0.27	
A_2	1.01	1.06	1.11	
D/E	9.90	10.00	10.10	
D_1/E_1	9.00 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc			0.10	
ddd			0.08	
eee			0.15	
fff			0.05	
Z_D/Z_E	0.35	0.50	0.65	
M	19			2

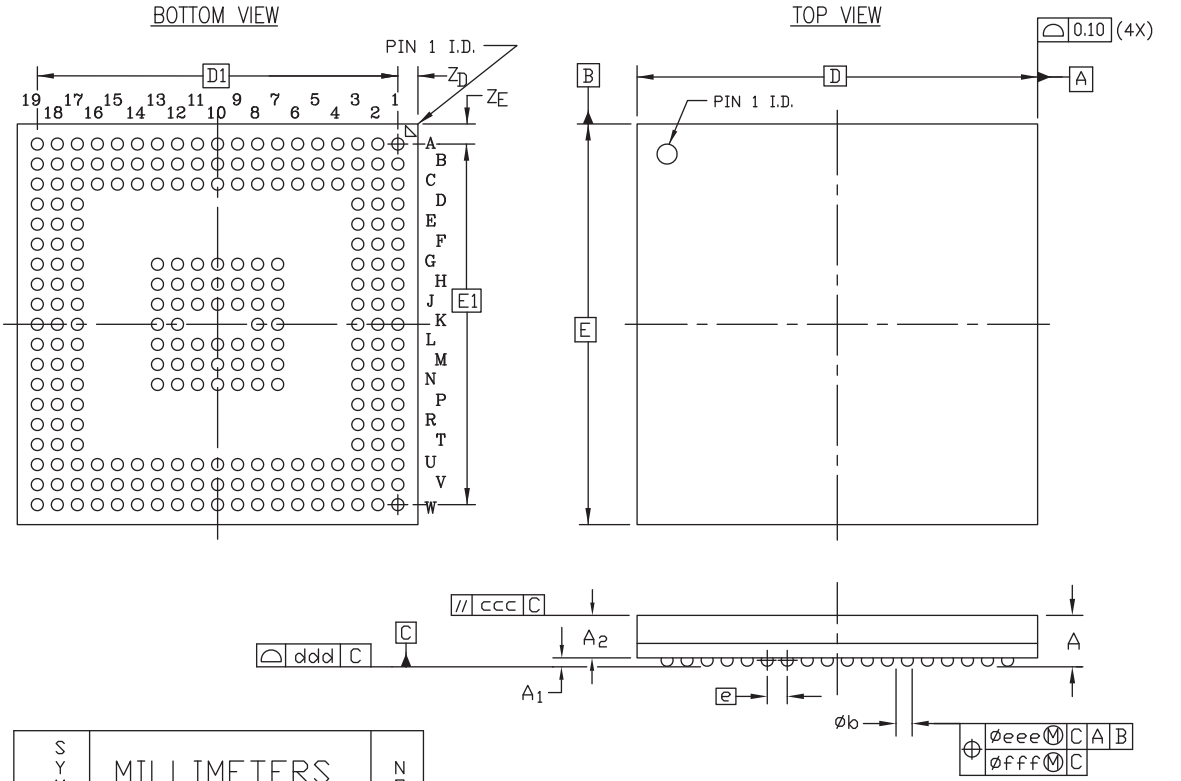
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC MO–275
4. ACTUAL SOLDER BALL COUNT IS 238

ug475_c4_99_071615

Figure 4-7: **CP236 and CPG236 Wire-Bond Chip-Scale BGA Package Specifications for Artix-7 FPGAs**

CPG238 (Artix-7 FPGAs: XC7A12T and XC7A25T) Wire-Bond Chip-Scale BGA (0.5 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	1.18	1.28	1.38	
A_1	0.17	0.22	0.27	
A_2	1.01	1.06	1.11	
D/E	9.90	10.00	10.10	
D_1/E_1	9.00 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc	~	~	0.10	
ddd	~	~	0.08	
eee	~	~	0.15	
fff	~	~	0.05	
Z_D/Z_E	0.35	0.50	0.65	
M	19			2

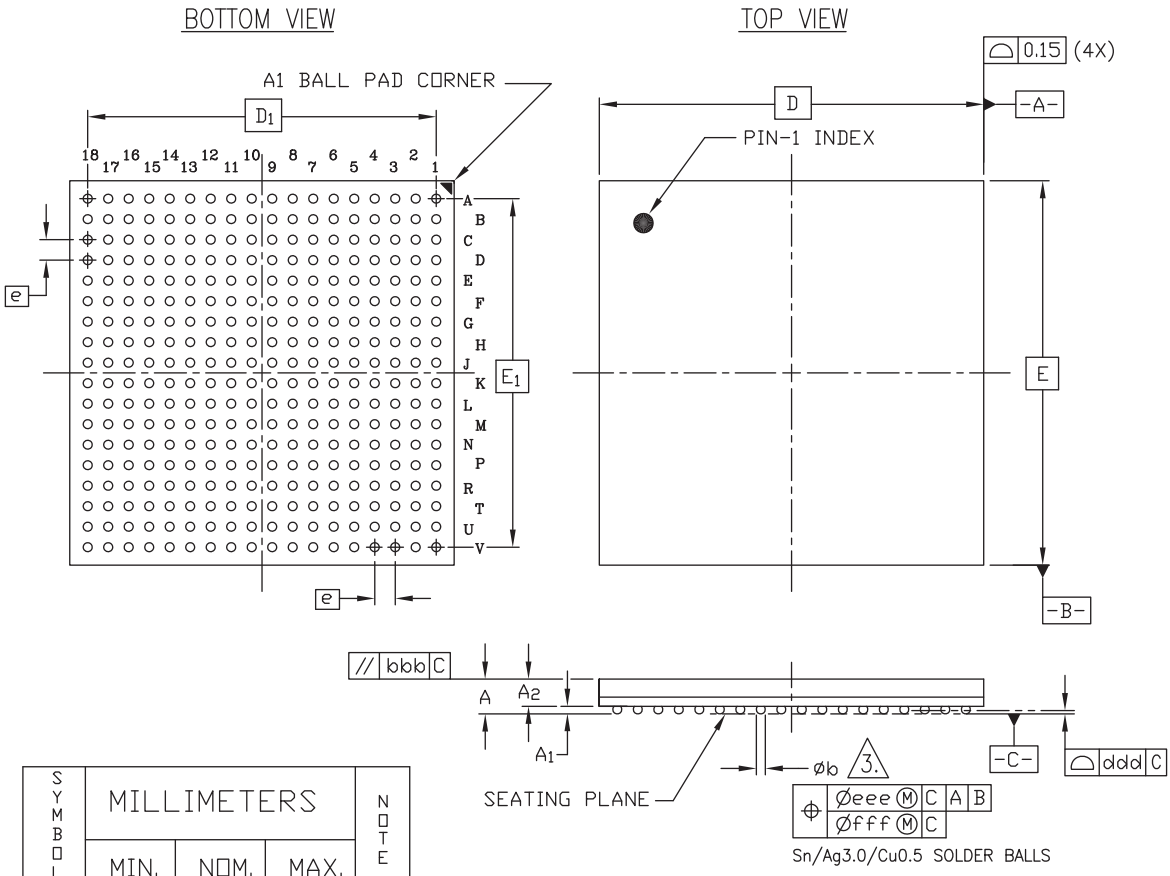
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC MO–275
4. ACTUAL SOLDER BALL COUNT IS 238

ug475_c4_cpg238_s7_061517

Figure 4-8: **CPG238 Wire-Bond Chip-Scale BGA Package Specifications for Artix-7 FPGAs: XC7A12T and XC7A25T**

CS/CSG324 and CS/CSG325 (Artix-7 FPGAs) Wire-Bond Chip-Scale BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			1.50	
A_1	0.25	0.30	0.40	
A_2	1.01	1.06	1.10	
D/E	15.00 BSC			
D_1/E_1	13.60 BSC			
e	0.80 BSC			
øb	0.40	0.45	0.50	3
bbb			0.20	
ddd			0.20	
eee			0.15	
fff			0.08	
M	18			2

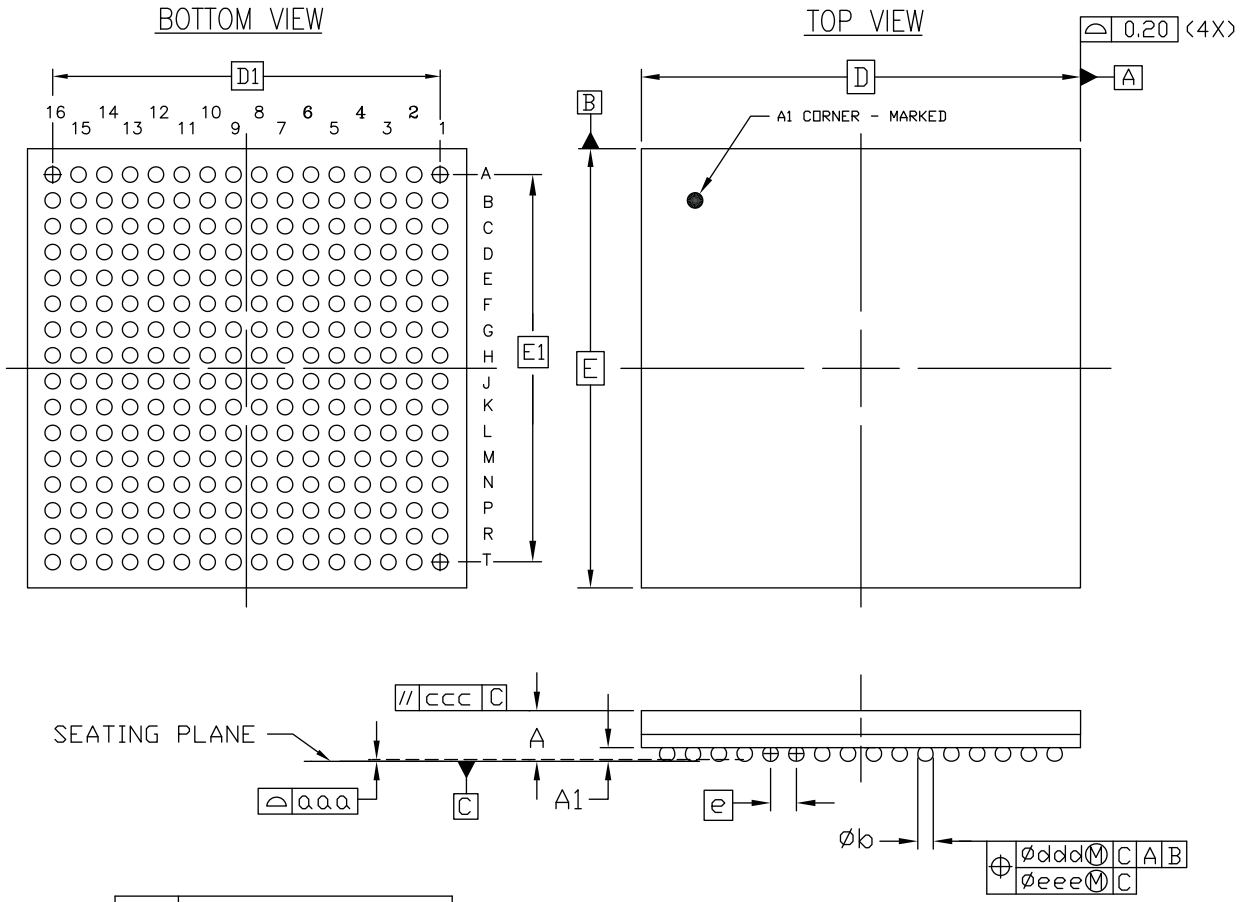
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE
5. CONFORMS TO JEDEC MO–275–KKAB–1

ug475_c4_100_013014

Figure 4-9: **CS/CSG324 and CS/CSG325 Wire-Bond Chip-Scale BGA Package Specifications for Artix-7 FPGAs**

FT/FTG256 (Artix-7 FPGAs) Wire-Bond Fine-Pitch Thin BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		1.40	1.55
A_1	0.30	0.40	0.50
D/E	17.00 BSC		
D_1/E_1	15.00 REF		
e	1.00 BSC		
Øb	0.40	0.50	0.60
aaa			0.15
ccc			0.15
ddd			0.25
eee			0.10
M	16		

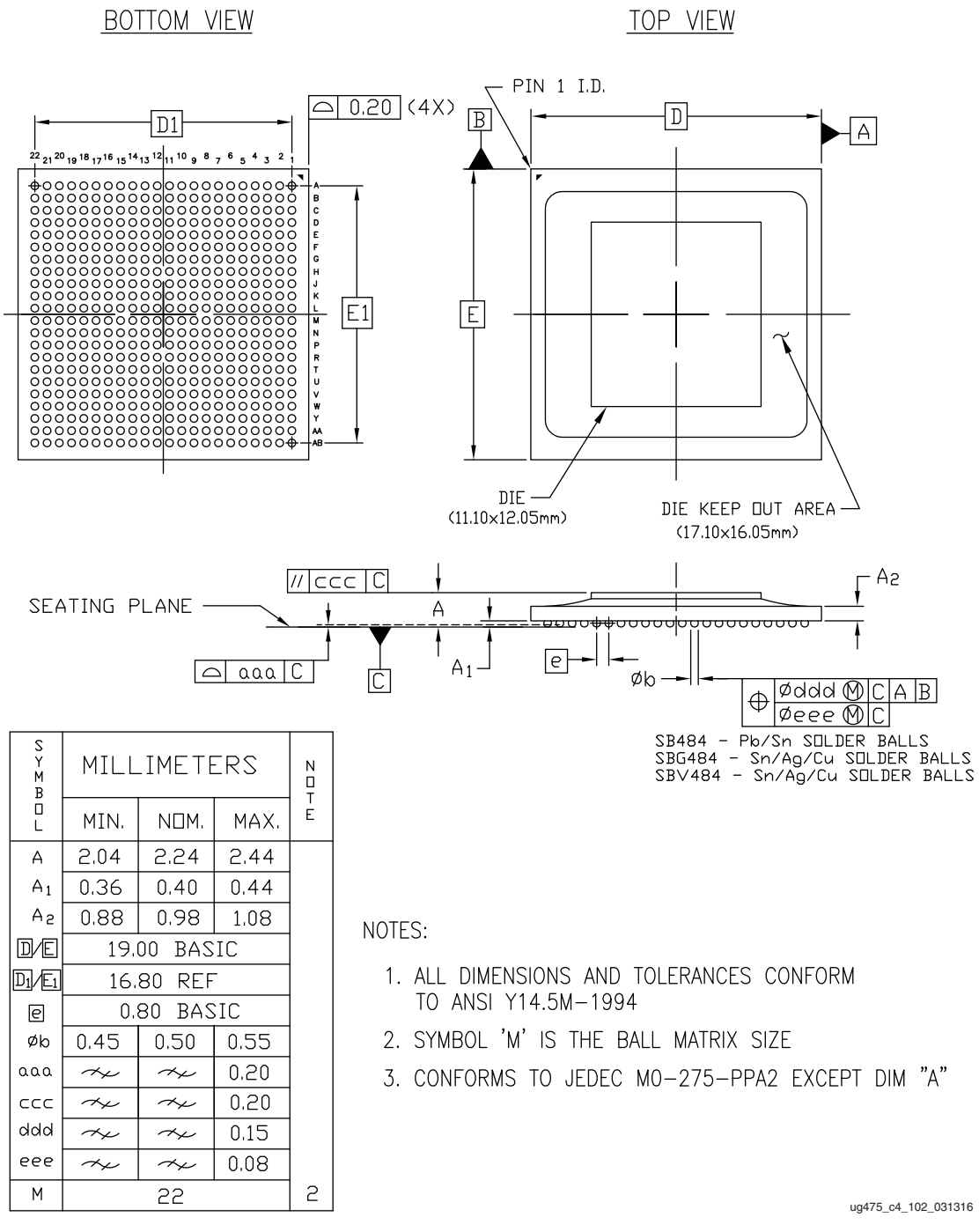
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAF–1 EXCEPT FOR THE SOLDER BALL SIZE.

ug475_c4_101_070516

Figure 4-10: **FT/FTG256 Wire-Bond Fine-Pitch Thin BGA Package Specifications for Artix-7 FPGAs**

SB484, SBG484, and SBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.04	2.24	2.44	
A_1	0.36	0.40	0.44	
A_2	0.88	0.98	1.08	
D/E	19.00 BASIC			
D_1/E_1	16.80 REF			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa	—	—	0.20	
ccc	—	—	0.20	
ddd	—	—	0.15	
eee	—	—	0.08	
M	22			2

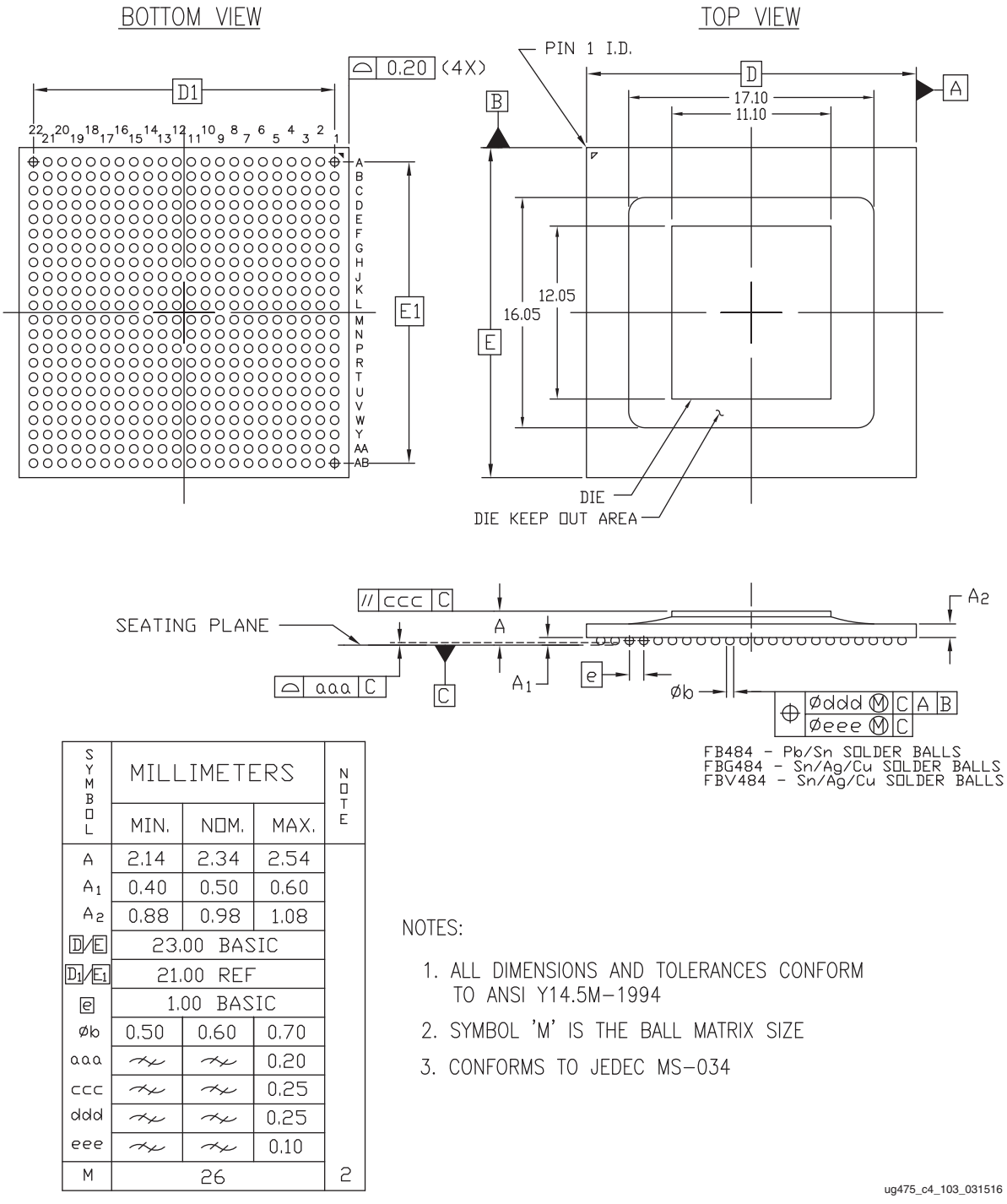
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–275–PPA2 EXCEPT DIM "A"

ug475_c4_102_031316

Figure 4-11: **SB484, SBG484, and SBV484 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs**

FB484, FBG484, and FBV484 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

ug475_c4_103_031516

Figure 4-12: **FB484, FBG484, and FBV484 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs**

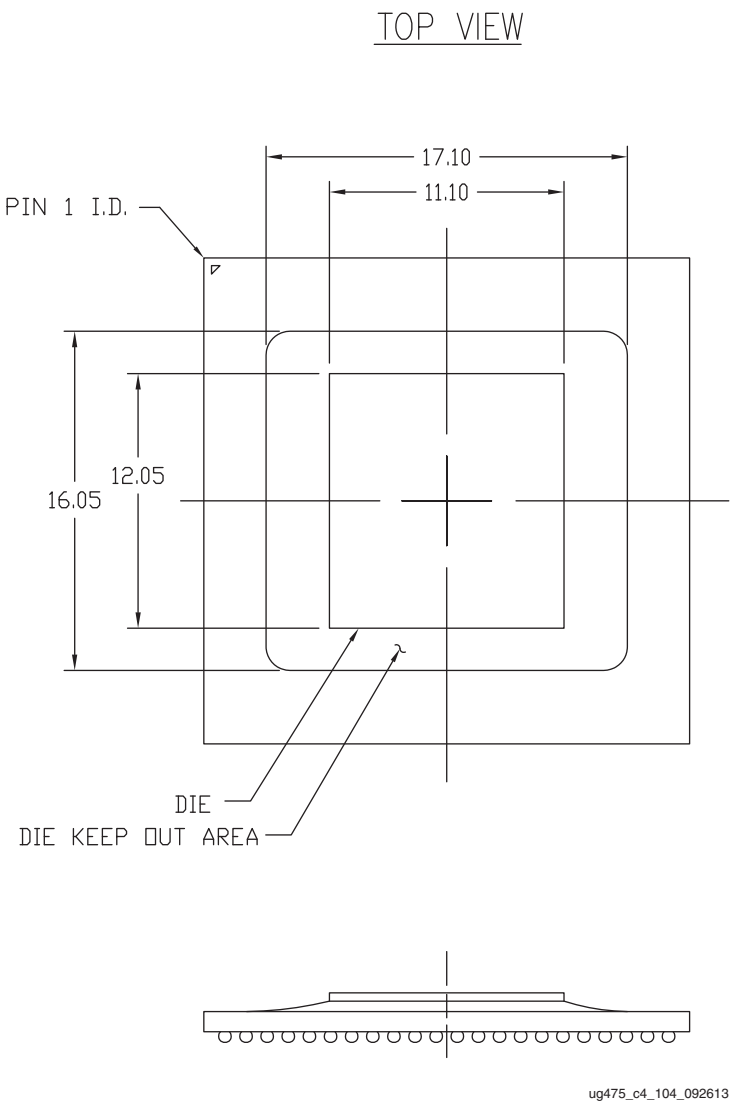
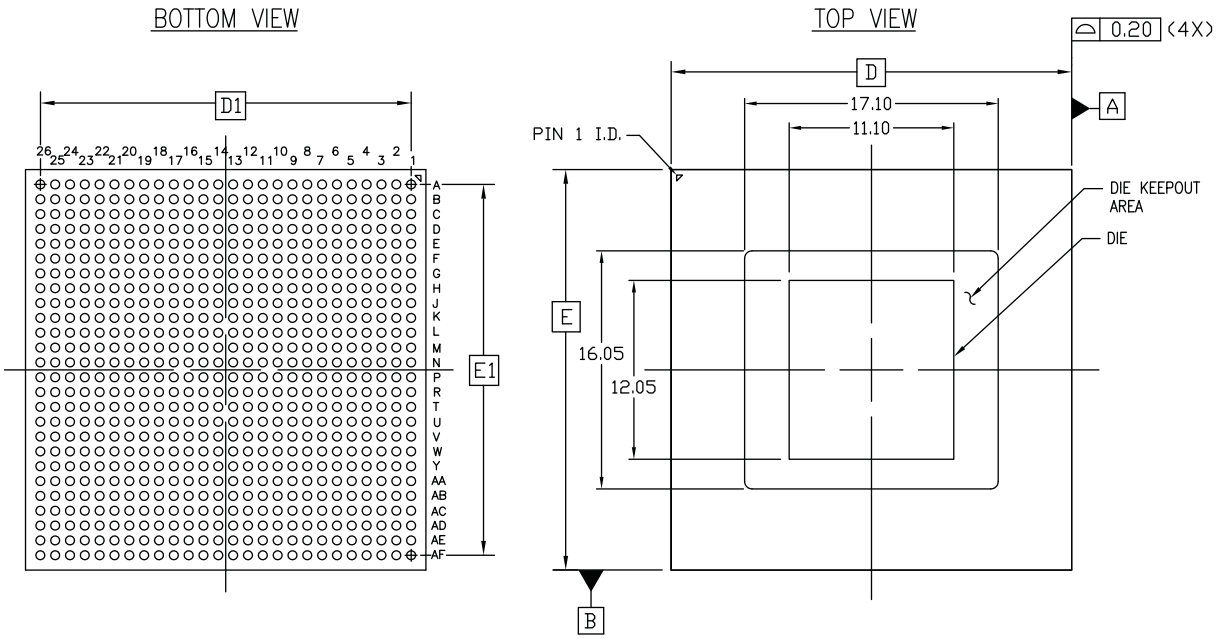


Figure 4-13: **XC7A200T FB484, FBG484, and FBV484 Die Dimensions**

FB676, FBG676, and FBV676 (Artix-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

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Figure 4-14: **FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Artix-7 FPGAs**

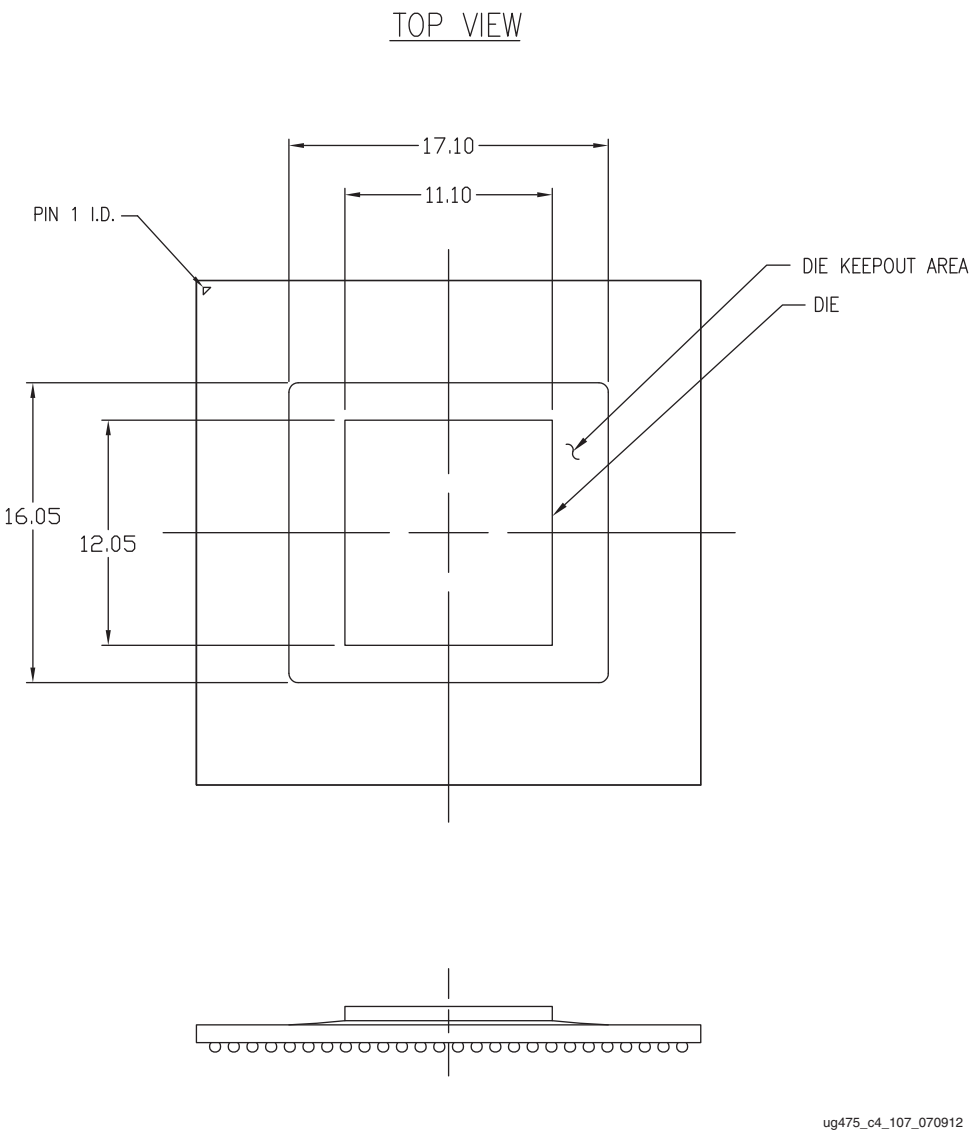
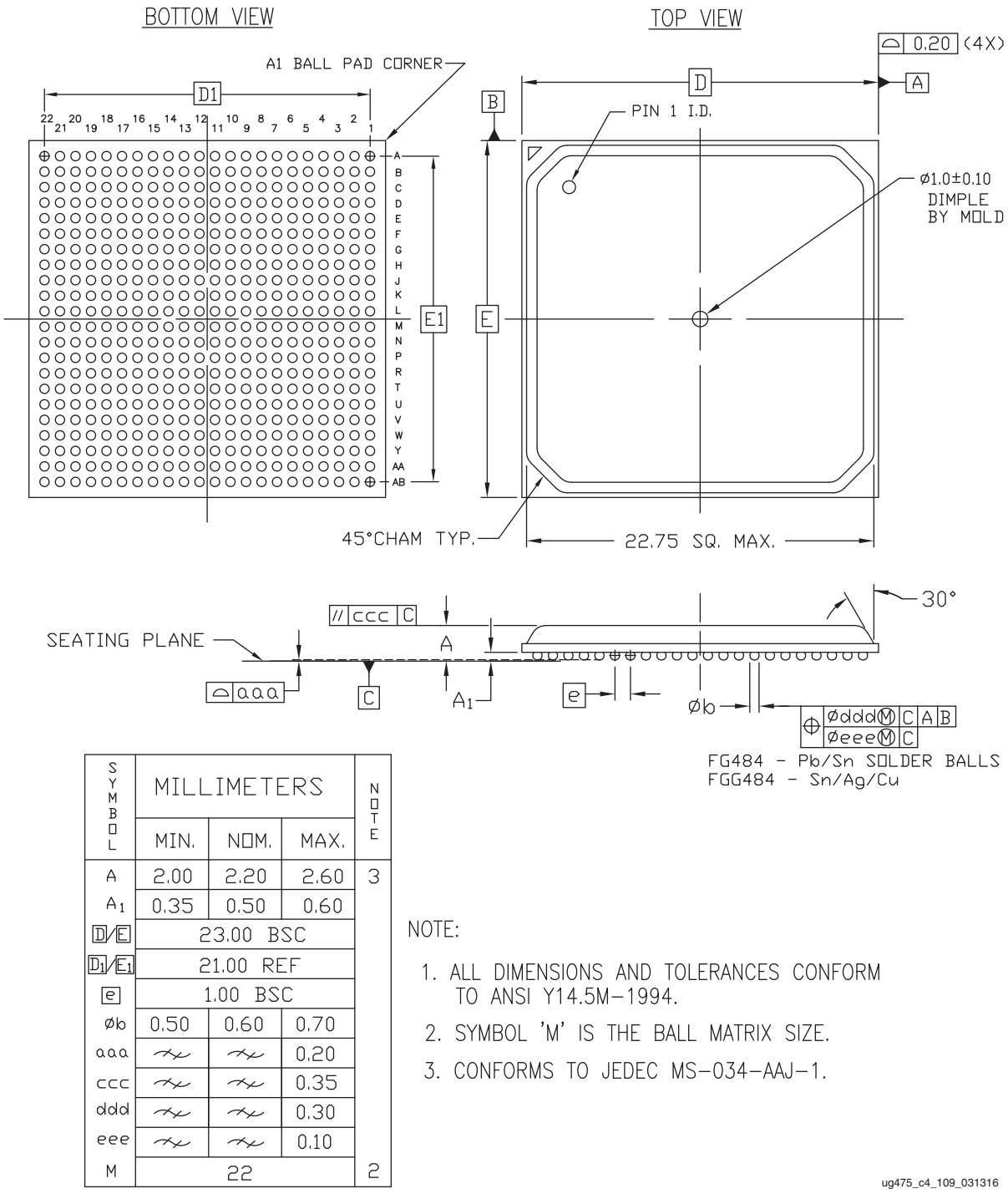


Figure 4-15: **XC7A200T FB676, FBG676, and FBV676 Die Dimensions**

FG484 and FGG484 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.00	2.20	2.60	3
A_1	0.35	0.50	0.60	
D/E	23.00 BSC			
D_1/E_1	21.00 REF			
e	1.00 BSC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	22			2

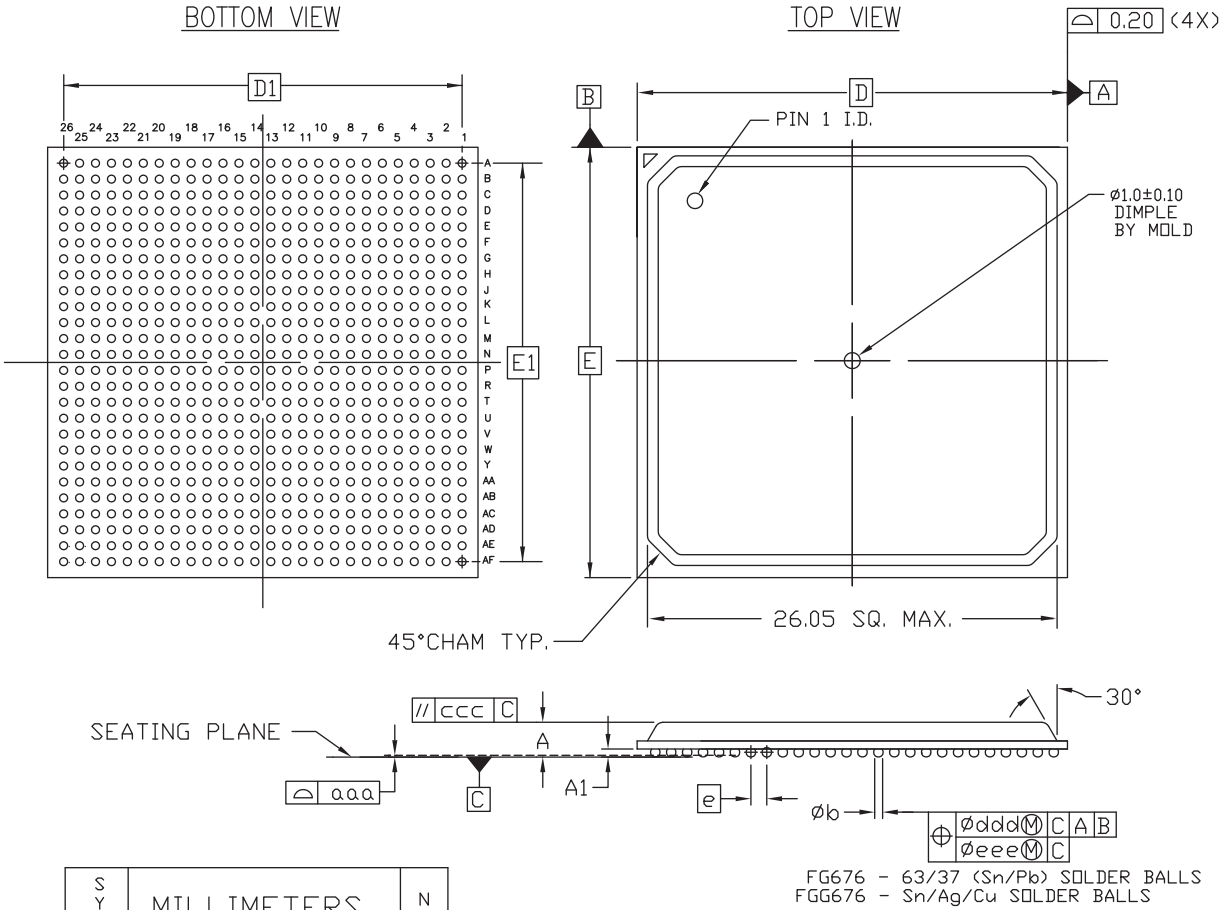
NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAJ–1.

ug475_c4_109_031316

Figure 4-16: **FG484 and FGG484 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs**

FG676 and FGG676 (Artix-7 FPGAs) Wire-Bond Fine-Pitch BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.02	2.23	2.44	
A_1	0.40	0.50	0.60	
D/E	27.00 BSC			
D_1/E_1	25.00 REF			
e	1.00 BSC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	26			2

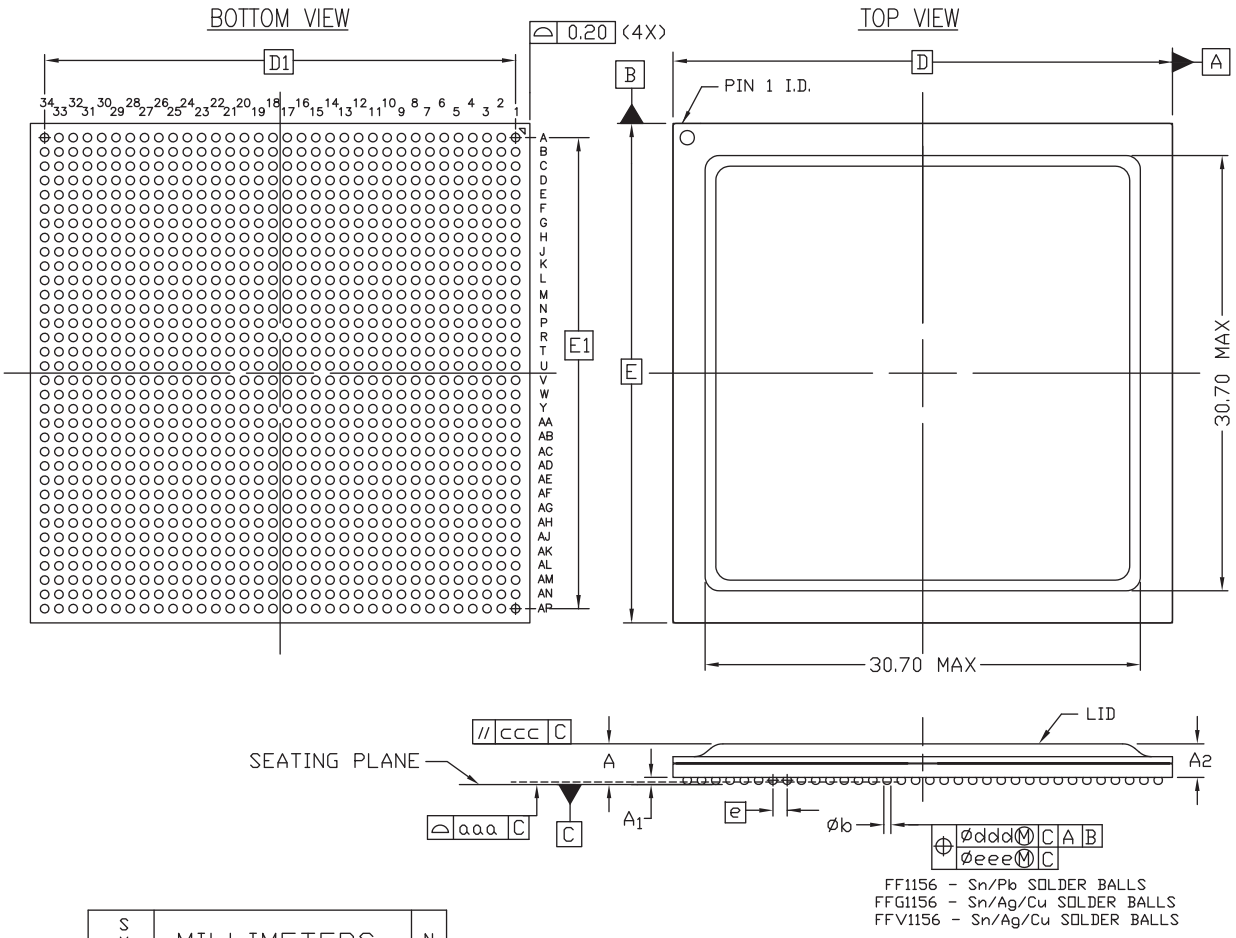
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug475_c4_110_030413

Figure 4-17: **FG676 and FGG676 Wire-bond Fine-Pitch BGA Package Specification for Artix-7 FPGAs**

FF1156, FFG1156, and FFV1156 (Artix-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70	2.90	3.10	
A_1	0.40	0.50	0.60	
A_2	2.30	2.40	2.50	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

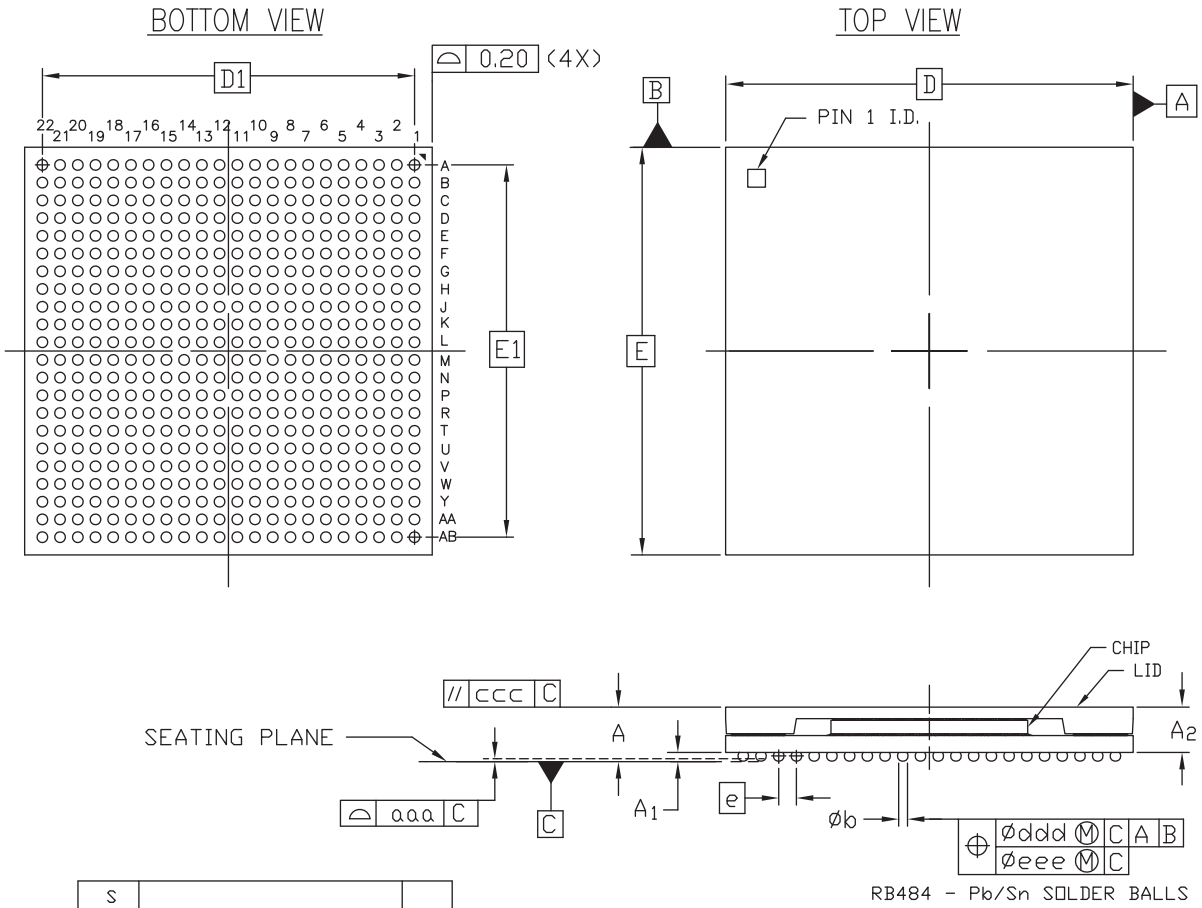
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156
5. THIS PACKAGE IS USED FOR ARTIX®–7 FPGAs REFER TO PK384 FOR THE MECHANICAL DRAWING OF FF1156 PACKAGE USED FOR VIRTEX®–5 FPGAS AND PK401 FOR VIRTEX®–6 FPGAS

ug475_c4_111_070516

Figure 4-18: **FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Artix-7 FPGAs**

RB484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch)



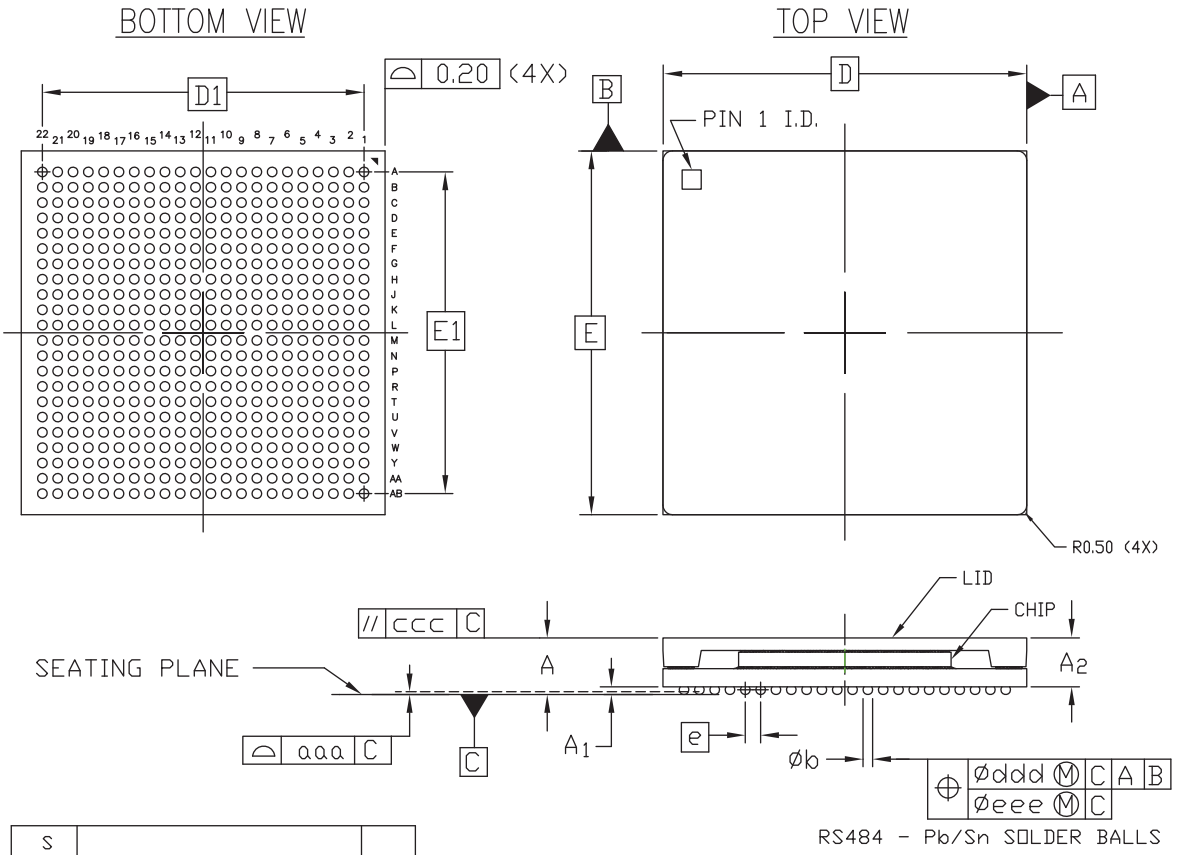
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.75	3.05	3.35	
A_1	0.40	0.50	0.60	
A_2	2.35	2.55	2.75	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	22			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

Figure 4-19: **RB484 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs**

RS484 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (0.8 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.71	2.95	3.19	
A_1	0.36	0.40	0.44	
A_2	2.35	2.55	2.75	
D/E	19.00 BASIC			
D_1/E_1	16.80 REF			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa			0.20	
ccc			0.20	
ddd			0.15	
eee			0.08	
M	22			2

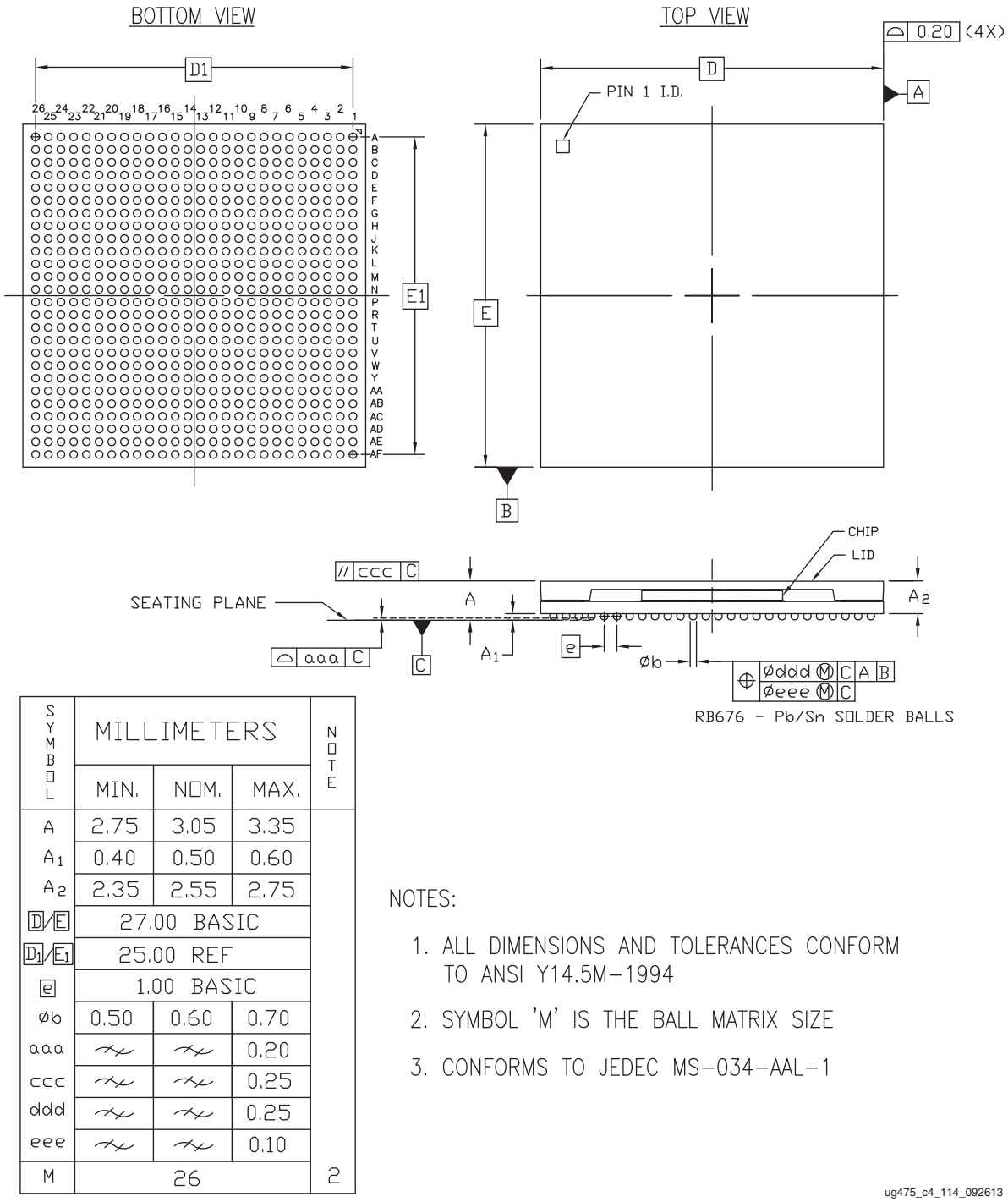
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–275–PPA2 EXCEPT DIM "A"

ug475_c4_113_070516

Figure 4-20: **RS484 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs**

RB676 (Artix-7 FPGAs) Ruggedized Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.75	3.05	3.35	
A_1	0.40	0.50	0.60	
A_2	2.35	2.55	2.75	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

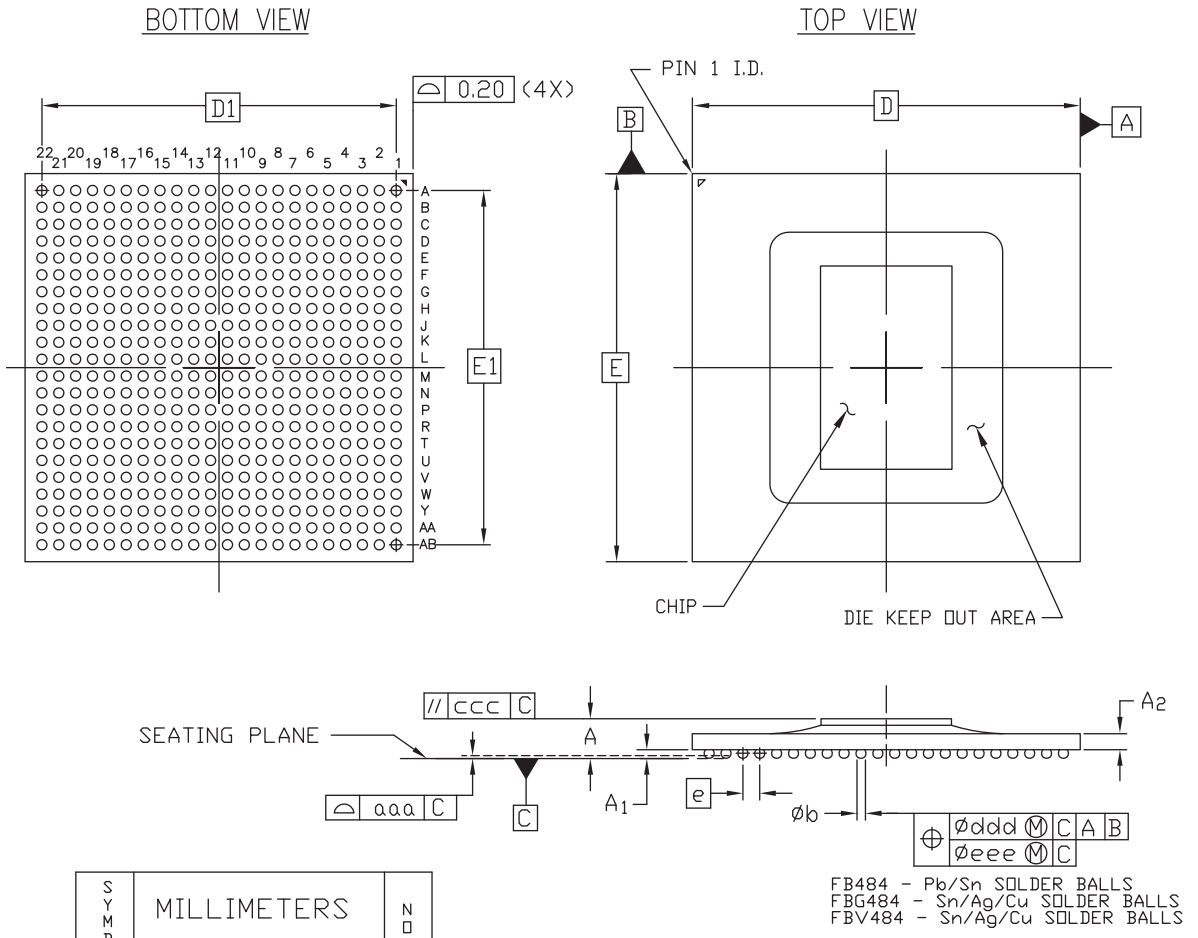
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAL–1

ug475_c4_114_092613

Figure 4-21: **RB676 Ruggedized Flip-Chip BGA Package Specifications for Artix-7 FPGAs**

FB484, FBG484, and FBV484 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.83	0.98	1.13	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE AND CHIP CAPACITOR LOCATION

ug475_c4_01_031516

Figure 4-22: **FB484, FBG484, and FBV484 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**

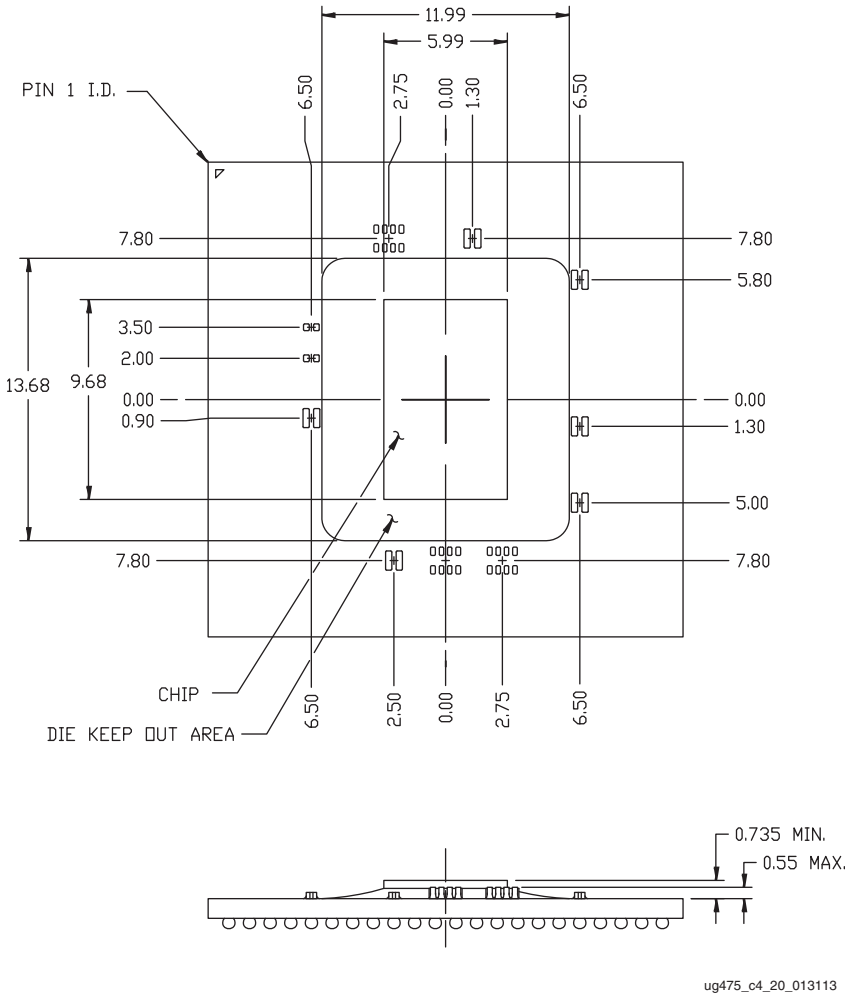


Figure 4-23: **XC7K70T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations**

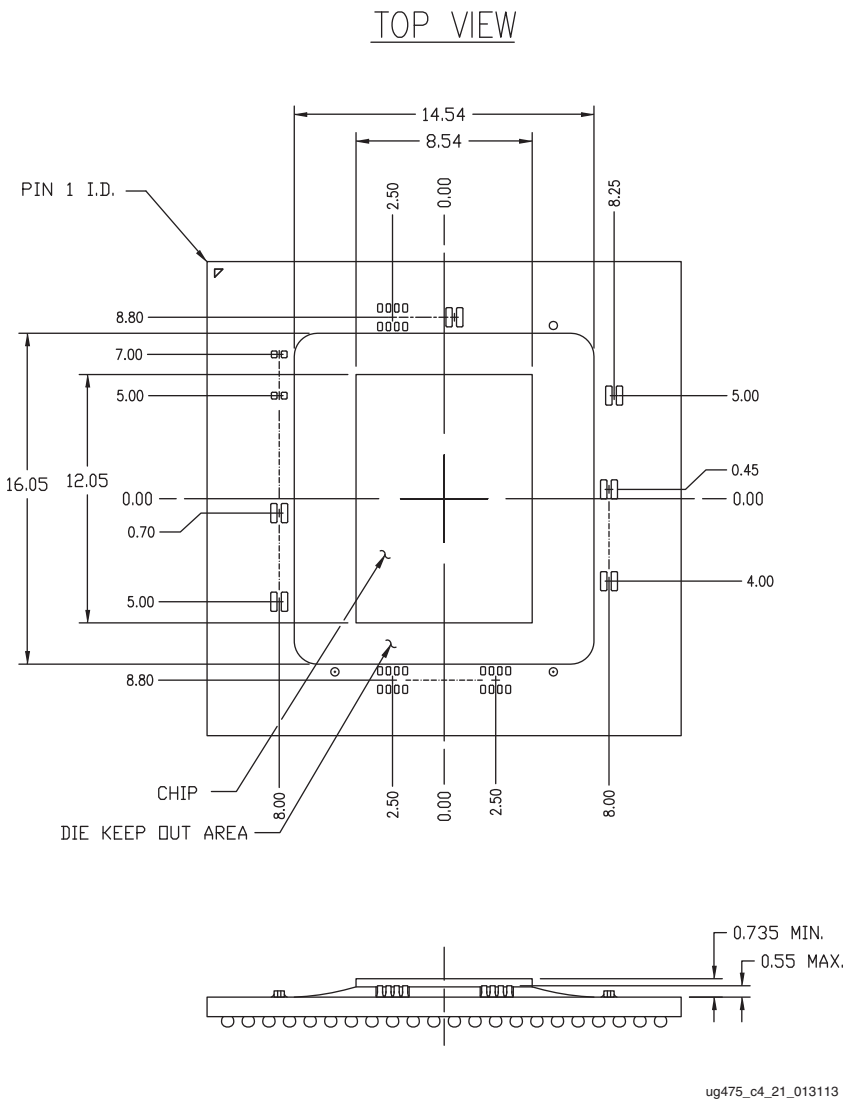
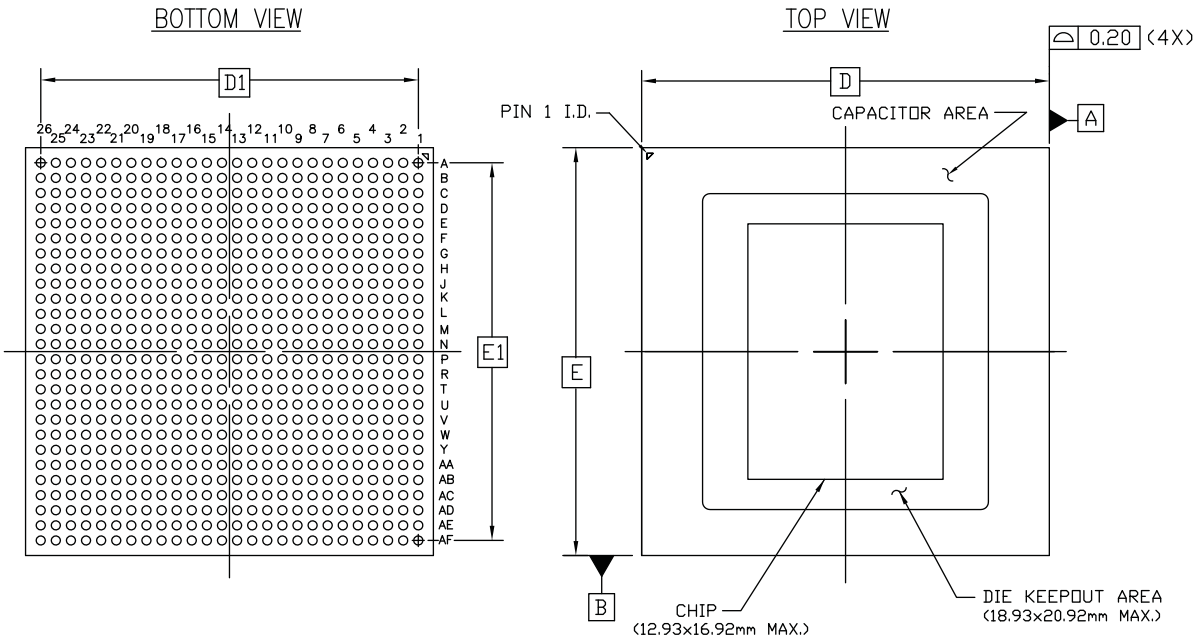


Figure 4-24: **XC7K160T FB484, FBG484, and FBV484 Die Dimensions with Capacitor Locations**

FB676, FBG676, and FBV676 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034
4. SEE FOLLOWING PAGES FOR SPECIFIC DIE SIZE AND CHIP CAPACITOR LOCATION

ug475_c4_02_070516

Figure 4-25: **FB676, FBG676, and FBV676 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**

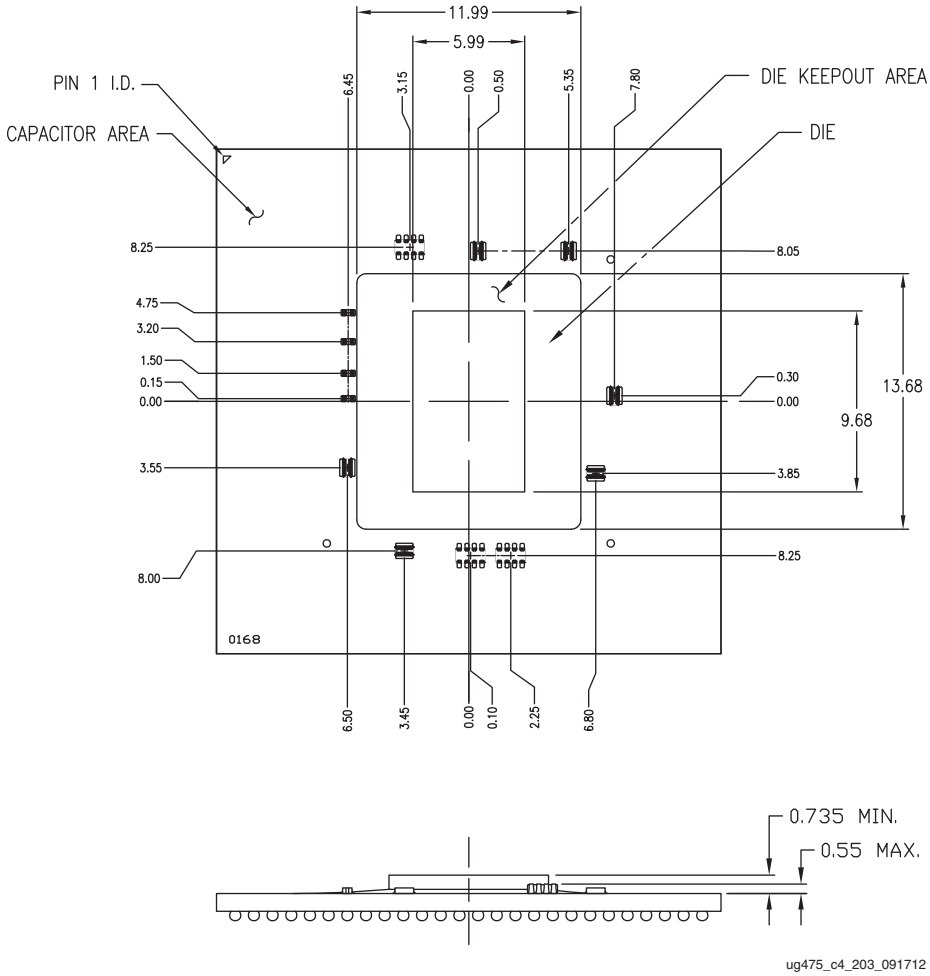


Figure 4-26: **XC7K70T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations**

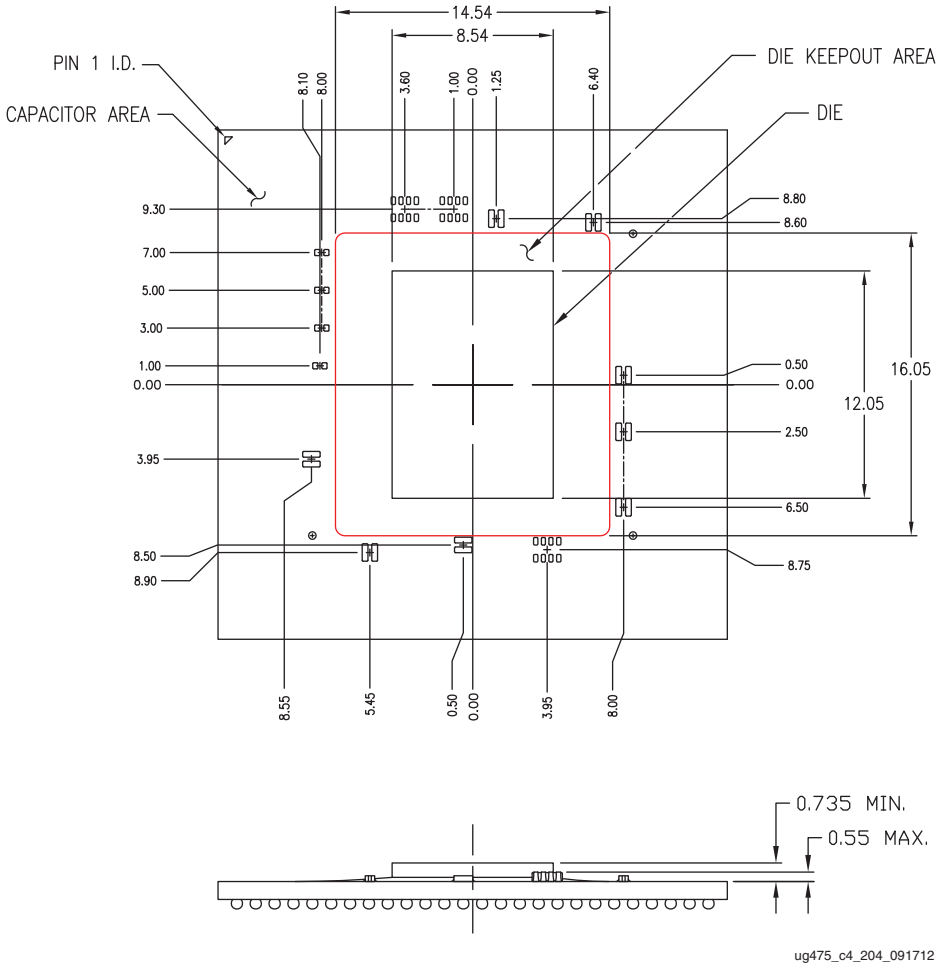


Figure 4-27: **XC7K160T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations**

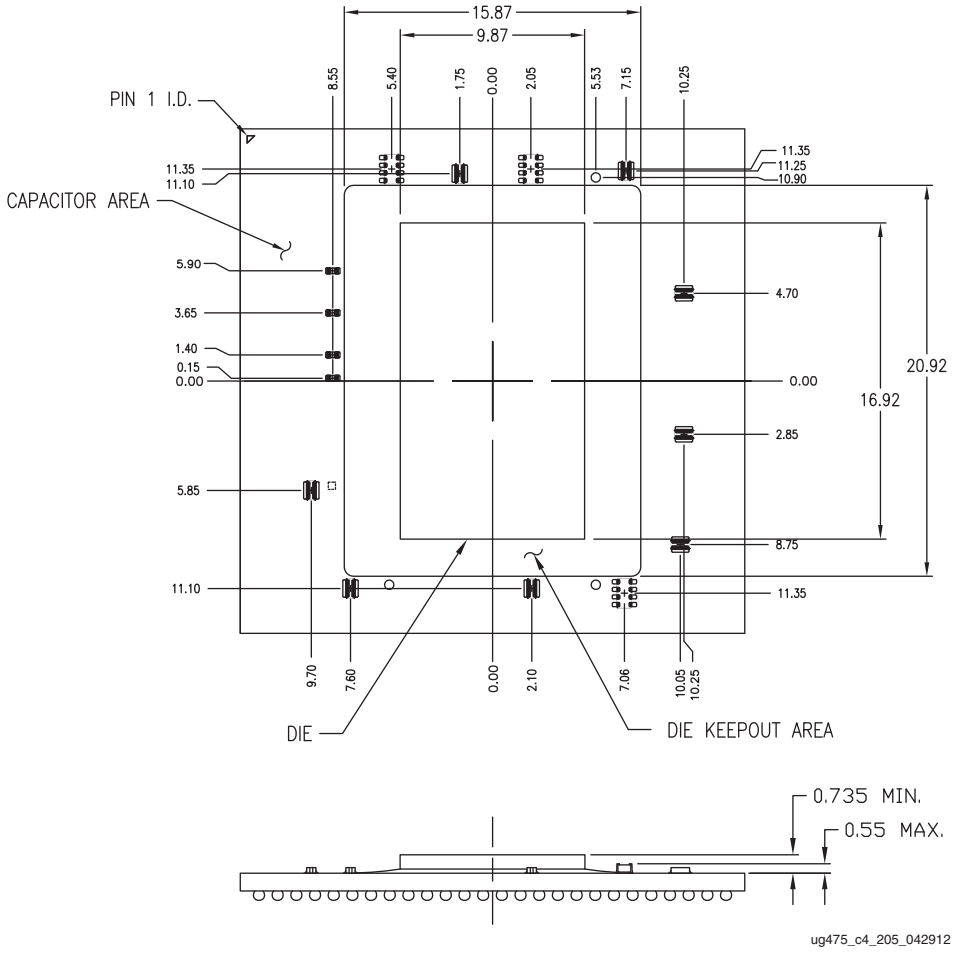


Figure 4-28: **XC7K325T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations**

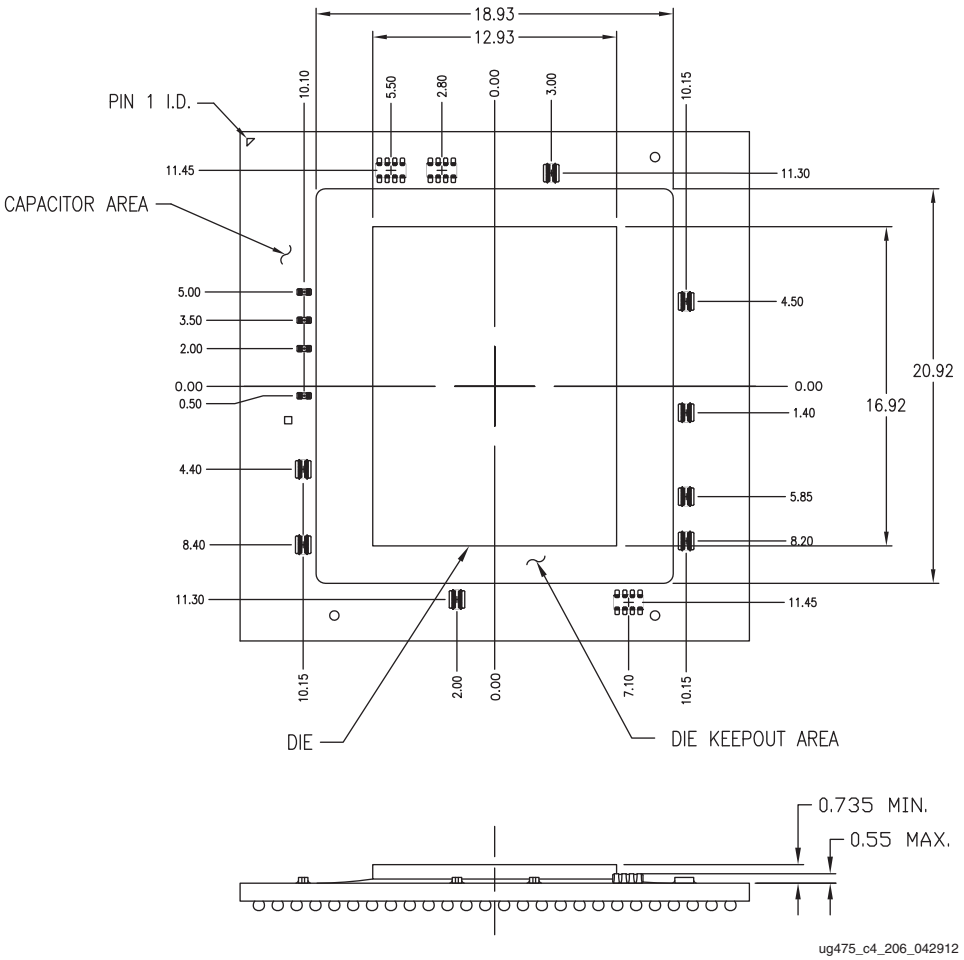
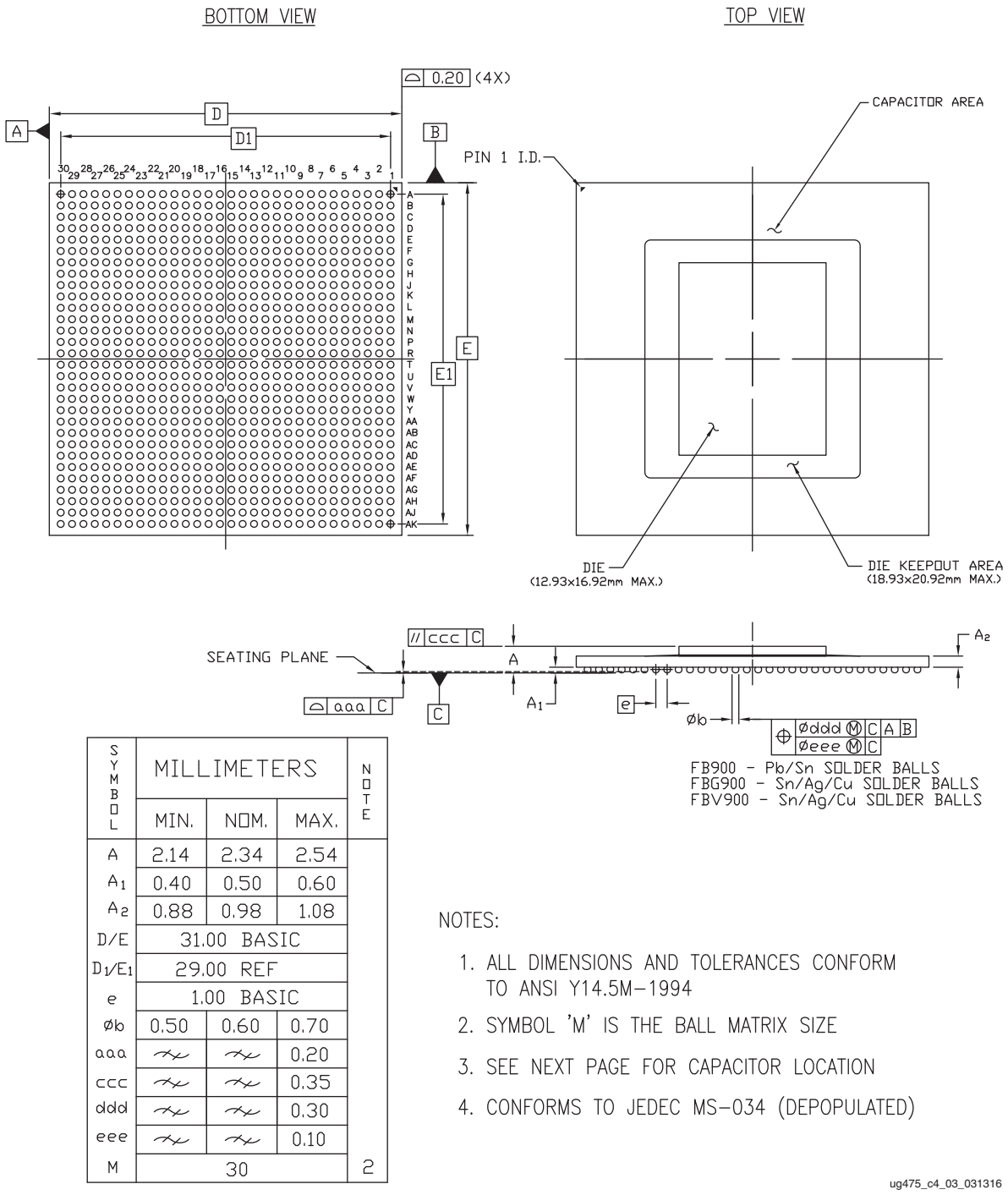


Figure 4-29: **XC7K410T FB676, FBG676, and FBV676 Die Dimensions with Capacitor Locations**

FB900, FBG900, and FBV900 (Kintex-7 FPGAs) Flip-Chip Lidless BGA (1.0 mm Pitch)



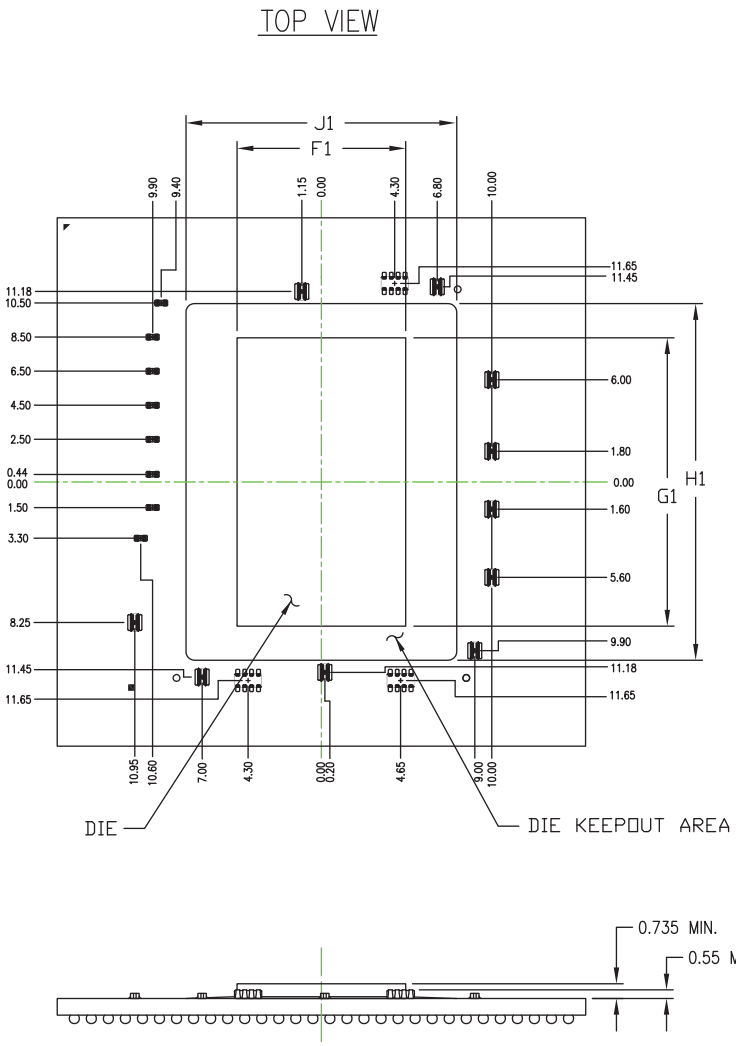
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. SEE NEXT PAGE FOR CAPACITOR LOCATION
4. CONFORMS TO JEDEC MS–034 (DEPOPULATED)

ug475_c4_03_031316

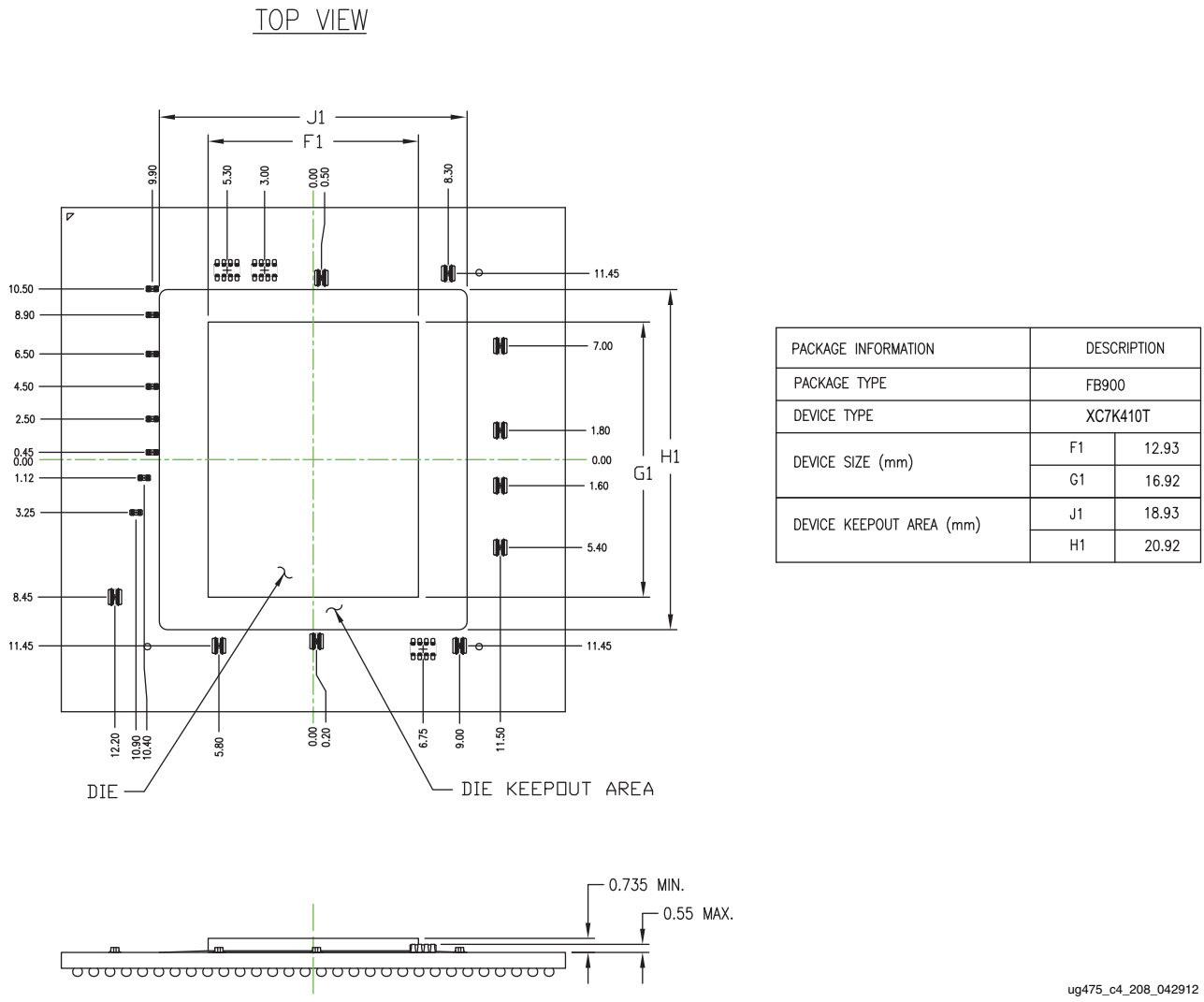
Figure 4-30: **FB900, FBG900, and FBV900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K325T	
DEVICE SIZE (mm)	F1	9.89
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	15.89
	H1	20.92

ug475_c4_207_042912

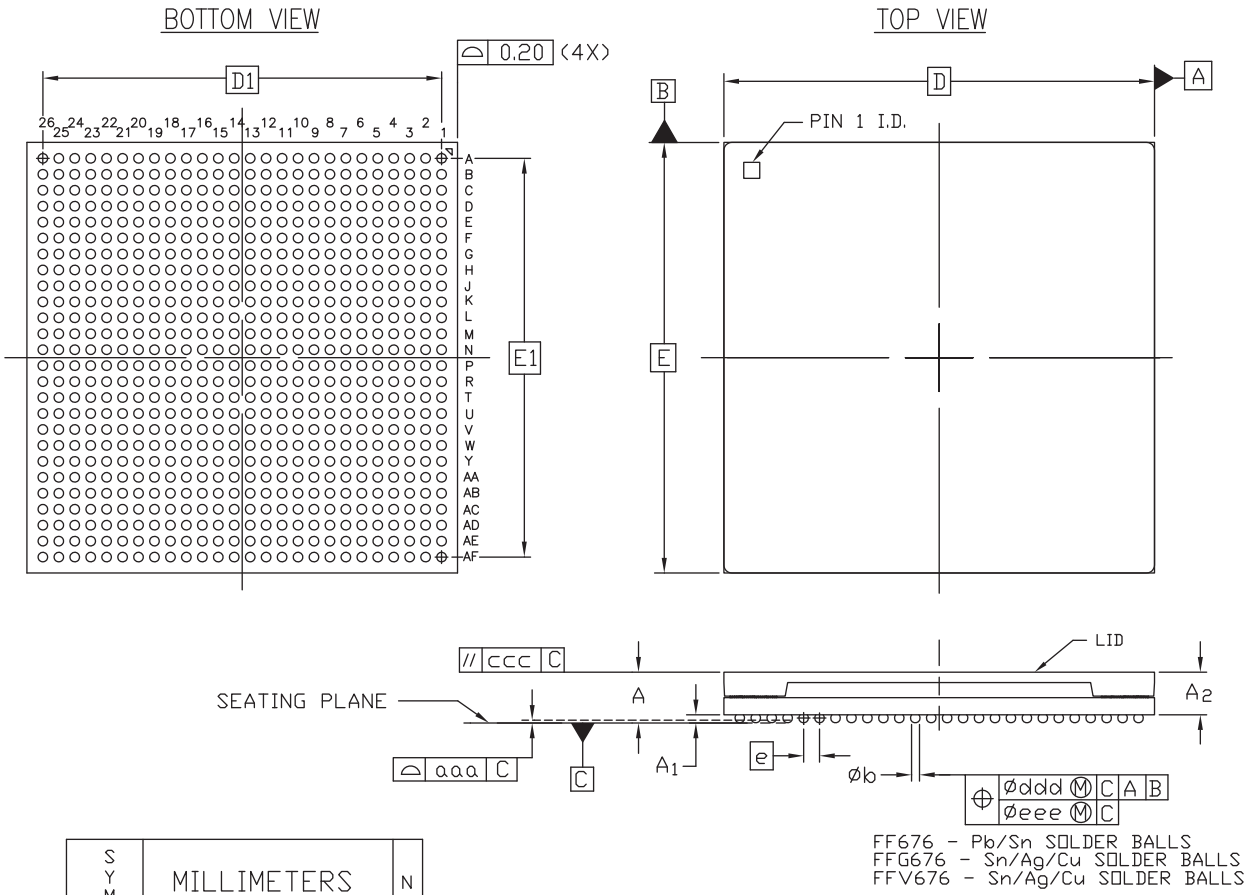
Figure 4-31: **XC7K325T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K410T	
DEVICE SIZE (mm)	F1	12.93
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	18.93
	H1	20.92

Figure 4-32: **XC7K410T FB900, FBG900, and FBV900 Die Dimensions with Capacitor Locations**

FF676, FFG676, and FFV676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.97	3.17	3.37	
A_1	0.40	0.50	0.60	
A_2	2.57	~	2.77	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

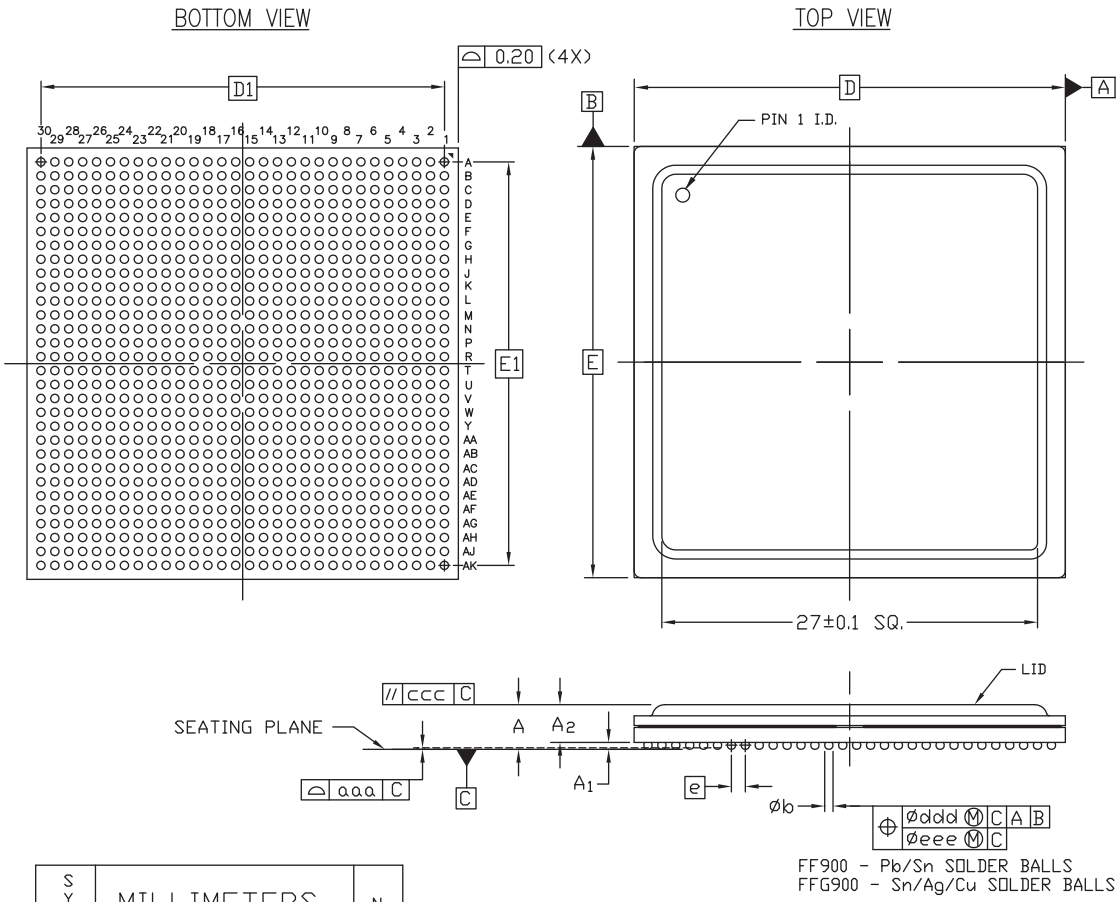
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug475_c4_04_070516

Figure 4-33: **FF676, FFG676, and FFV676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

FF900 and FFG900 (XC7K325T and XC7K410T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	3.15	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~~	2.75	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	30			2

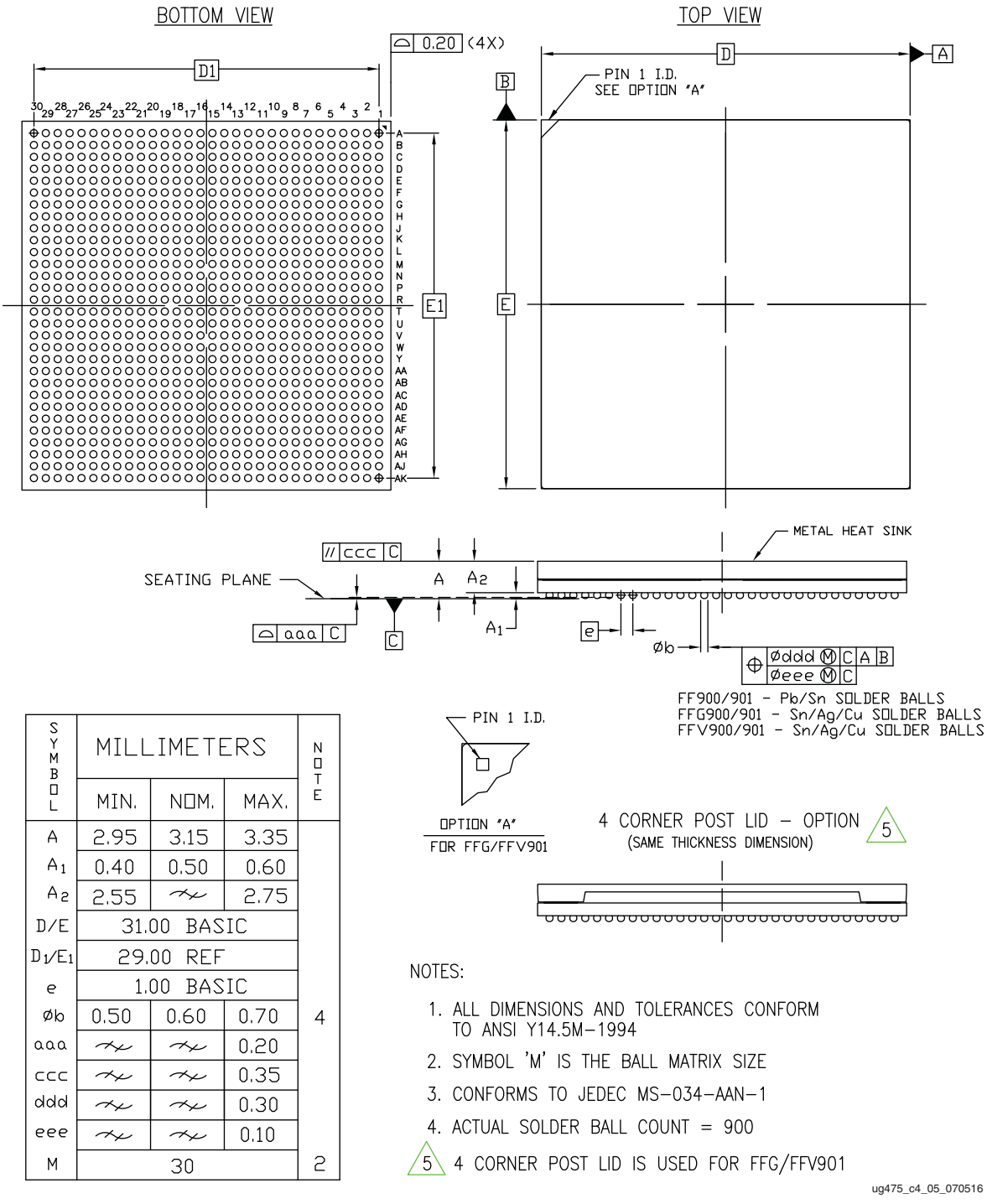
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAN–1
4. ACTUAL SOLDER BALL COUNT = 900

ug475_c4_ffg900_k7_020818

Figure 4-34: **FF900 and FFG900 (XC7K325T an XC7K410T) Flip-Chip BGA Package Specifications**

FF900, FFG900, FFV900, FF901, FFG901, and FFV901 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	3.15	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~~	2.75	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	30			2

NOTES:

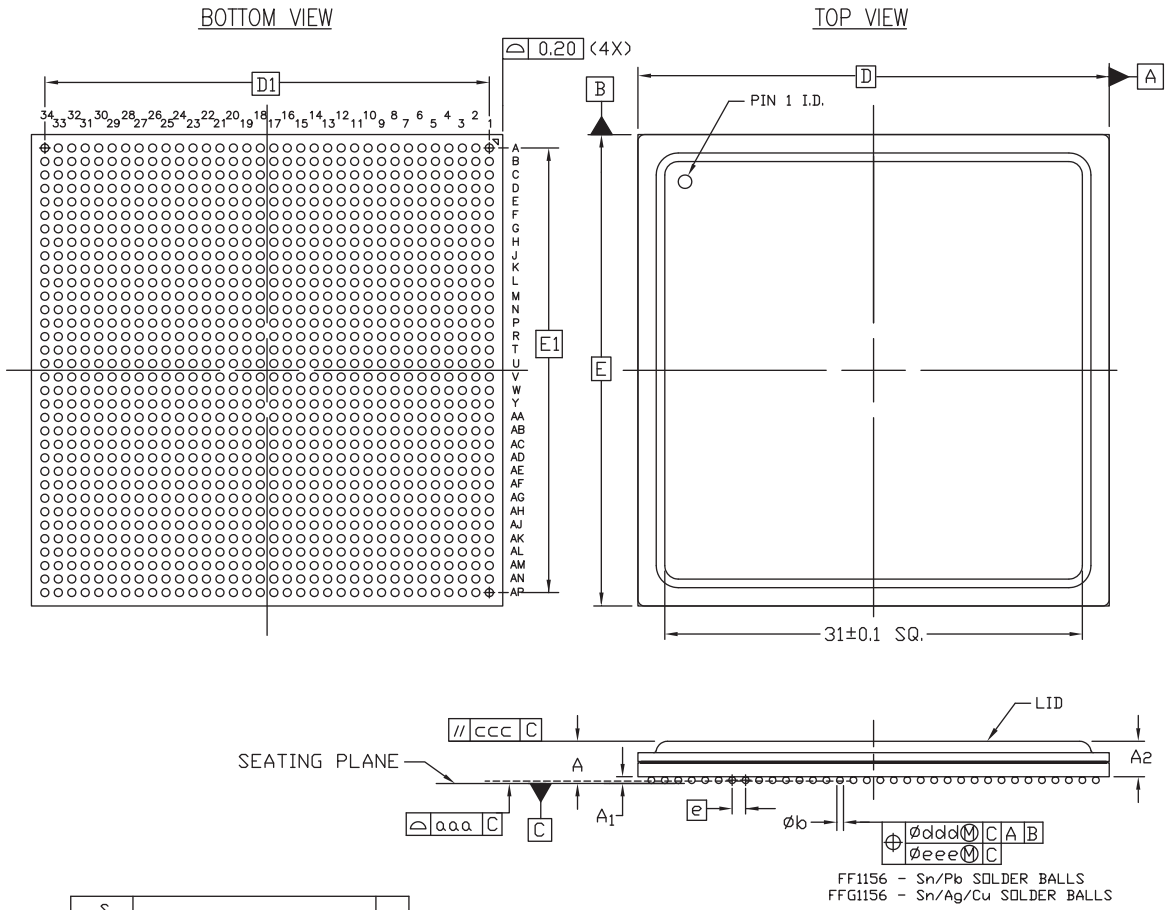
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAN–1
4. ACTUAL SOLDER BALL COUNT = 900

5 4 CORNER POST LID IS USED FOR FFG/FFV901

ug475_c4_05_070516

Figure 4-35: **FF900, FFG900, FFV900, FF901, FFG901, and FFV901 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

FF1156 and FFG1156 (XC7K420T and XC7K480T) Flip-Chip BGA (1.0 mm Pitch) with Stamped Lid



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	3.15	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	2.65	2.75	
D/E	35.00 BASIC			
D_1/E_1	33.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

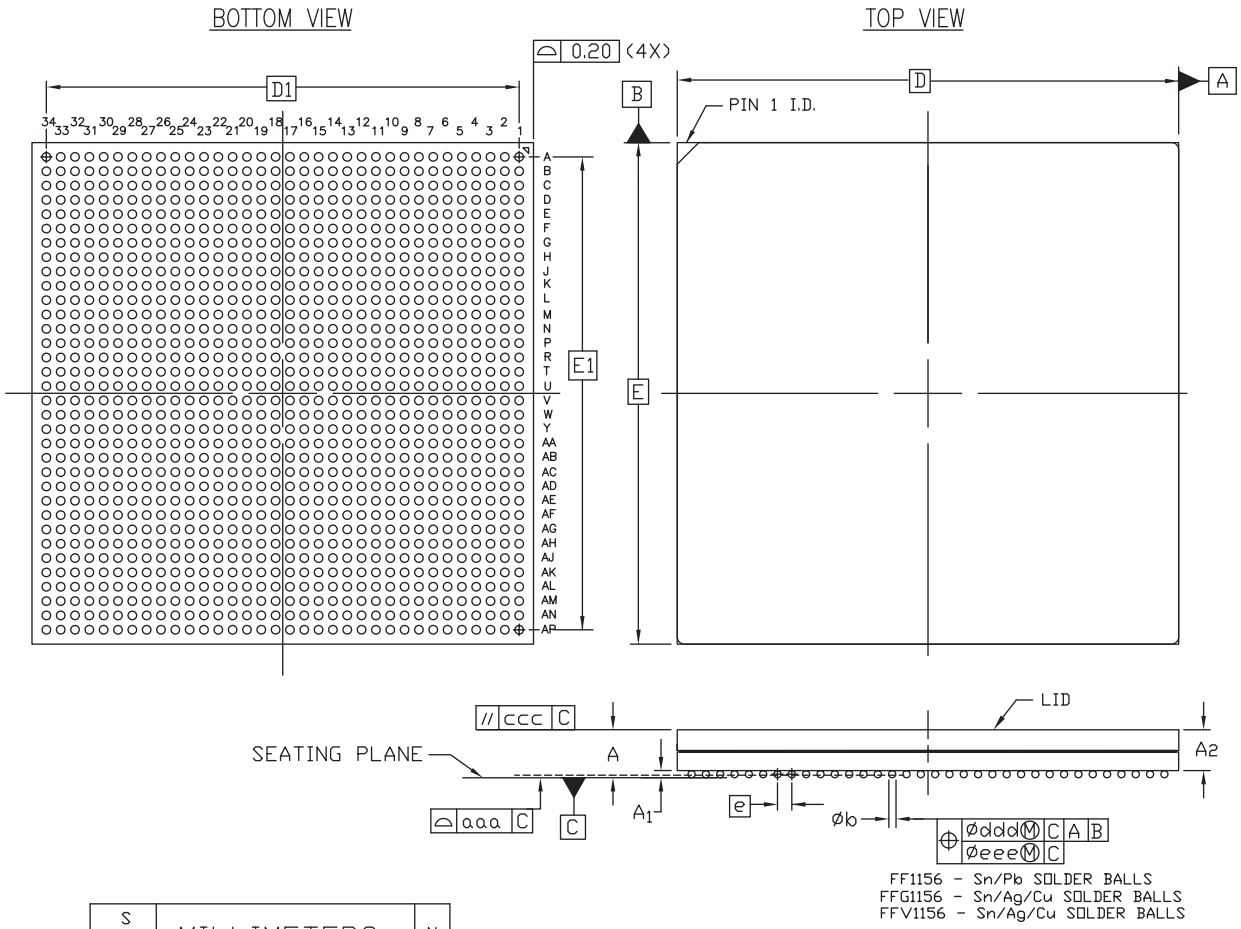
NOTES:

1. DIMENSIONS ARE FOR KINTEX-7
2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
3. SYMBOL 'M' IS THE BALL MATRIX SIZE
4. CONFORMS TO JEDEC MS-034-AAR-1
5. ACTUAL SOLDER BALL COUNT = 1156

ug475_c4_ffg1156_k7_020818

Figure 4-36: **FF1156 and FFG1156 (XC7K420T and XC7K480T) Flip-Chip BGA Package Specification**

FF1156, FFG1156, and FFV1156 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	---	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	---	2.75	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	---	---	0.20	
ccc	---	---	0.35	
ddd	---	---	0.30	
eee	---	---	0.10	
M	34			2

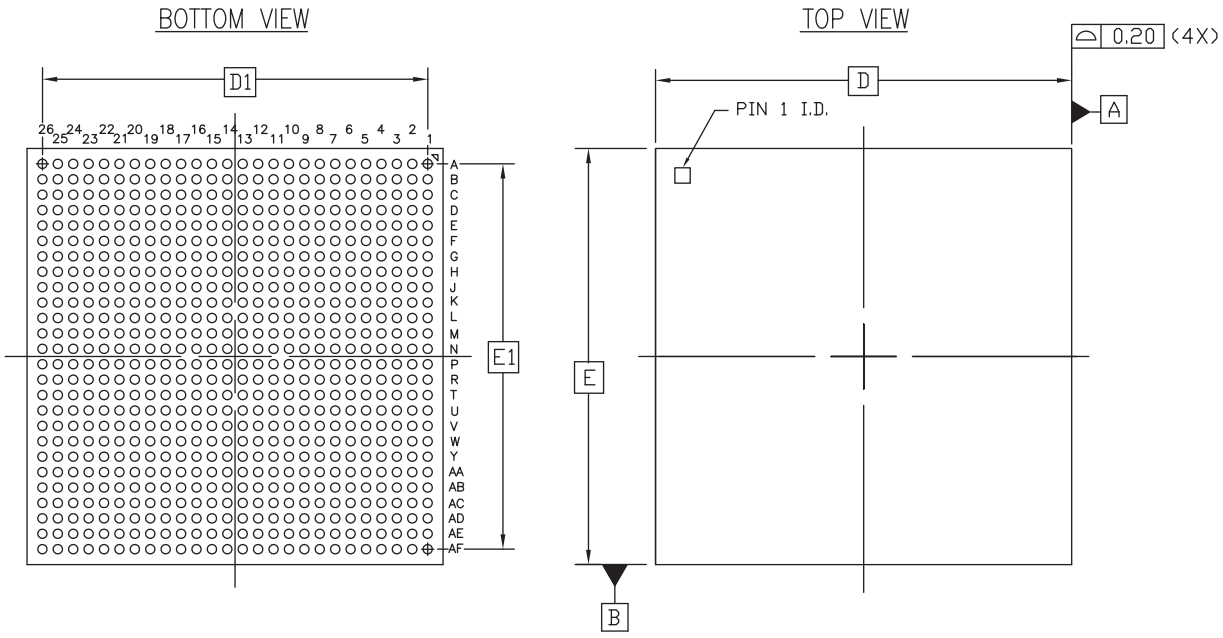
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156
5. THIS PACKAGE IS USED FOR KINTEX®–7 FPGAs REFER TO PK384 FOR THE MECHANICAL DRAWING OF THE FF1156 PACKAGE USED FOR VIRTEX®–5 FPGAS AND PK401 FOR VIRTEX®–6 FPGAS

ug475_c4_07_031516

Figure 4-37: **FF1156, FFG1156, and FFV1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs**

RF676 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.97	3.17	3.37	
A_1	0.40	0.50	0.60	
A_2	2.57	2.67	2.77	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

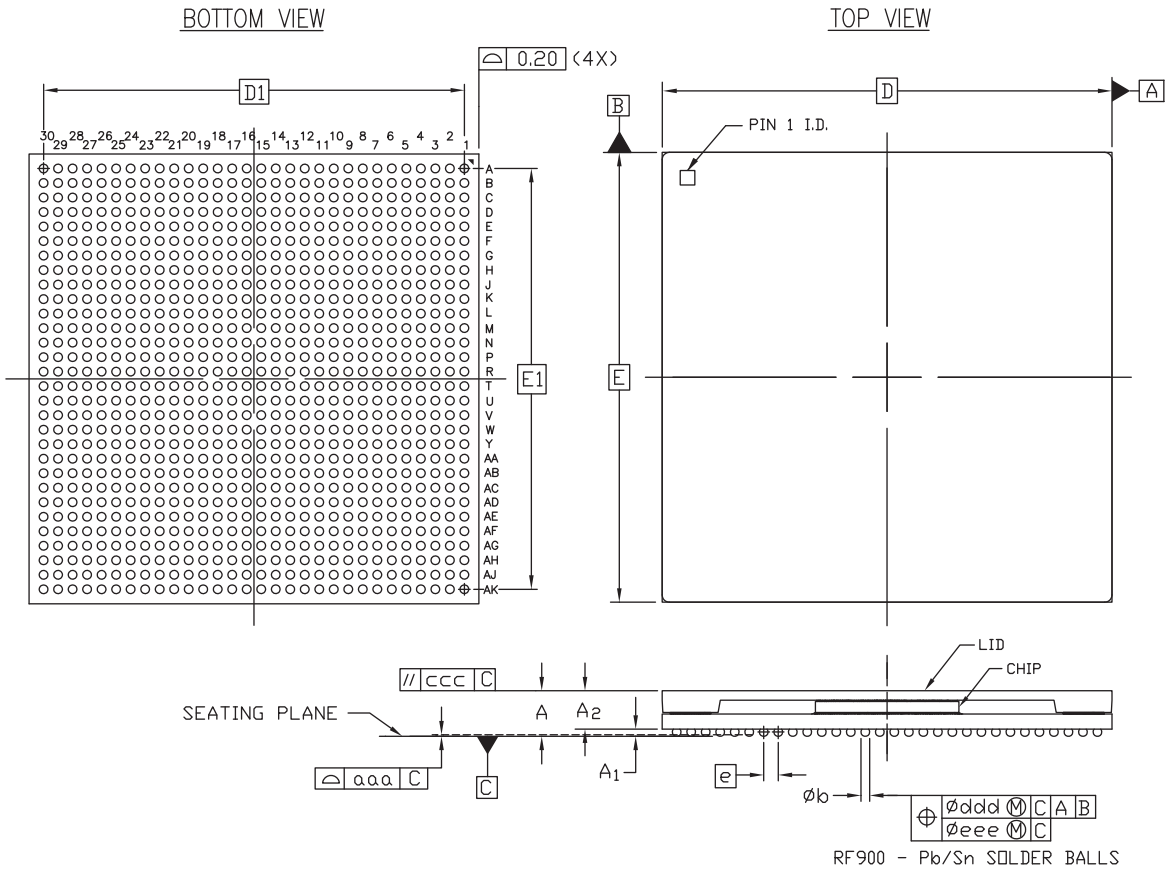
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

ug475_c4_28_070516

Figure 4-38: **RF676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

RF900 (Kintex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.84	3.14	3.44	
A_1	0.40	0.50	0.60	
A_2	2.44	2.64	2.84	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

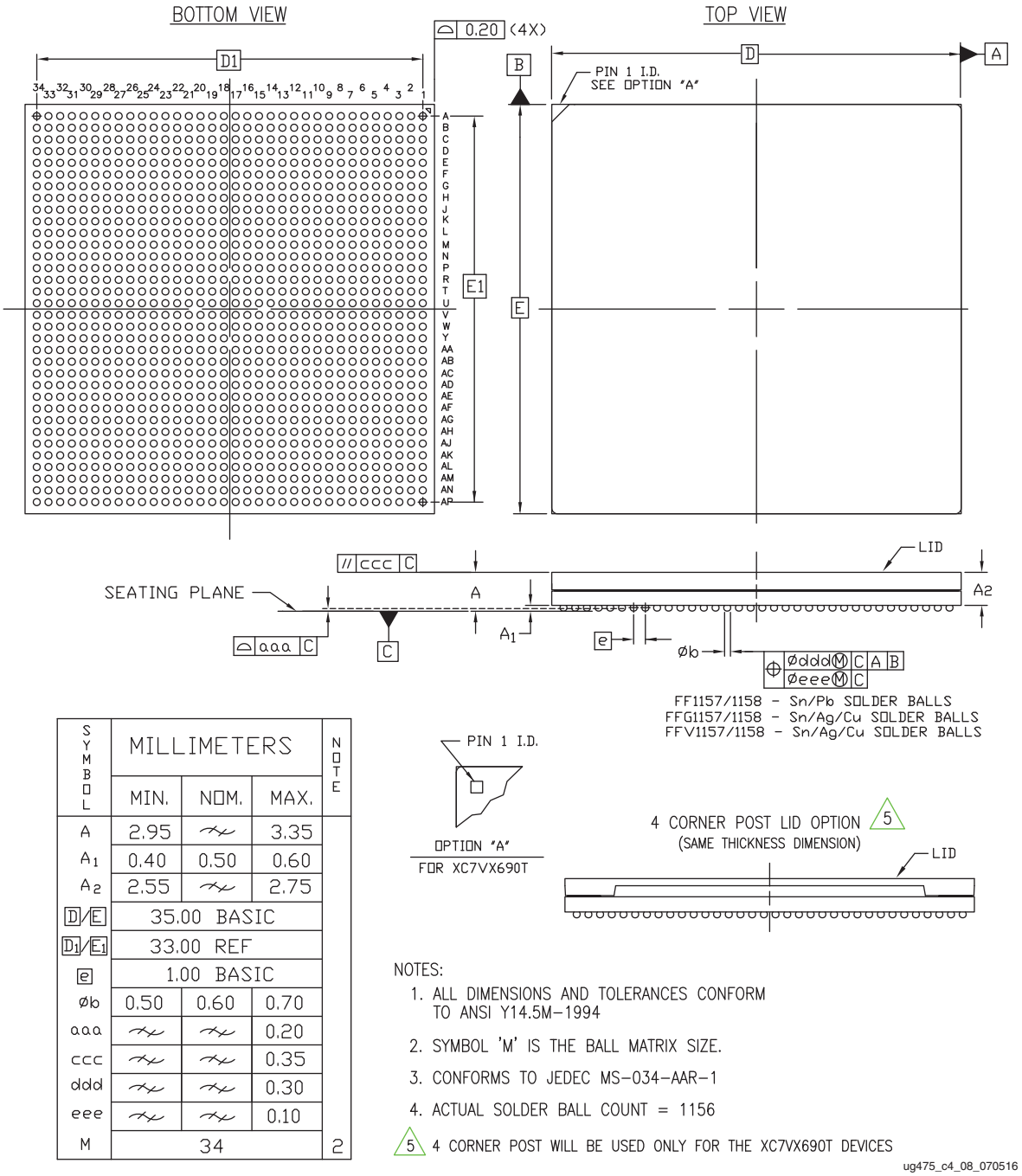
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAN–1

ug475_c4_30_092613

Figure 4-39: **RF900 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.95	~~	3.35	
A_1	0.40	0.50	0.60	
A_2	2.55	~~	2.75	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	34			2

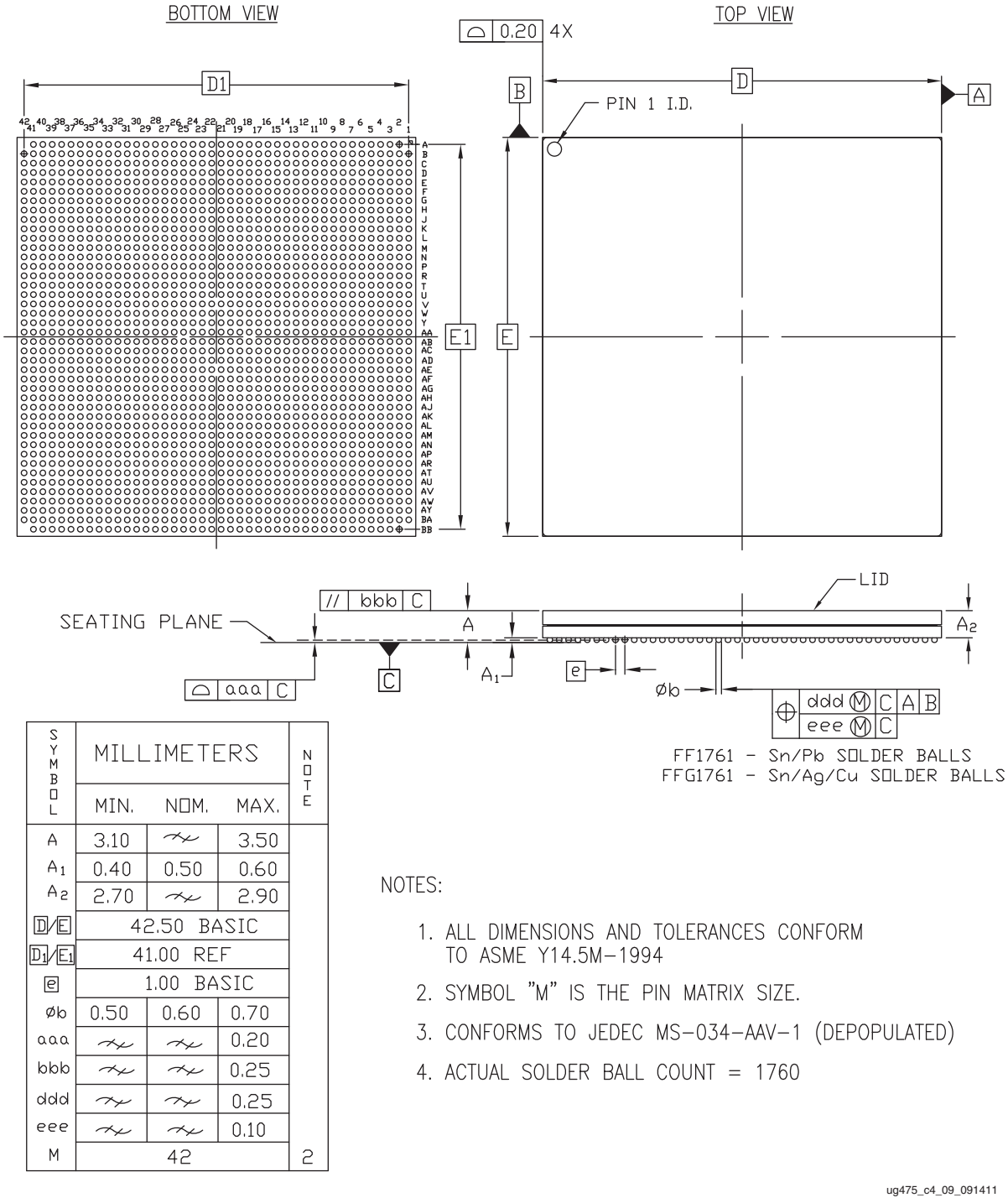
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156
5. 4 CORNER POST WILL BE USED ONLY FOR THE XC7VX690T DEVICES

ug475_c4_08_070516

Figure 4-40: **FF1157, FFG1157, FFV1157, FF1158, FFG1158, and FFV1158 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

FF1761 and FFG1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.10		3.50	
A1	0.40	0.50	0.60	
A2	2.70		2.90	
D/E	42.50 BASIC			
D1/E1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

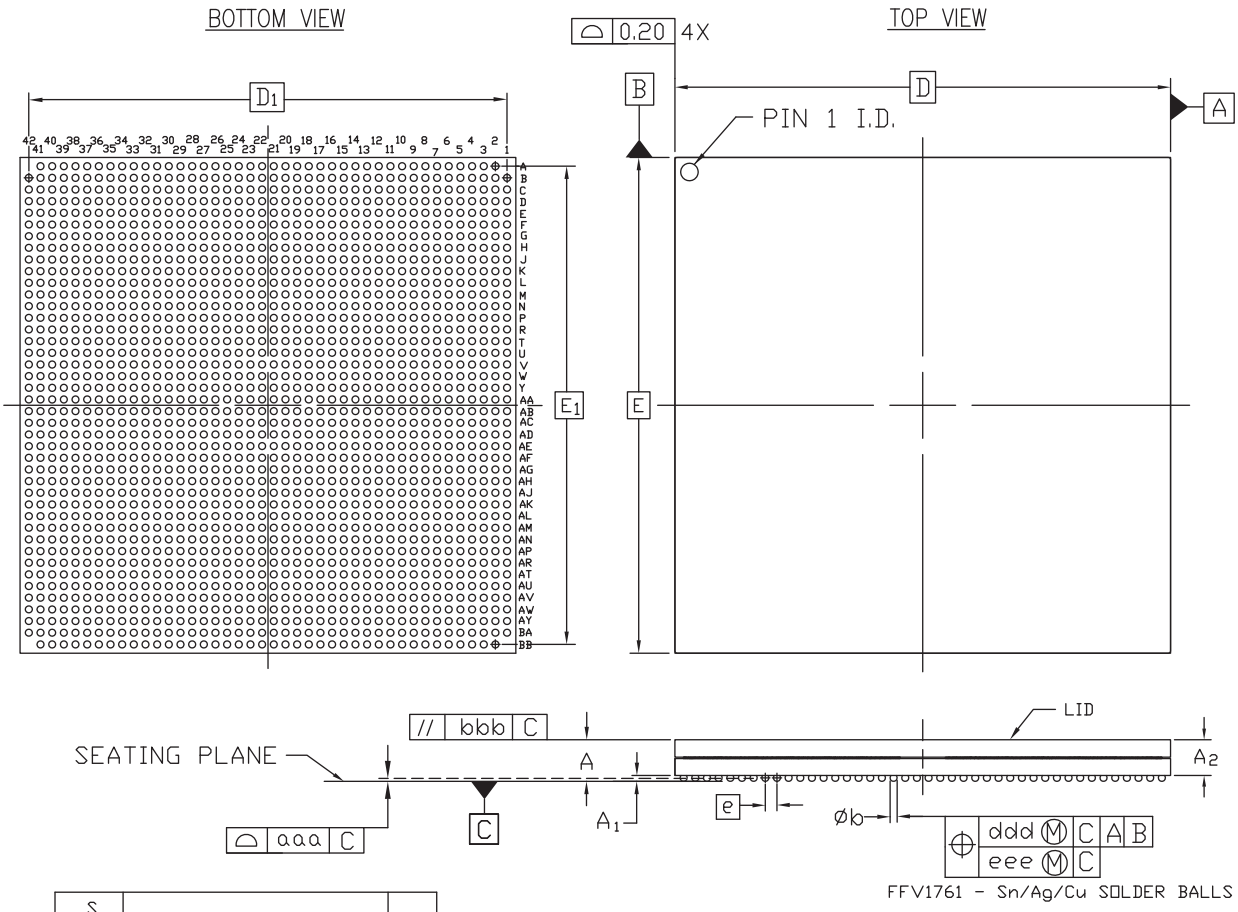
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_09_091411

Figure 4-41: **FF1761 and FFG1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

FFV1761 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.37	3.57	3.77	
A_1	0.40	0.50	0.60	
A_2	2.87	3.07	3.27	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	42			2

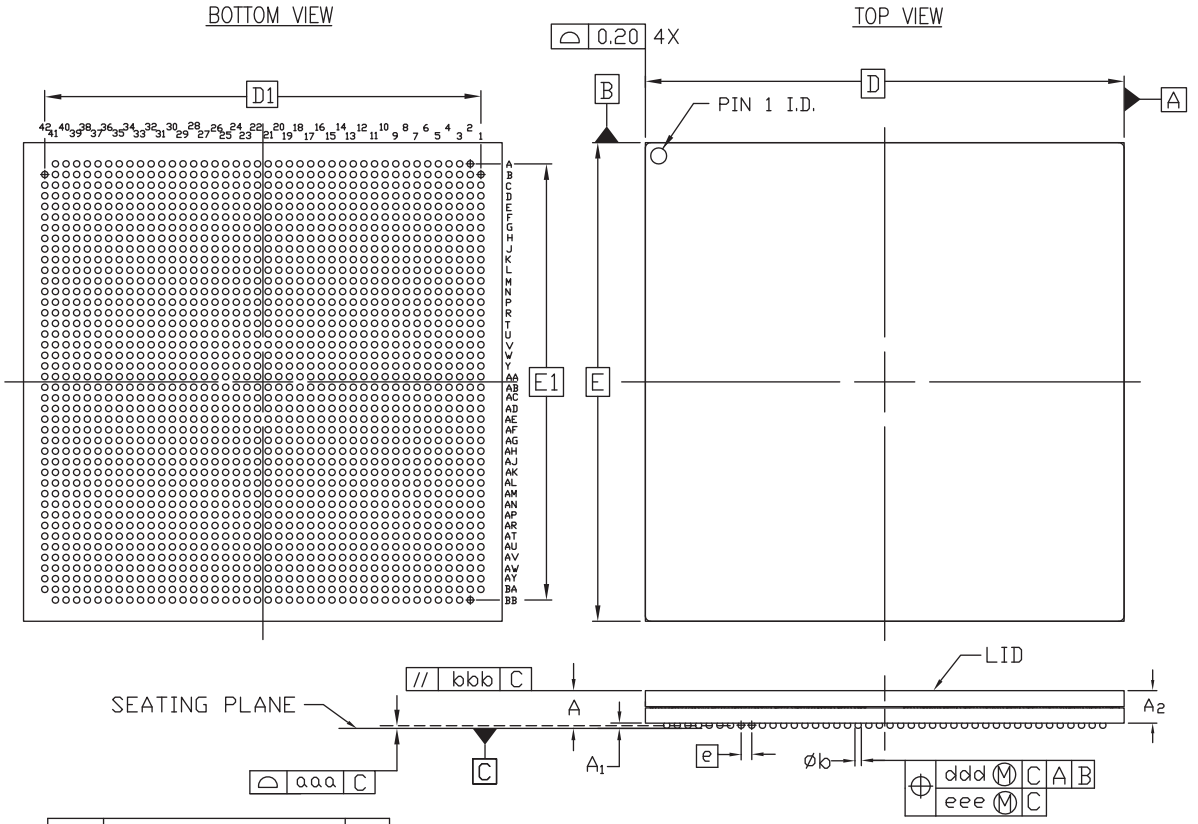
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_233_031516

Figure 4-42: **FFV1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

FH1761 and FHG1761 (Virtex-7 T FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.75	
A_1	0.40	0.50	0.60	
A_2	2.85		3.15	
D/E	45.00 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

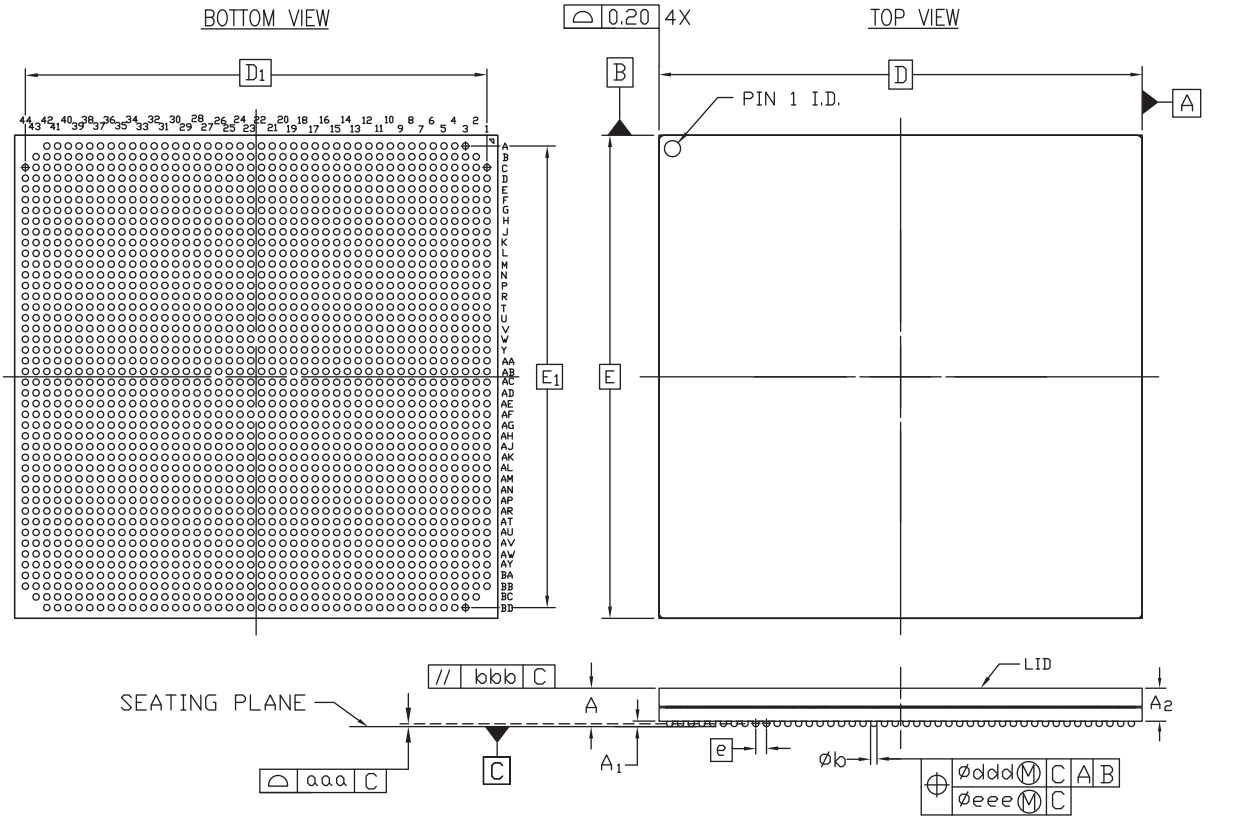
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_10_092412

Figure 4-43: **FH1761 and FHG1761 Flip-Chip BGA Package Specification for Virtex-7 T FPGAs**

FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 (Virtex-7 XT FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.65	
A_1	0.40	0.50	0.60	
A_2	2.85		3.05	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

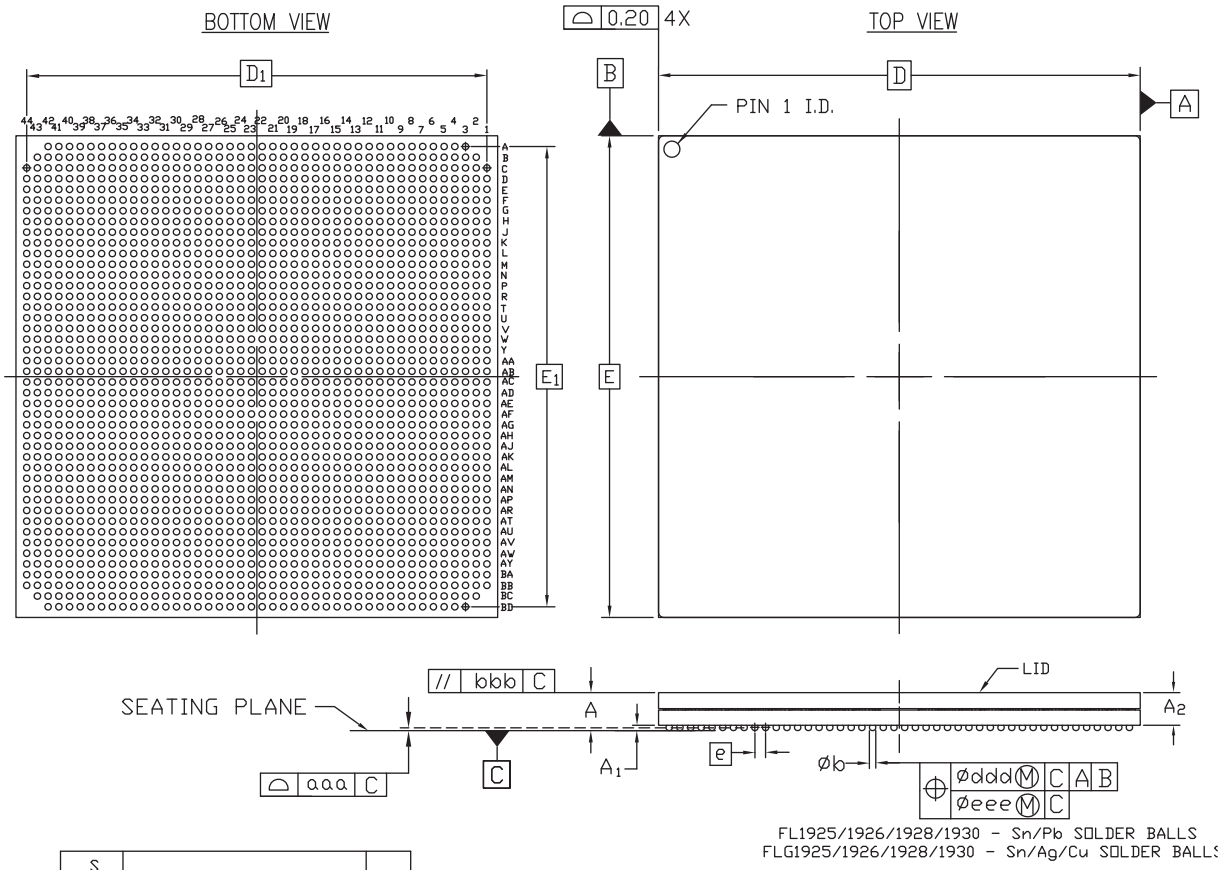
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924
4. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

ug475_c4_11_070516

Figure 4-44: **FF1926, FFG1926, FF1927, FFG1927, FFV1927, FF1928, FFG1928, FF1930, and FFG1930 Flip-Chip BGA Package Specification for Virtex-7 XT FPGAs**

FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 (Virtex-7 FPGAs) Flip-Chip BGA (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.75	
A_1	0.40	0.50	0.60	
A_2	2.85		3.15	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

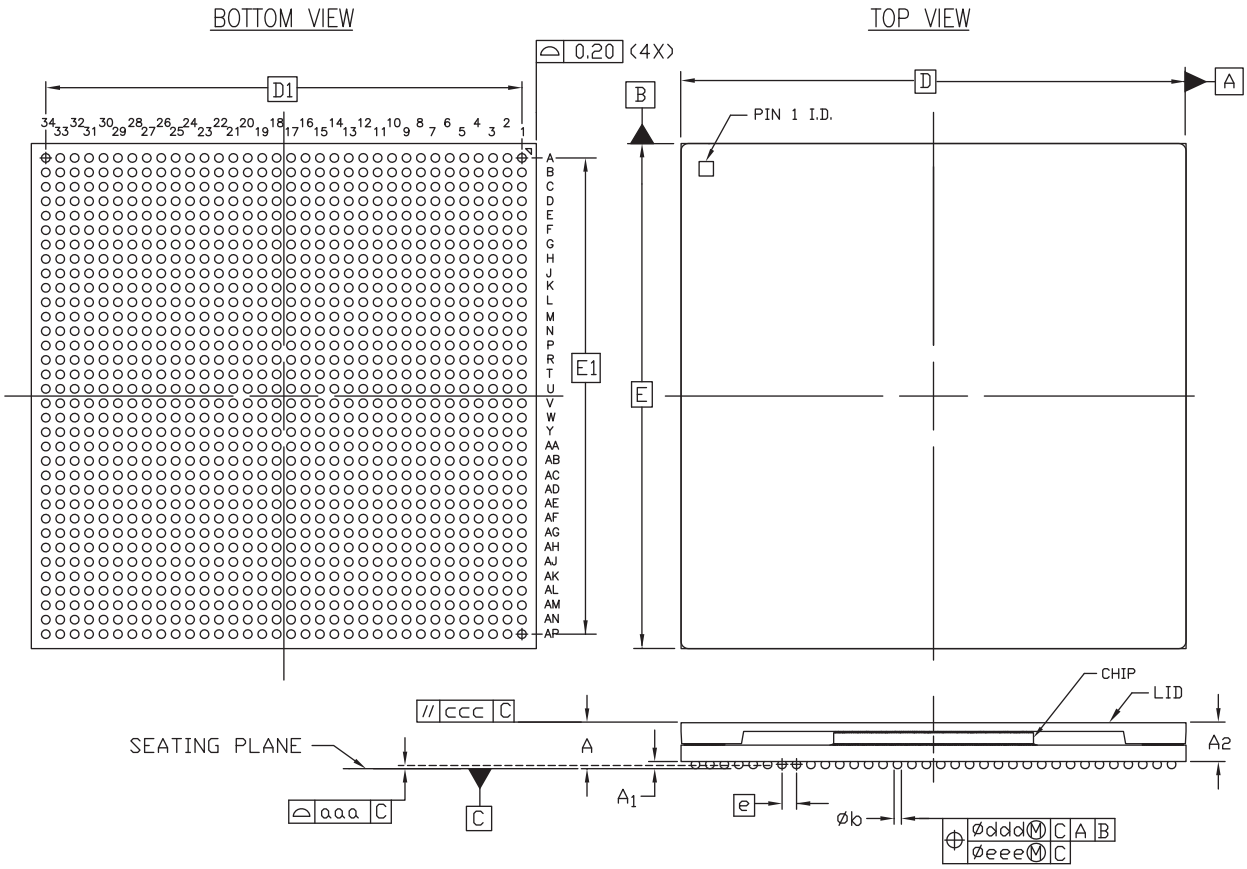
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924

ug475_c4_12_070516

Figure 4-45: **FL1925, FLG1925, FL1926, FLG1926, FL1928, FLG1928, and FL1930, FLG1930 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

RF1157 and RF1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.88	3.18	3.48	
A_1	0.40	0.50	0.60	
A_2	2.48	2.68	2.88	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	34			2

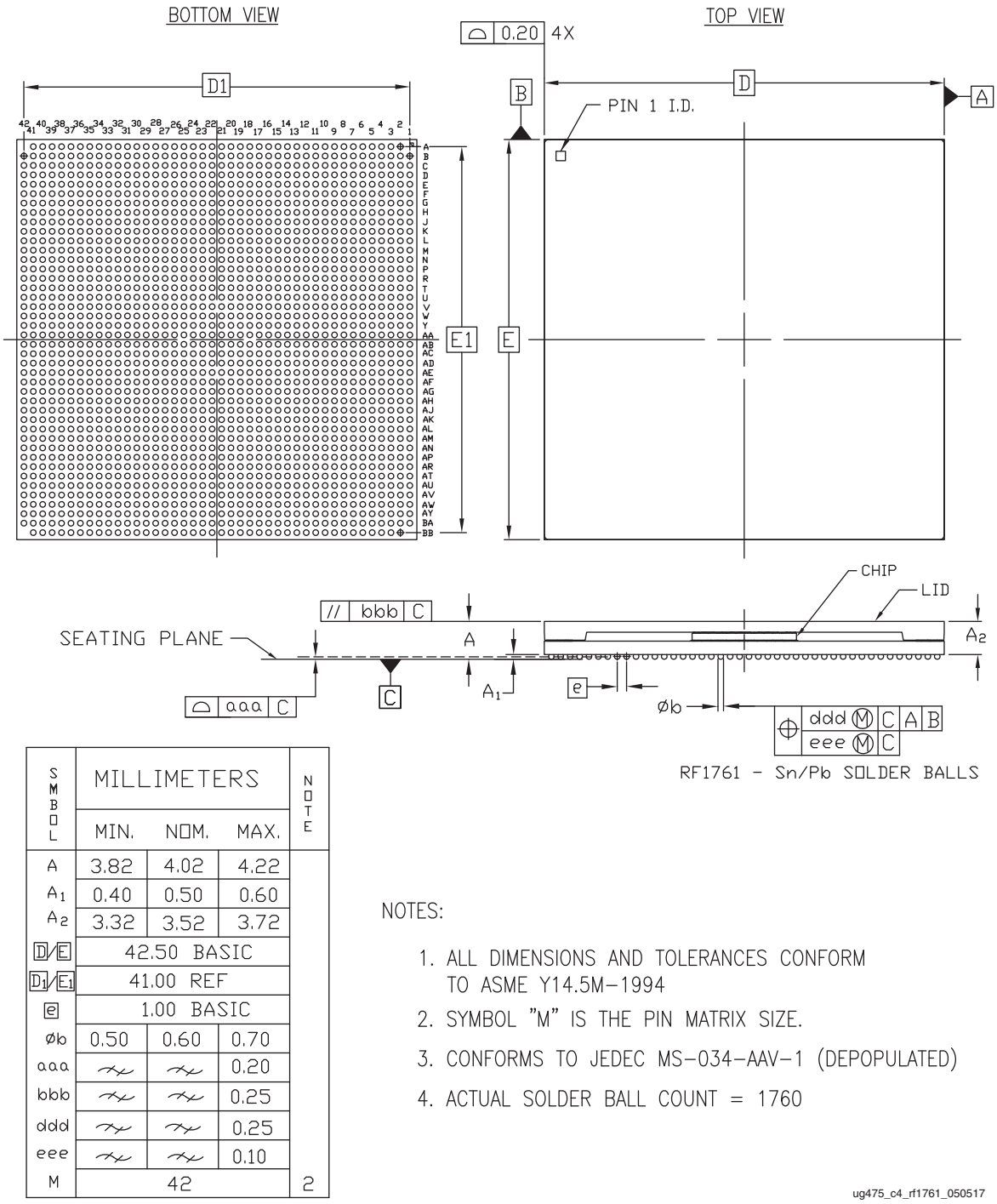
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug475_c4_209_071615

Figure 4-46: **RF1157 and RF1158 Flip-Chip BGA Package Specifications for Virtex-7 FPGAs**

RF1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.82	4.02	4.22	
A_1	0.40	0.50	0.60	
A_2	3.32	3.52	3.72	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

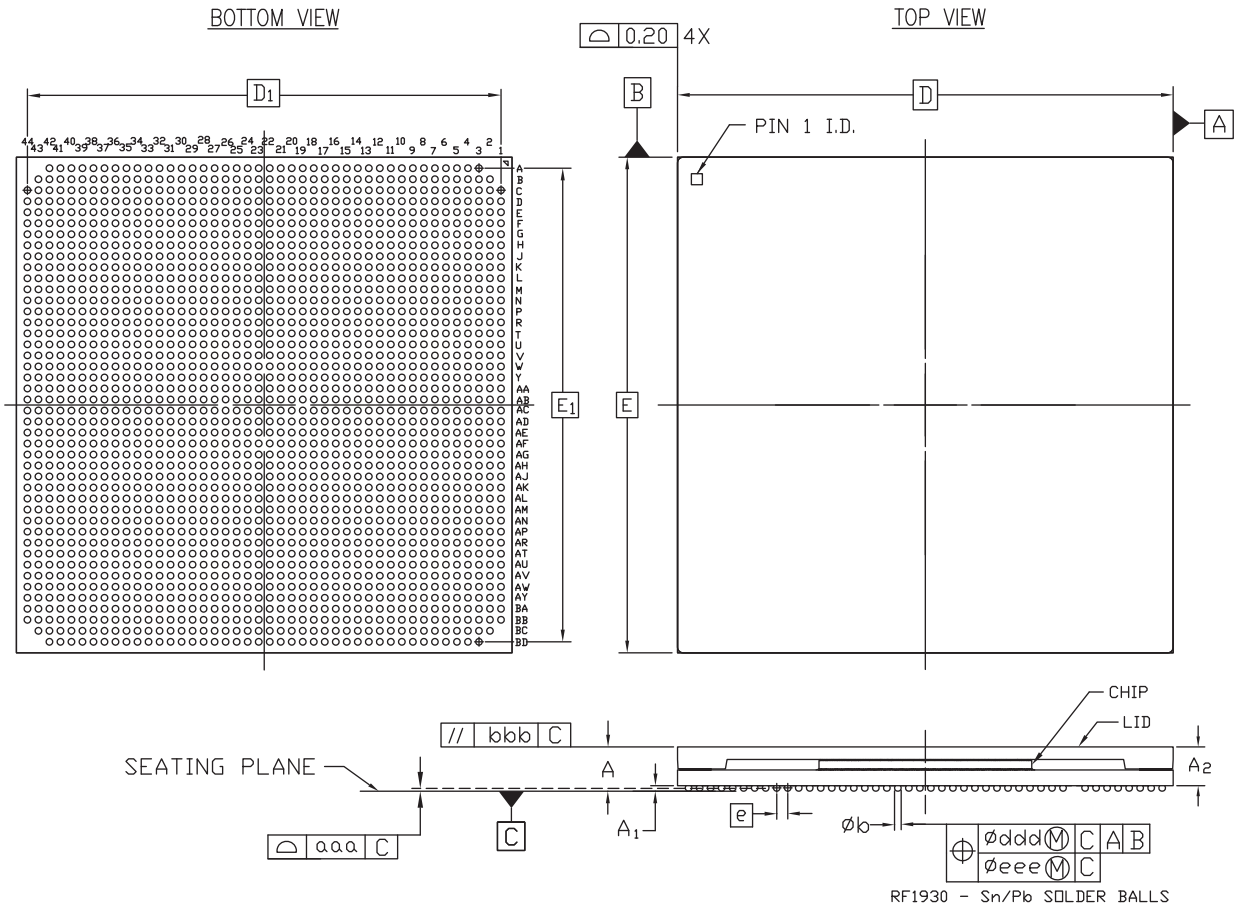
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_rf1761_050517

Figure 4-47: **RF1761 Flip-Chip BGA Package Specifications for Virtex-7 FPGAs**

RF1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.77	4.02	4.27	
A_1	0.40	0.50	0.60	
A_2	3.37	3.52	3.67	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924
4. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

ug475_c4_211_092613

Figure 4-48: **RF1930 Flip-Chip BGA Package Specifications for Virtex-7 FPGAs**

Thermal Specifications

Introduction

Most 7 series FPGAs are offered in thermally efficient flip-chip BGA packages. These 0.5 mm, 0.8 mm, and 1.0 mm flip-chip packages range in pin-count from the smaller 8 x 8 mm CPGA196 to the 45 x 45 mm FFG1930. This suite of packages is used to address the various power requirements of the 7 series devices. All 7 series devices are implemented in the 28 nm process technology (that is Artix®-7, Kintex®-7, Spartan®-7, and Virtex®-7 FPGAs).

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. 7 series devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

Thermal Resistance Data

Table 5-1 shows the thermal resistance data for 7 series devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

Note: The data in Table 5-1 is for device/package comparison purposes only. Do not apply directly to your system design. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.

The thermal data query for all available devices by package is available on the Xilinx website:

www.xilinx.com/cgi-bin/thermal/thermal.pl

Table 5-1: **Thermal Resistance Data—All Devices**

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)[1]		
						@250 LFM	@500 LFM	@750 LFM
Spartan-7 FPGAs								
CPGA196	8 x 8	XC7S6	15.1	35.0	8.46	30.1	28.6	27.9
CPGA196	8 x 8	XA7S6	15.1	35.0	8.46	30.1	28.6	27.9
CPGA196	8 x 8	XC7S15	15.1	35.0	8.46	30.1	28.6	27.9
CPGA196	8 x 8	XA7S15	15.1	35.0	8.46	30.1	28.6	27.9
CSGA225	13 x 13	XC7S6	17.4	32.2	10.6	26.7	25.1	24.2
CSGA225	13 x 13	XA7S6	17.4	32.2	10.6	26.7	25.1	24.2
CSGA225	13 x 13	XC7S15	17.4	32.2	10.6	26.7	25.1	24.2
CSGA225	13 x 13	XA7S15	17.4	32.2	10.6	26.7	25.1	24.2
CSGA225	13 x 13	XC7S25	15.6	30.6	9.4	27.1	23.5	24.4
CSGA225	13 x 13	XA7S25	15.6	30.6	9.4	27.1	23.5	24.4
CSGA324	15 x 15	XC7S25	9.4	22.1	5.65	18.1	16.7	16.2
CSGA324	15 x 15	XA7S25	9.4	22.1	5.65	18.1	16.7	16.2
CSGA324	15 x 15	XC7S50	7.6	20.1	4.47	15.9	14.8	14.1
CSGA324	15 x 15	XA7S50	7.6	20.1	4.47	15.9	14.8	14.1
FTGB196	15 x 15	XC7S6	13.7	27.8	8.9	22.5	21.1	20.0
FTGB196	15 x 15	XA7S6	13.7	27.8	8.9	22.5	21.1	20.0
FTGB196	15 x 15	XC7S15	13.7	27.8	8.9	22.5	21.1	20.0
FTGB196	15 x 15	XA7S15	13.7	27.8	8.9	22.5	21.1	20.0
FTGB196	15 x 15	XC7S25	12.5	26.2	7.1	20.9	19.4	18.6
FTGB196	15 x 15	XA7S25	12.5	26.2	7.1	20.9	19.4	18.6
FTGB196	15 x 15	XC7S50	8.8	22.6	5.3	17.3	15.9	15.1
FTGB196	15 x 15	XA7S50	8.8	22.6	5.3	17.3	15.9	15.1
FGGA484	23 x 23	XC7S50	9.2	17.9	5.85	13.8	12.7	12.1
FGGA484	23 x 23	XA7S50	9.2	17.9	5.85	13.8	12.7	12.1
FGGA484	23 x 23	XC7S75	6.8	15.8	3.85	12.1	11.0	10.4
FGGA484	23 x 23	XA7S75	6.8	15.8	3.85	12.1	11.0	10.4
FGGA484	23 x 23	XC7S100	6.8	15.8	3.85	12.1	11.0	10.4
FGGA484	23 x 23	XA7S100	6.8	15.8	3.85	12.1	11.0	10.4
FGGA676	27 x 27	XC7S75	6.8	15.0	3.71	11.2	10.2	9.7
FGGA676	27 x 27	XA7S75	6.8	15.0	3.71	11.2	10.2	9.7
FGGA676	27 x 27	XC7S100	6.8	15.0	3.71	11.2	10.2	9.7
FGGA676	27 x 27	XA7S100	6.8	15.0	3.71	11.2	10.2	9.7

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)[1]		
						@250 LFM	@500 LFM	@750 LFM
Artix-7 FPGAs								
CP/CPG236	10 x 10	XC7A15T	7.9	24.8	5.29	20.3	18.9	18.0
CPG236	10 x 10	XA7A15T	7.9	24.8	5.29	20.3	18.9	18.0
CP/CPG236	10 x 10	XC7A35T	7.9	24.8	5.29	20.3	18.9	18.0
CPG236	10 x 10	XA7A35T	7.9	24.8	5.29	20.3	18.9	18.0
CP/CPG236	10 x 10	XC7A50T	7.9	24.8	5.29	20.3	18.9	18.0
CPG236	10 x 10	XA7A50T	7.9	24.8	5.29	20.3	18.9	18.0
CPG238	10 x 10	XC7A12T	8.5	8.42	25.4	20.9	19.5	18.8
CPG238	10 x 10	XA7A12T	8.5	8.42	25.4	20.9	19.5	18.8
CPG238	10 x 10	XC7A25T	8.5	8.42	25.4	20.9	19.5	18.8
CPG238	10 x 10	XA7A25T	8.5	8.42	25.4	20.9	19.5	18.8
CS/CSG324	15 x 15	XC7A15T	6.9	19.6	4.03	15.4	14.3	13.6
CSG324	15 x 15	XA7A15T	6.9	19.6	4.03	15.4	14.3	13.6
CS/CSG324	15 x 15	XC7A35T	6.9	19.6	4.03	15.4	14.3	13.6
CSG324	15 x 15	XA7A35T	6.9	19.6	4.03	15.4	14.3	13.6
CS/CSG324	15 x 15	XC7A50T	6.9	19.6	4.03	15.4	14.3	13.6
CSG324	15 x 15	XA7A50T	6.9	19.6	4.03	15.4	14.3	13.6
CS/CSG324	15 x 15	XC7A75T	5.7	18.2	3.25	14.1	13.0	12.3
CSG324	15 x 15	XA7A75T	5.7	18.2	3.25	14.1	13.0	12.3
CS/CSG324	15 x 15	XC7A100T	5.7	18.2	3.25	14.1	13.0	12.3
CSG324	15 x 15	XA7A100T	5.7	18.2	3.25	14.1	13.0	12.3
CS/CSG324	15 x 15	XQ7A100T	5.7	18.2	3.25	14.1	13.0	12.3
CSG325	15 x 15	XC7A12T	9.4	22.1	5.65	18.1	16.7	16.2
CSG325	15 x 15	XA7A12T	9.4	22.1	5.65	18.1	16.7	16.2
CS/CSG325	15 x 15	XC7A15T	6.9	19.6	4.05	15.4	14.3	13.6
CSG325	15 x 15	XA7A15T	6.9	19.6	4.05	15.4	14.3	13.6
CSG325	15 x 15	XC7A25T	9.4	22.1	5.65	18.1	16.7	16.2
CSG325	15 x 15	XA7A25T	9.4	22.1	5.65	18.1	16.7	16.2
CS/CSG325	15 x 15	XC7A35T	6.9	19.6	4.05	15.4	14.3	13.6
CSG325	15 x 15	XA7A35T	6.9	19.6	4.05	15.4	14.3	13.6
CS/CSG325	15 x 15	XC7A50T	6.9	19.6	4.05	15.4	14.3	13.6
CSG325	15 x 15	XA7A50T	6.9	19.6	4.05	15.4	14.3	13.6
CS/CSG325	15 x 15	XQ7A50T	6.9	19.6	4.05	15.4	14.3	13.6

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)(1)		
						@250 LFM	@500 LFM	@750 LFM
FT/FTG256	17 x 17	XC7A15T	8.4	19.8	4.24	15.6	14.4	13.7
FT/FTG256	17 x 17	XC7A35T	8.4	19.8	4.24	15.6	14.4	13.7
FT/FTG256	17 x 17	XC7A50T	8.4	19.8	4.24	15.6	14.4	13.7
FT/FTG256	17 x 17	XC7A75T	6.9	18.2	3.34	14.1	12.9	12.2
FT/FTG256	17 x 17	XC7A100T	6.9	18.2	3.34	14.1	12.9	12.2
SB/SBG/SBV484	19 x 19	XC7A200T	5.0	14.8	0.08	10.9	9.8	9.2
RS484	19 x 19	XQ7A200T	4.7	14.2	0.33	9.9	8.7	8.0
FB/FBG/FBV484	23 x 23	XC7A200T	4.8	13.9	0.08	9.9	8.9	8.3
FG/FGG484	23 x 23	XC7A15T	8.7	17.7	4.89	13.6	12.6	12.1
FG/FGG484	23 x 23	XC7A35T	8.7	17.7	4.89	13.6	12.6	12.1
FG/FGG484	23 x 23	XC7A50T	8.7	17.7	4.89	13.6	12.6	12.1
FG/FGG484	23 x 23	XQ7A50T	9.1	18.1	5.42	14.1	13.0	12.5
FG/FGG484	23 x 23	XC7A75T	6.8	15.8	3.85	12.1	11.0	10.4
FGG484	23 x 23	XA7A75T	6.8	15.8	3.85	12.1	11.0	10.4
FG/FGG484	23 x 23	XC7A100T	6.8	15.8	3.85	12.1	11.0	10.4
FGG484	23 x 23	XA7A100T	6.8	15.8	3.85	12.1	11.0	10.4
FG/FGG484	23 x 23	XQ7A100T	6.8	15.8	3.85	12.1	11.0	10.4
RB484	23 x 23	XQ7A200T	4.0	12.5	0.26	8.3	7.2	6.7
FB/FBG/FBV676	27 x 27	XC7A200T	4.7	13.0	0.08	9.2	8.2	7.7
FG/FGG676	27 x 27	XC7A75T	6.8	15.0	3.71	11.2	10.2	9.7
FG/FGG676	27 x 27	XC7A100T	6.8	15.0	3.71	11.2	10.2	9.7
RB676	27 x 27	XQ7A200T	3.7	11.4	0.33	7.3	6.2	5.6
FF/FFG/FFV1156	35 x 35	XC7A200T	2.6	9.3	0.32	6.1	5.2	4.7
Kintex-7 FPGAs								
FB/FBG/FBV484	23 x 23	XC7K70T	6.8	16.4	0.13	11.7	10.7	10.1
		XC7K160T	5.3	14.6	0.10	10.5	9.5	8.9
FB/FBG/FBV676	27 x 27	XC7K70T	6.7	15.7	0.13	11.8	10.8	10.2
		XC7K160T	5.2	14.0	0.10	9.8	8.8	8.3
		XC7K325T	4.2	12.9	0.06	8.9	8.0	7.5
		XC7K410T	3.7	12.2	0.05	8.6	7.6	7.1
FF/FFG/FFV676	27 x 27	XC7K160T	4.0	11.7	0.41	7.5	6.4	5.8
		XC7K325T	3.5	11.1	0.26	7.3	6.3	5.8
		XC7K410T	3.3	10.9	0.20	7.0	6.0	5.5

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)[1]		
						@250 LFM	@500 LFM	@750 LFM
RF676	27 x 27	XQ7K325T	3.5	11.1	0.26	7.3	6.3	5.8
		XQ7K410T	3.3	10.9	0.20	7.0	6.0	5.5
FB/FBG/FBV900	31 x 31	XC7K325T	4.3	12.0	0.06	8.9	7.9	7.3
		XC7K410T	3.7	11.4	0.05	8.3	7.3	6.7
FF/FFG/FFV900	31 x 31	XC7K325T	2.8	9.7	0.26	6.2	5.4	5.0
		XC7K410T	2.6	9.5	0.19	6.0	5.2	4.9
RF900	31 x 31	XQ7K325T	3.3	10.0	0.26	6.4	5.4	4.9
		XQ7K410T	3.0	9.8	0.20	6.3	5.4	4.9
FF/FFG/FFV901	31 x 31	XC7K355T	3.2	10.0	0.23	6.3	5.3	4.8
		XC7K420T	2.9	9.6	0.17	6.2	5.3	4.8
		XC7K480T	2.9	9.6	0.17	6.2	5.3	4.8
FF/FFG/FFV1156	35 x 35	XC7K420T	2.4	8.7	0.17	5.7	4.7	4.3
		XC7K480T	2.4	8.7	0.17	5.7	4.7	4.3
Virtex-7 T FPGAs								
FF/FFG1157	35 x 35	XC7V585T	2.3	8.7	0.14	5.6	4.8	4.3
RF1157	35 x 35	XQ7V585T	2.7	8.9	0.15	5.8	4.8	4.3
FF/FFG1761	42.5 x 42.5	XC7V585T	2.1	7.6	0.11	4.9	4.1	3.7
RF1761	42.5 x 42.5	XQ7V585T	2.4	7.8	0.11	4.9	4.0	3.5
FH/FHG1761	45 x 45	XC7V2000T	2.0	7.0	0.05	4.3	3.5	3.1
FL/FLG1925	45 x 45	XC7V2000T	1.7	6.9	0.06	4.2	3.4	3.0
Virtex-7 XT FPGAs								
FF/FFG/FFV1157	35 x 35	XC7VX330T	2.5	8.9	0.19	5.8	4.9	4.5
		XC7VX415T	2.3	8.8	0.16	5.7	4.8	4.4
		XC7VX485T	2.3	8.7	0.13	5.6	4.7	4.3
		XC7VX690T	2.3	8.7	0.09	5.5	4.6	4.1
RF1157	35 x 35	XQ7VX330T	2.9	9.3	0.19	6.0	5.0	4.4
		XQ7VX690T	2.3	8.7	0.09	5.3	4.4	3.9
FF/FFG/FFV1158	35 x 35	XC7VX415T	2.3	8.8	0.16	5.7	4.8	4.4
		XC7VX485T	2.3	8.7	0.13	5.6	4.7	4.3
		XC7VX550T	2.3	8.7	0.09	5.5	4.6	4.1
		XC7VX690T	2.3	8.7	0.09	5.5	4.6	4.1
RF1158	35 x 35	XQ7VX690T	2.3	8.7	0.09	5.3	4.4	3.9

Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	$\theta_{JA\text{-}Effective}$ (°C/W)(1)		
						@250 LFM	@500 LFM	@750 LFM
FF/FFG/FFV1761	42.5 x 42.5	XC7VX330T	2.3	7.8	0.19	5.1	4.3	3.9
		XC7VX485T	2.1	7.6	0.13	4.9	4.1	3.6
		XC7VX690T	1.9	7.5	0.09	4.7	3.9	3.5
RF1761	42.5 x 42.5	XQ7VX485T	2.3	7.7	0.14	4.8	3.9	3.4
		XQ7VX330T	2.7	8.0	0.20	5.0	4.1	3.6
		XQ7VX690T	2.1	7.5	0.09	4.7	3.8	3.3
FF/FFG1926	45 x 45	XC7VX690T	1.9	7.1	0.09	4.5	3.7	3.3
		XC7VX980T	1.8	7.1	0.09	4.4	3.6	3.2
FF/FFG/FFV1927	45 x 45	XC7VX415T	2.1	7.4	0.16	4.7	3.9	3.5
		XC7VX485T	2.0	7.3	0.13	4.6	3.8	3.4
		XC7VX550T	1.8	7.1	0.09	4.4	3.6	3.2
		XC7VX690T	1.8	7.1	0.09	4.4	3.6	3.2
FF/FFG1928	45 x 45	XC7VX980T	1.8	7.1	0.09	4.4	3.6	3.2
FF/FFG1930	45 x 45	XC7VX485T	2.0	7.3	0.13	4.8	3.9	3.5
		XC7VX690T	1.9	7.1	0.09	4.5	3.7	3.3
		XC7VX980T	1.8	7.1	0.09	4.4	3.6	3.2
RF1930	45 x 45	XQ7VX485T	2.4	7.5	0.14	4.8	3.9	3.5
		XQ7VX690T	2.2	7.3	0.10	4.5	3.6	3.1
		XQ7VX980T	2.1	7.3	0.09	4.5	3.6	3.1
FL/FLG1926	45 x 45	XC7VX1140T	1.7	6.9	0.06	4.2	3.4	3.0
FL/FLG1928	45 x 45	XC7VX1140T	1.7	6.9	0.06	4.2	3.4	3.0
FL/FLG1930	45 x 45	XC7VX1140T	1.7	6.9	0.06	4.2	3.4	3.0

Notes:

1. All $\theta_{JA\text{-}Effective}$ values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The Xilinx power estimation tools (Vivado® Power Analysis, and Xilinx Power Estimator), which require detailed board dimensions and layer counts, are useful for deriving more precise $\theta_{JA\text{-}Effective}$ values.

Support for Thermal Models

Table 5-1 provides the traditional thermal resistance data for 7 series devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for 7 series FPGAs, boundary conditions independent thermal resistor network (Delphi) models are offered. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-1.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi models are available for download on the Xilinx website (under the Device Model tab).

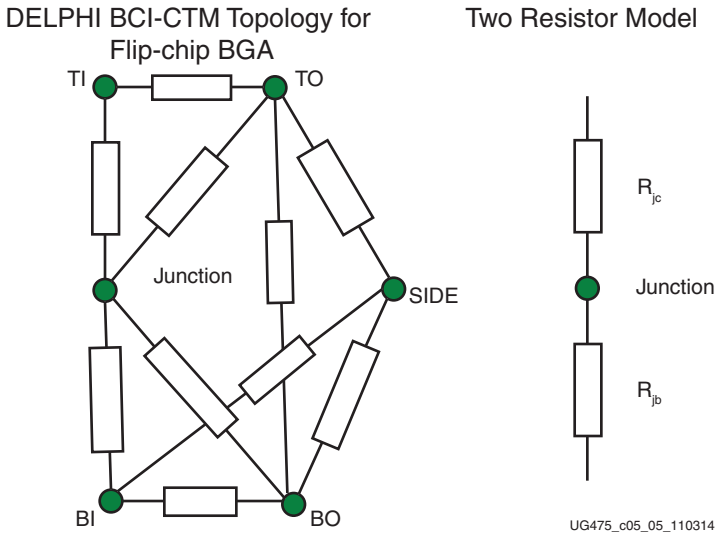


Figure 5-1: **Thermal Model Topologies**

Note: Xilinx recommends the use of the Delphi thermal model during thermal modeling of a package. The Delphi thermal model includes consideration of the thermal interface material parameters and the manufacture variation on the thermal solution. Examples of manufacture variations include the tolerance in airflow from a fan, the tolerance on performance of the heat pipe and vapor chamber, and the manufacture variation of the attachment of fins to the heat-sink base and the flatness of the surface.

Thermal Management Strategy

As described in this section, Xilinx relies on a multi-pronged approach with regards to the heat-dissipating potential of 7 series devices.

Cavity-Up Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the circuit board in the users system. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields. The substrate is made of a multi-layer BT (bismaleimide triazene) epoxy-based material. Power and GND pins are grouped together and signal pins are assigned to the perimeter for ease of routing on the board. The package is offered in a die-up format and contains a wire-bond device covered with a mold compound. As shown in the cross section of Figure 5-2, the BGA package contains a wire-bond die on a single-core printed circuit board with an overmold.

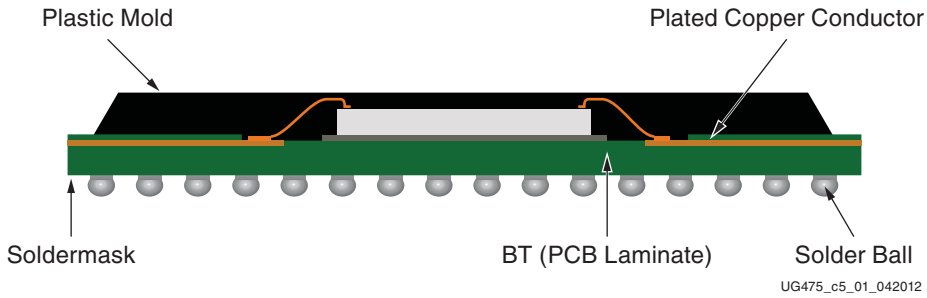


Figure 5-2: **Cavity-Up Ball Grid Array Package**

The key features/advantages of cavity-up BGA packages are:

- Low profile and small footprint
- Enhanced thermal performance
- Excellent board-level reliability

Wire-Bond Packages

Wire-bond packages meet the demands required by miniaturization while offering improved performance. Applications for wire-bond packages are targeted to portable and consumer products where board space is of utmost importance, miniaturization is a key requirement, and power consumption/dissipation must be low. By employing 7 series FPGA wire-bond packages, system designers can dramatically reduce board area requirements. Xilinx wire-bond packages are rigid BT-based substrates (see Figure 5-3).

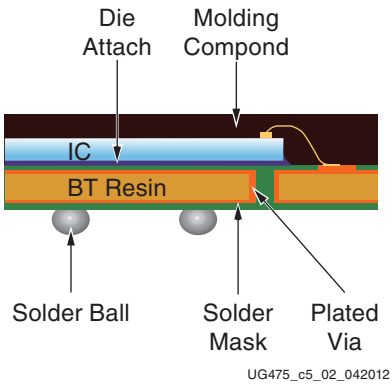


Figure 5-3: **Rigid BT-Based Substrate Wire-Bond Packages**

The key features/advantages of wire-bond packages are:

- An extremely small form factor which significantly reduces board area requirements for portable and wireless designs and PC add-in card applications.
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other small package types
- A very thin, light-weight package

Flip-Chip Packages

For larger 7 series devices, Xilinx offers the flip-chip BGA packages, which present a low thermal path. These packages incorporate a heat spreader with additional thermal interface material (TIM), as shown in Figure 5-4.

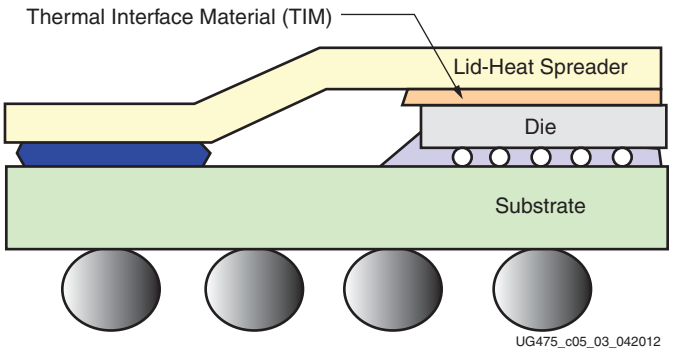


Figure 5-4: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all 7 series FPGA packages is typically less than 0.20°C/W. These packages deliver a low resistance platform for heat-sink applications.

A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity. These packages offer up to 20% lower θ_{JB} compared to previous flip-chip packages.

System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

Thermal Interface Material

When installing heat sinks for Xilinx FPGAs, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink. For optimum heat transfer, Xilinx recommends the use of thermal interface materials.

For lidless flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the lidless flip-chip BGA and lidded flip-chip BGA are different. Xilinx recommends a different type of thermal material for long-term use with each type of flip-chip BGA package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an FPGA unless there is good physical contact between the base of the heat sink and the top of the FPGA. The surfaces of both the heat sink and the FPGA silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the FPGA die and the heat sink.

The selection of the thermal interface (TIM) between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.

2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in step 1 and step 2, which are published in the data sheet of the thermal interface supplier.

Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase change material
- Thermal paste
- Thermal adhesives
- Thermal tape

Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- Thermal Conductivity of the Material
- Electrical Conductivity of the Material
- Spreading Characteristics of the Material
- Long-Term Stability and Reliability of the Materiall
- Ease of Application
- Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the FPGA die itself, but other elements on the FPGA or motherboard can be at risk if they become contaminated by the compound. For this reason, Xilinx does not recommend the use of electrically conductive thermal interface material.

Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the FPGA and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the FPGA. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on lidless devices.

Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Xilinx recommends that the applied pressure on the package be in the range of 20 to 40 PSI for optimum performance of the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements.

Xilinx recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See Figure 5-5.

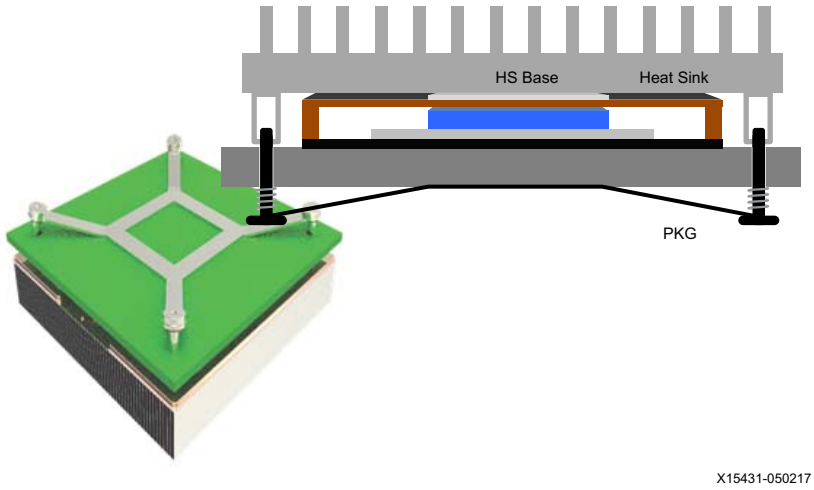


Figure 5-5: **Dynamic Mounting and Bracket Clips on Heat Sink Attachment**

Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

Note: Xilinx recommends that customers qualify their custom PCB assembly processes using package samples.

The primary phases of the reflow process are:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a plastic surface-mount component (PSMC) body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages (220°C for eutectic packages), and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

Sn/Pb Reflow Soldering

Figure 5-6 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

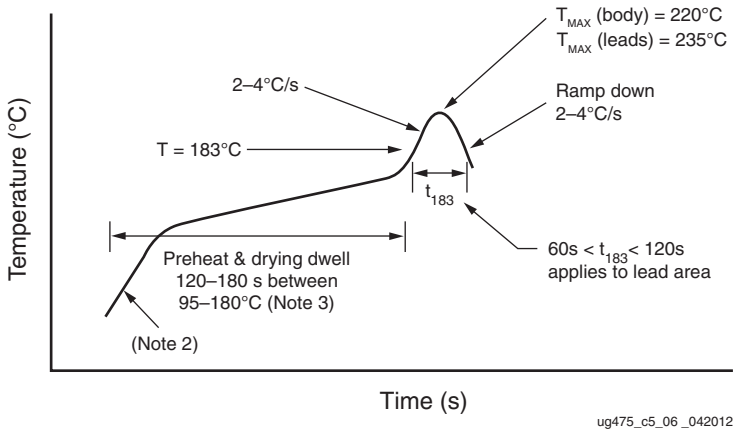


Figure 5-6: **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**

Notes for Figure 5-6:

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2–4°C/s
3. Preheat dwell 95–180°C for 120–180 seconds
4. IR reflow must be performed on dry packages

Pb-Free Reflow Soldering

Xilinx uses SnAgCu solder balls for BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

Xilinx does not recommend soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board.

Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

Table 5-2 and Figure 5-7 provide guidelines for profiling Pb-free solder reflow.

In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders (Figure 5-7). SAC305 alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. It might not be necessary to ramp to peak temperatures of 260°C and above. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to Table 5-2 for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 5-2: **Pb-Free Reflow Soldering Guidelines**

Profile Feature	Convection, IR/Convection
Ramp-up rate	2°C/s maximum
Preheat temperature 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak temperature (lead/ball)	235°C minimum, 245°C typical (depends on solder paste, board size, components mixture)
Peak temperature (body)	245°C–250°C, package body size dependent (reference Table 5-3)
Ramp-down rate	2°C/s maximum
Time 25°C to peak temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

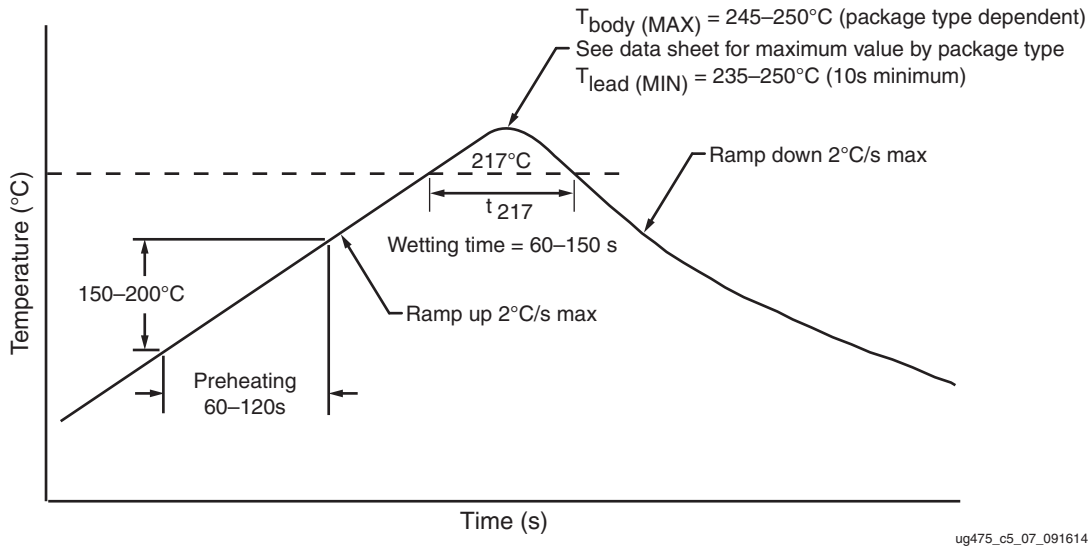


Figure 5-7: **Typical Conditions for Pb-Free Reflow Soldering**

Table 5-3: **Peak Package Reflow Body Temperature for Packages (Based on J-STD-020 Standard)**

Package		Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
BGA			
Wire Bond	CPGA196 FTGB196 CSGA225 CPG236 CPG238 CSG324 CSGA324 FTG256 FGG484 FGGA484 FGG676 FGGA676	260°C	3

Table 5-3: **Peak Package Reflow Body Temperature for Packages (Based on J-STD-020 Standard) *(Cont'd)***

Package		Peak Package Reflow Body Temperature	JEDEC Moisture Sensitivity Level (MSL)
Flip-Chip	FLG1925 FLG1926 FLG1928 FLG1930 FHG1761 FFG900/FFV900 FFG901/FFV901 FFG1156/FFV1156 FFG1157/FFV1157 FFG1158/FFV1158 FFG1761/FFV1761 FFG1926 FFG1927/FFV1927 FFG1928 FFG1930	245°C	4
	SBG484/SBV484 FBG484/FBV484 FBG676/FBV676 FBG900/FBV900 FFG676/FFV676	250°C	4
	RF676 RF900 RF1157 RF1158 RF1761 RF1930	225°C	4

Notes:

1. See specific 7 series device data sheets at Xilinx Documentation.

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages. Xilinx recommends a heating rate of less than 1°C/s during the preheating and soaking stages, in combination with a heating rate of not more than 2°C/s throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of

the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, Xilinx recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

Conformal Coating

Xilinx has no information about the reliability of flip-chip BGA packages on a board after exposure to conformal coating. Any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Note: Xilinx does not recommend using Toluene-based conformal coatings because they can weaken the lid adhesive used in Xilinx packages.

Package Marking

Introduction

All 7 series devices (Spartan®-7, Artix®-7, Kintex®-7, and Virtex®-7 FPGAs) have package top-markings similar to the examples shown in Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4. The markings are explained in Table 6-1.

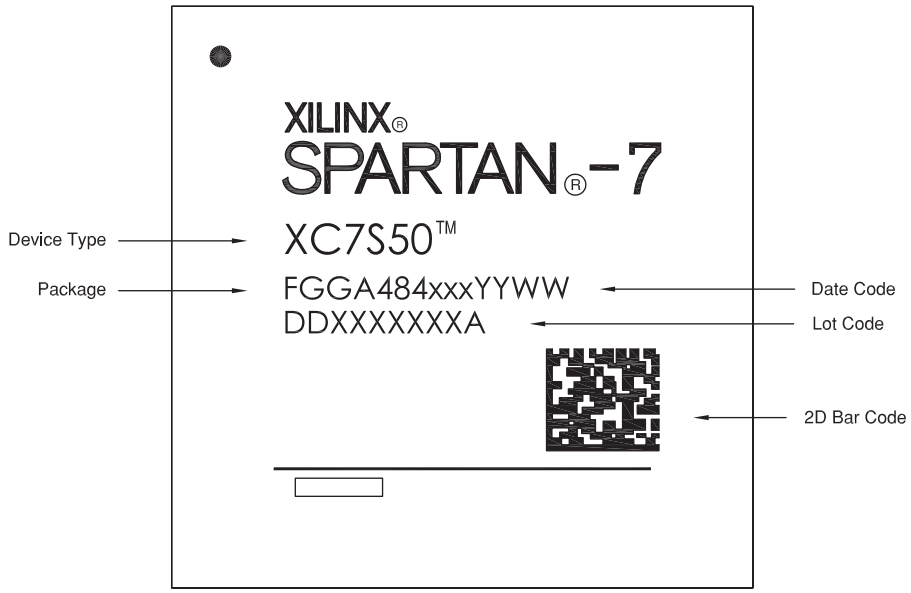


Figure 6-1: **Spartan-7 Device Package Marking**

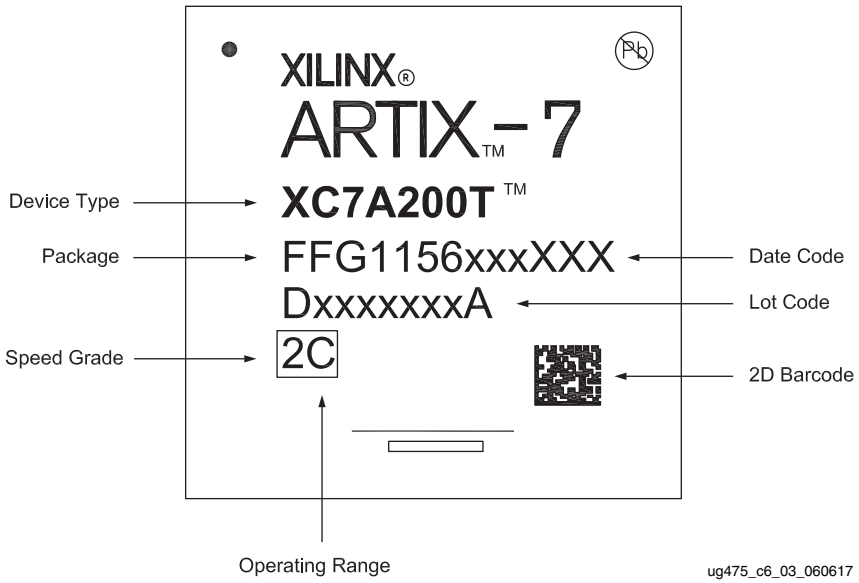


Figure 6-2: **Artix-7 Device Package Marking**

Figure 6-3: **Kintex-7 Device Package Marking**

Figure 6-4: **Virtex-7 Device Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Pb-free Character	For FFG, FBG, or SBG packages, a Pb-free character is marked in the upper right corner of the device to denote that the device is manufactured using a lead-free material set as described in *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages* (XCN16022).
Family Brand Logo	Device family name with trademark and trademark-registered status. This line is optional and could appear blank.
1st Line	Device type.
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A *G* (or V) in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: www.xilinx.com/pbfree.
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an *A* or an *M* if a stepping version does not exist.

Table 6-1: **Xilinx Device Marking Definition—Example *(Cont'd)***

Item	Definition	
4th Line	When marked, this line describes the device speed grade and temperature range. For more information on the ordering codes, see the *7 Series FPGAs Overview* (DS180). Other variations for the 4th line:	
	L2E	The *L2E* indicates a -2LE device. The -2LE speed grade offers reduced maximum power consumption. Artix-7 and Kintex-7 FPGAs are capable of operating at lower core voltage. The E is for the extended temperature operating range. For more information, see the specific device data sheets at: 7 series FPGAs.
	1C xxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C ES	The addition of an *ES* indicates an Engineering Sample.
	This line is not marked on some devices. Refer to the bar code for device speed grade and temperature range information.	
Bar Code	A device-specific bar code is marked on each device. Refer to the *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424).	

Packing and Shipping

Introduction

The 7 series devices are packed in trays (Table 7-1). Trays are used to pack most of Xilinx surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using anti-static material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C. The maximum operating temperature is 140°C.

Table 7-1: **Standard Device Counts per Tray and Box**

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
CPGA196	360	1800
FTGB196	126	630
CP/CPG236	240	1200
CPG238		
FT/FTG256	90	450
CSGA225	160	800
CS/CSG/CSGA324	126	630
CS/CSG325		
SB/SBG/SBV484	84	420
RS484		
FG/FGG/FGGA484	60	300
FB/FBG/FBV484		
RB484		
FG/FGG/FGGA676	40	200
FB/FBG/FBV676		
FF/FFG/FFV676		
RB676		
RF676		

Table 7-1: **Standard Device Counts per Tray and Box *(Cont'd)***

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
FB/FBG/FBV900	27	135
FF/FFG/FFV900		
FF/FFG/FFV901		
RF900		
FF/FFG/FFV1156	24	120
FF/FFG/FFV1157		
RF1157		
FF/FFG/FFV1158		
RF1158		
FF/FFG/FFV1761	12	60
RF1761	12	36
FHG1761	12	36
FL/FLG1925	12	36
FF/FFG1926		
FL/FLG1926		
FF/FFG/FFV1927		
FF/FFG1928		
FL/FLG1928		
FF/FFG1930	12	36
FL/FLG1930		
RF1930		

Recommended PCB Design Rules for BGA Packages

BGA Packages

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure A-1 and summarized in Table A-1 for both 0.8 mm and 1.0 mm pitch packages. For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure A-1. An example of an NSMD PCB pad solder joint is shown in Figure A-2. It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability.

The space between the NSMD pad and the solder mask as well as the actual signal trace widths and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

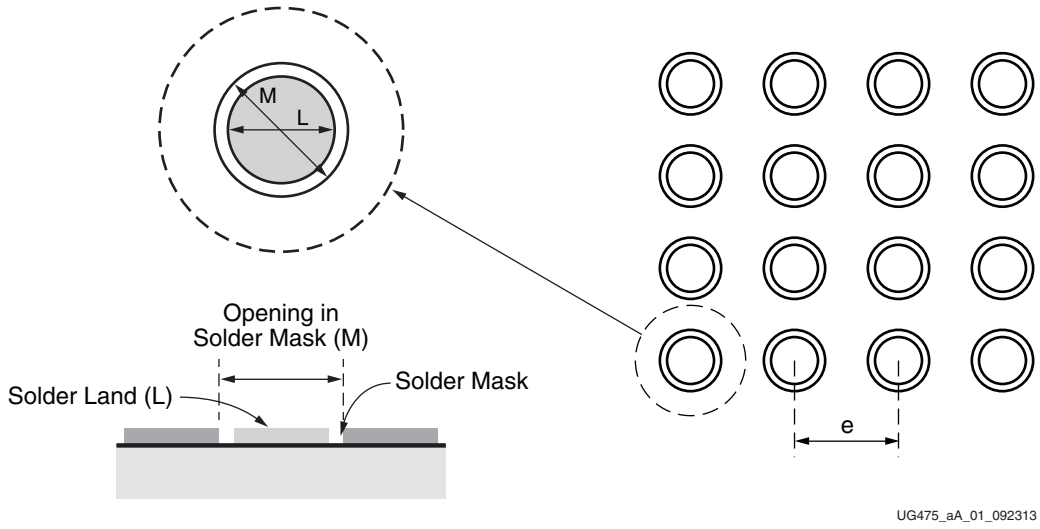


Figure A-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

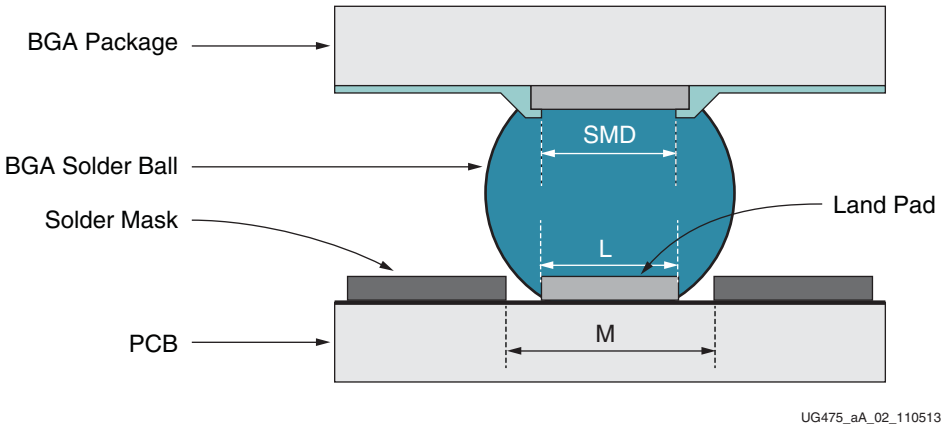


Figure A-2: **Example of an NSMD PCB Pad Solder Joint**

Table A-1: **BGA Package Design Rules**

Packages	0.5 mm Pitch	0.8 mm Pitch	1.0 mm Pitch		
	CPG	SB/SBG/SBV CS/CSG CPGA	FF/FFG/FFV, FB/FBG/FBV, FH/FHG, FL/FLG, RF/RB/RS	FG/FGG	FT/FTG
Design Rule	**Dimensions in mm (mils)**				
Package land pad opening (SMD)	0.275 mm (10.8 mils)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)	0.50 mm (19.7 mils)	0.40 mm (15.7 mils)
Maximum PCB solder land (L) diameter	0.275 mm (10.8 mils)	0.40 mm (15.7 mils)	0.53 mm (20.9 mils)	0.50 mm (19.7 mils)	0.40 mm (15.7 mils)
Opening in PCB solder mask (M) diameter	0.375 mm (14.76 mils)	0.50 mm (19.7 mils)	0.63 mm (24.8 mils)	0.60 mm (23.6 mils)	0.50 mm (19.7 mils)
Solder ball land pitch (e)	0.50 mm (19.7 mils)	0.80 mm (31.5 mils)	1.00 mm (39.4 mils)	1.00 mm (39.4 mils)	1.00 mm (39.4 mils)

Notes:

1. Controlling dimension in mm.

Heat Sink Guidelines for Lidless Flip-Chip Packages

Heat Sink Attachments for Lidless Flip-chip BGA (FB/FBG/FBV and SB/SBG/SBV)

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for lidless flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure B-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

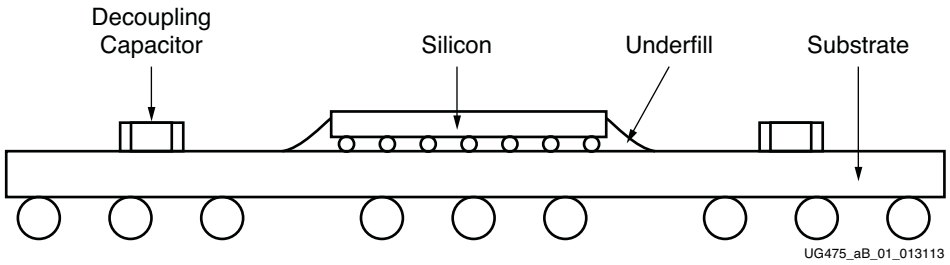


Figure B-1: **Cross Section of Lidless Flip-chip BGA**

Types of Heat Sink Attachments

There are six main methods for heat sink attachment. Table B-1 lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue (epoxy)
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

Table B-1: **Heat Sink Attachment Methods**

Attachment Method	Advantages	Disadvantages
Thermal tape	• Generally easy to attach and is inexpensive. • Lowest cost approach for aluminum heat sink attachment. • No additional space required on the PCB.	• The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly. • Because of the small contact area, the tape might not provide sufficient bond strength. • Tape is a moderate to low thermal conductor that could affect the thermal performance.
Thermally conductive adhesive or glue	• Outstanding mechanical adhesion. • Fairly inexpensive, costs a little more than tape. • No additional space required on the PCB.	• Adhesive application process is challenging and it is difficult to control the amount of adhesive to use. • Difficult to rework. • Because of the small contact area, the adhesive might not provide sufficient bond strength.
Wire form Z-clips	• It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary. • Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device). • It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance.	• Requires additional space on the PCB for anchor locations.

Table B-1: **Heat Sink Attachment Methods *(Cont'd)***

Attachment Method	Advantages	Disadvantages
Plastic clip-ons	• Suitable for designs where space on the PCB is limited. • Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board. • Can provide a strong enough mechanical attachment to pass shock and vibration test.	• Needs a keep out area around the silicon devices to use the clip. • Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.
Threaded stand-offs (PEMs) and compression springs	• Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis. • Suitable for high mass heat sinks. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Holes are required in the PCB taking valuable space that can be used for trace lines. • Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.
Push-pins and compression springs	• Provides a stable attachment to a heat source and transfers load to the PCB. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Requires additional space on the PCB for push-pin locations.

Heat Sink Attachment

Component Pick-up Tool Consideration

For pick-and-place machines to place lidless flip-chip BGAs onto PCBs, Xilinx recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure B-2).

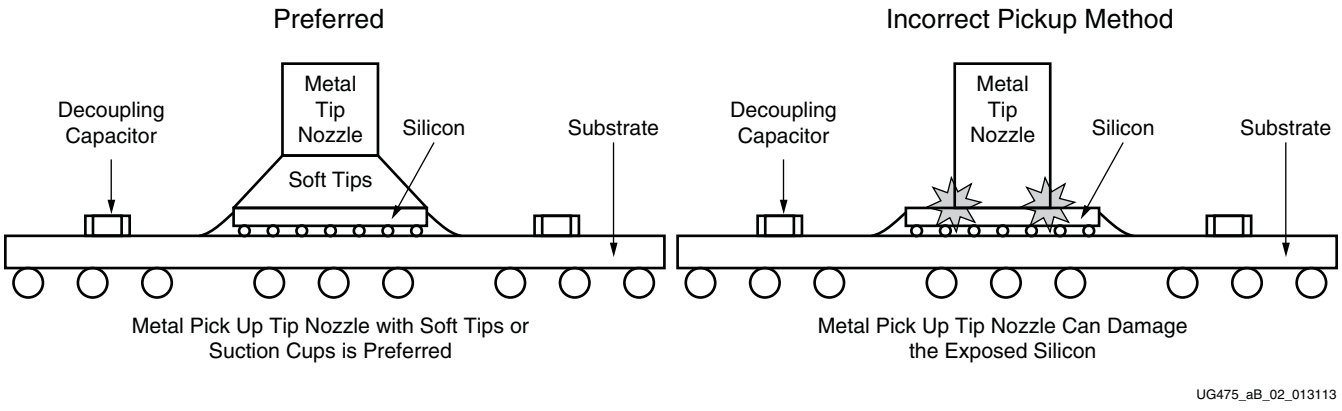


Figure B-2: **Recommended Method For Using Pick-up Tools**

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the lidless package, the factors in Table B-2 must be carefully considered (see Figure B-3).

Table B-2: **Heat Sink Attachment Considerations**

Consideration(s)	Effect(s)	Recommendation(s)
In heat sink attach process, what factors can cause damage to the expose die and passive capacitors?	• Uneven heat sink placement • Uneven TIM thickness • Uneven force applied when placing heat sink placement	• Even heat sink placement • Even TIM thickness • Even force applied when placing heat sink placement
Does the heat sink tilt or tip the post attachment?	Uneven heat sink placement will damage the silicon and can cause field failures.	• Careful handling not to contact the heat sink with the post attachment. • Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.

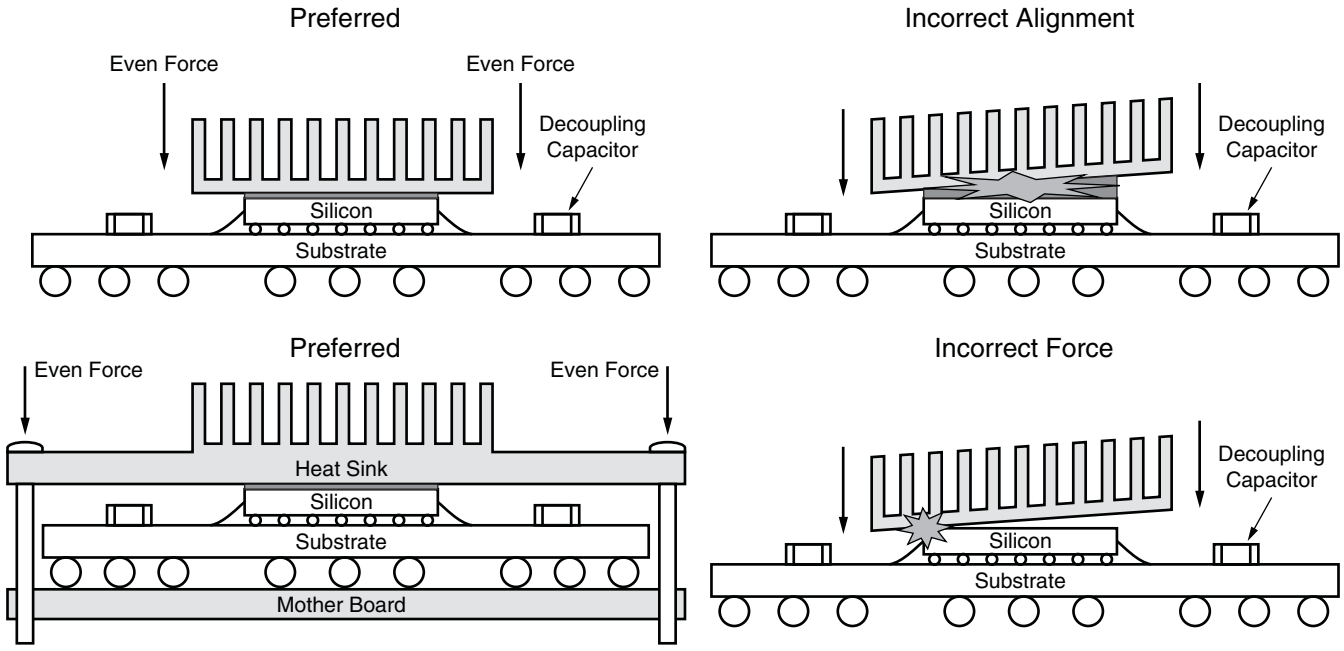


Figure B-3: **Recommended Application of Heat Sink**

Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

   Note: Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

   Note: The epoxy curing temperature and time is based on manufacturer's specifications.

Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

   Note: The thermal adhesive tape hold time is based on manufacturer's specifications.

Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the FPGA needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

   Note: The jig or fixture needs to account for the push pin depth of the heat sink.

2. PCM tape, cut to the size of the heat sink, os applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.

3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

   Note: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The following websites contain additional information on heat management and contact information.

- Wakefield: www.wakefield-vette.com
- Aavid: www.aavidthermalloy.com
- Advanced Thermal Solutions: www.qats.com
- CTS: www.ctscorp.com
- Radian Thermal Products: www.radianheatsinks.com
- Thermo Cool: www.thermocoolcorp.com

Refer to the following websites for interface material sources:

- Henkel: www.henkel.com
- Bergquist Company: www.bergquistcompany.com
- AOS Thermal Compound: www.aosco.com

- Chometrics: www.chomerics.com
- Kester: www.kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Mentor: Flotherm: http://www.mentor.com/products/mechanical/flomerics
- ANSYS Icepak: www.ansys.com

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