TTCrq Manual

P. Moreira*

CERN - EP/MIC, Geneva Switzerland

November 2004

Version 1.5

*Technical contact e-mail: Paulo.Moreira@cern.ch

SUMMARY OF CHANGES;

Version 1.5 — 2005-01-11

I2C terminations configuration table added. See page 11

Version 1.4 — 2004-11-17

TTCrq mezzanine board was redesigned to include an AC coupled resistive divider that reduces the power delivered to the quartz crystal. At the request of the users, as detailed below, some other modifications were introduced to the card. These modifications are fully compatible with the previous version; In particular, all the physical dimensions and connector positions have remained the same.

- Introduction of an AC couple resistive divider to reduce the power delivered to the QPLL quartz crystal.
- Introduction of a 2.5 V power pin on connector J2. See page 6.
- Possibility of internal terminating all of the LVDS signals. See page 6
- TTCrq configuration tables updated. See page 10

Version 1.3 — 2004-11-09

- Footprint of the TTCrq was define and is available through the CERN components library. See page 10.

Version 1.2 — 2004-02-27

- Section on terminating the LVDS clock signals added. See page 6.

RELATED DOCUMENTS

To understand the operation of the TTCrq mezzanine card, the user should be familiar with the functionality of the TTCrx and the QPLL. Documentation for these two devices can be found at the following web addresses:

TTCrx: http://www.cern.ch/TTC/intro.htmll

QPLL: http://www.cern.ch/proj-qpll

Note: updates of this document can be obtained from the QPLL site.

INTRODUCTION

A mezzanine card (the **TTCrq**) was designed by the CERN microelectronics group to replace the TTCrm. The device is supported by the CERN Electronics Pool (EP-ESS Group). For further information on support please refer to the EP-ESS Croup TTC support web page: http://ess.web.cern.ch/ESS/TTCsupport .

The TTCrq can be mounted on a standard VME unit without imposing restrictions on the space between two VME modules. The card contains a TTCrx, a QPLL with its associated crystal and a TrueLight pin-preamplifier (TRR-1B43-000).

The TTCrq mezzanine card is backward-compatible with the TTCrm. That means that the existing electrical connectors (J1 and J2) are kept in the same physical positions with the same pinout as in the TTCrm. An additional connector (J3) is added to the card located on the PCB side opposite to the optical connector side as represented in Figure 1. J3 is a 26-pin connector. (VME board areas under the dotted/shadowed regions (top view drawing) should remain free on the mother board for tool insertion during board removal.)

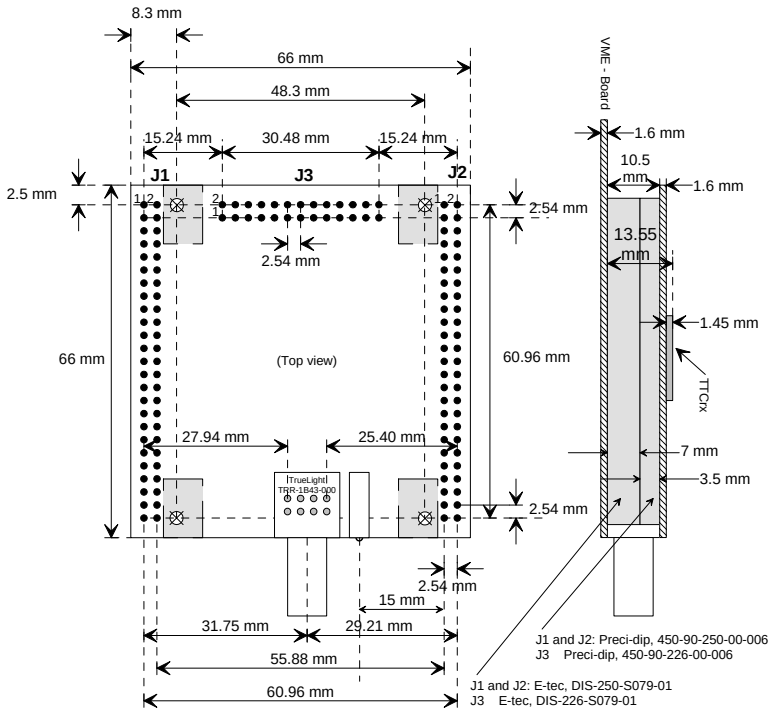


Figure 1 TTCrx and QPLL mezzanine card

To reduce the module height the optical receiver is mounted under the card on the same PCB side as the electrical connectors. The optical connector was moved to the

bottom side of the PCB but its distance to the J1 and J2 connectors remained unchanged (please see details in Figure 1).

As shown in Fig. 1, the overall height of the components on the mounted TTCrq mezzanine card is 13.55 mm above the components side of the VME motherboard. To ensure compliance with VMEbus Rule 7.14, assembled VME modules should be measured to verify that the sum of TTCrm component height and board warpage does not exceed 13.71 mm.

The 13.71 mm limit allows a guaranteed 2.44 mm clearance between the TTCrx and the longest component leads on the adjacent VME board. More importantly for the cooling airflow, it allows a nominal 4.91 mm space to an unwarped adjacent VMEboard. According to VMEbus Observation 7.11, this space allows adequate airflow for cooling. However, designers should avoid putting high-dissipation components on the VME board underneath the mezzanine board, as the horizontal orientation of the connectors is likely to restrict airflow for cooling.

CIRCUIT

A block diagram of the mezzanine card is represented in Figure 2. The card contains a pin-preamplifier (the Truelight TRR-1B43-000), a TTCrx, a QPLL, a PROM and a bank of SMD pull-up/pull-down resistors and jumpers to setup the TTCrx address and operation modes. All of the QPLL pins (with the exception of the crystal dedicated pins and the VCXO decoupling capacitor pin) are accessible through the J3 connector. The QPLL input can be taken either from the J3 connector (external source) or from one of the TTCrx clock outputs (Clock40, Clock40Des1 or Clock40Des2). When using the QPLL with an external source the reference clock signal can be either LVDS or CMOS. If necessary, the QPLL clock signal (after LVDS to CMOS conversion) can be routed to the Clock40Des1 signal on the J1 connector. This allows using the TTCrq on boards that were designed to receive the TTCrm card while at same time profiting from the QPLL as a jitter filter.

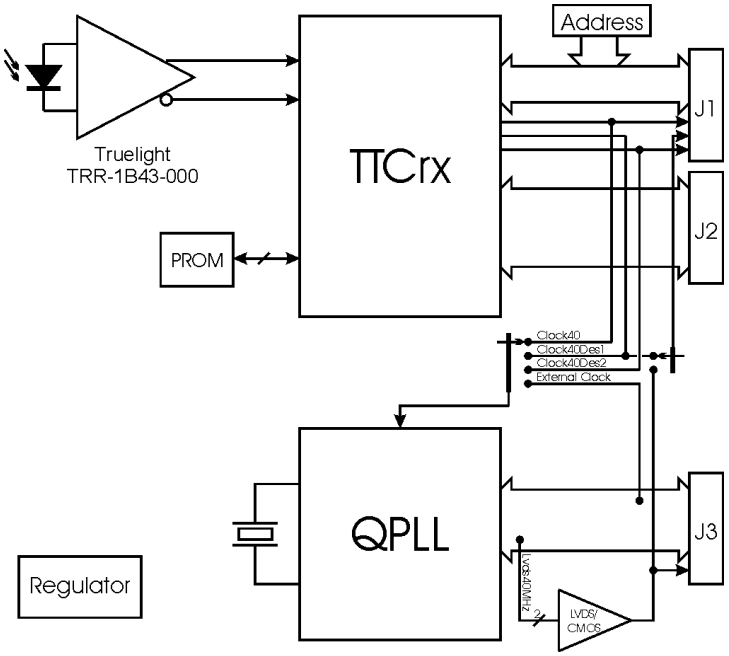


Figure 2 TTCrq block diagram

All the QPLL clock signals are available in the J3 connector as LVDS signals. Additionally, the 40 MHz clock output is also present as a CMOS output.

Users of the TTCrq should be aware that due to limited lock range of the QPLL (≈ ±160 ppm), high precision clock references centred around the LHC clock frequency are required to guaranty lock during laboratory test.

Power supply

Three independent power connections are present on the board: one dedicated to the pin-preamplifier, another to the QPLL and the third to the remaining circuitry.

The TTCrx, the PROM and the LVDS/CMOS level converter can be either powered from 3.3 or 5 V. The choice of this voltage will set the CMOS levels of all the TTCrx signals as well as that of the 40 MHz CMOS clock output in the J3 connector. Notice however, that the pin-preamplifier has to be powered from a 5V power supply.

The power supply for the QPLL is obtained from the TTCrx power using a 2.5V low dropout regulator. Alternatively, it is possible to provide the QPLL power through pin 39 of connector J2. In this case the internal regulator should not be present in the circuit and the resistor R59 (0 Ω) must be mounted.

Termination resistors

When the LVDS clock signals are to be carried out of the board termination resistors (100 Ω) must be provided external to the board. These resistors should be located at the end of the transmission lines that carry the signals. The transmission lines should be designed to have 100 Ω differential characteristic impedance.

Optionally all LVDS signals (input and outputs) can be terminated on the board. In principle, the LVDS signals that are not in use do not require a termination resistor. However, by default, the 40 MHz LVDS clock signal is terminated on the board for proper operation of the internal LVDS to CMOS level translator. If this signal is to be used outside the mezzanine card, the onboard termination should be removed and an external termination resistor must be provided.

TTCrq pin assignments:

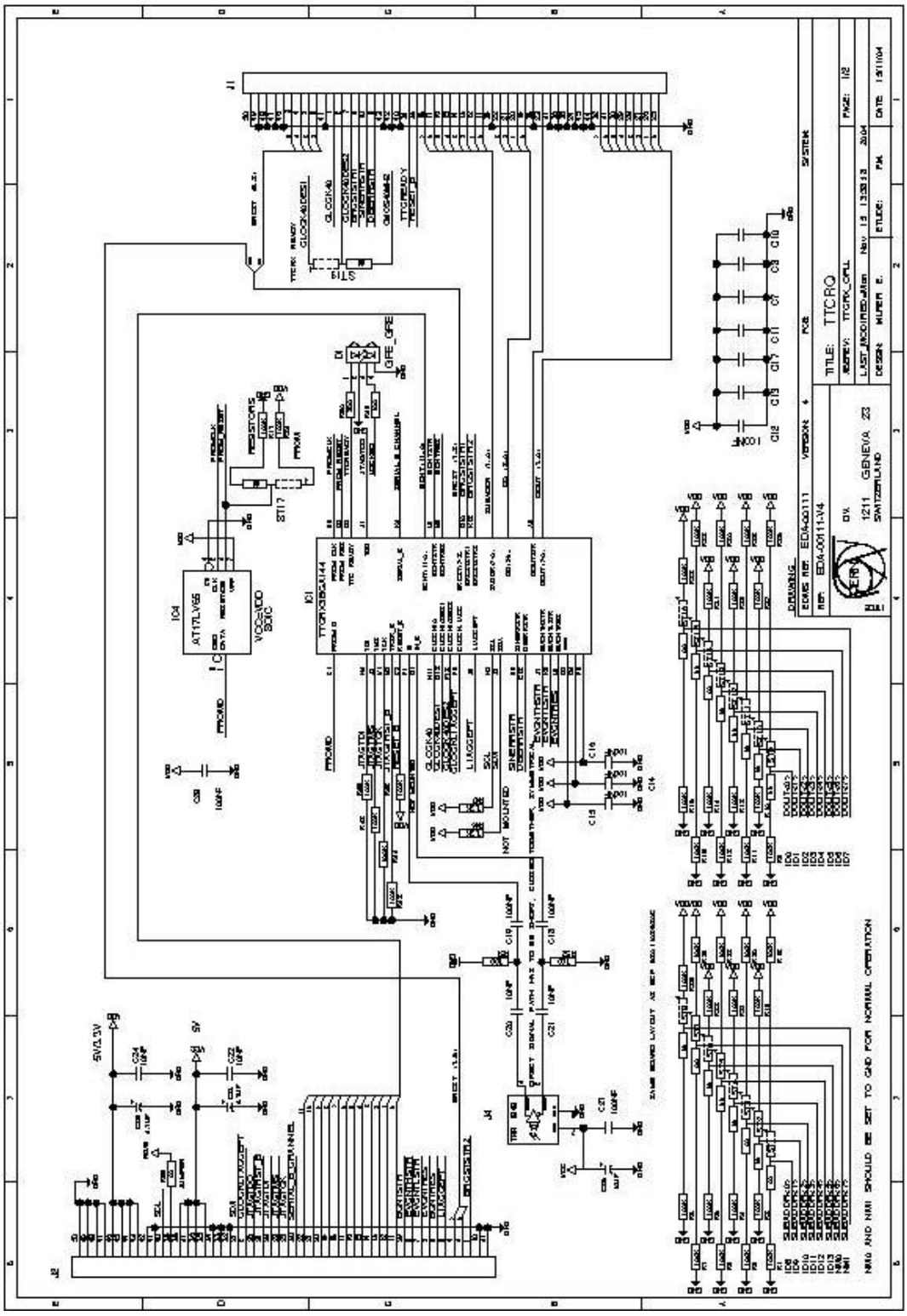
J1 Connector		J2 Connector		J3 Connector	
Pin Number	**Signal Name**	**Pin Number**	**Signal Name**	**Pin Number**	**Signal Name**
1	Clock40	1	BrcstStr2	1	f_0Select<0>
2	Clock40Des1	2	ClockL1Accept	2	mode
3	Brcst<5>	3	Brcst<6>	3	inLVDS+
4	Brcst<4>	4	Brcst<7>	4	inLVDS-
5	Brcst<3>	5	EvCntRes	5	gnd
6	Brcst<2>	6	L1Accept	6	externalClock
7	Clock40Des2	7	EvCntLStr	7	autoRestart
8	BrcstStr1	8	EvCntHStr	8	externalControl
9	DbErrStr	9	BcntRes	9	f_0Select<3>
10	SinErrStr	10	GND	10	~reset
11	SubAddr<0>	11	BCnt<0>	11	locked
12	SubAddr<1>	12	BCnt<1>	12	error
13	SubAddr<2>	13	BCnt<2>	13	gnd
14	SubAddr<3>	14	BCnt<3>	14	lvds80MHz-
15	SubAddr<4>	15	BCnt<4>	15	lvds80MHz+
16	SubAddr<5>	16	BCnt<5>	16	gnd

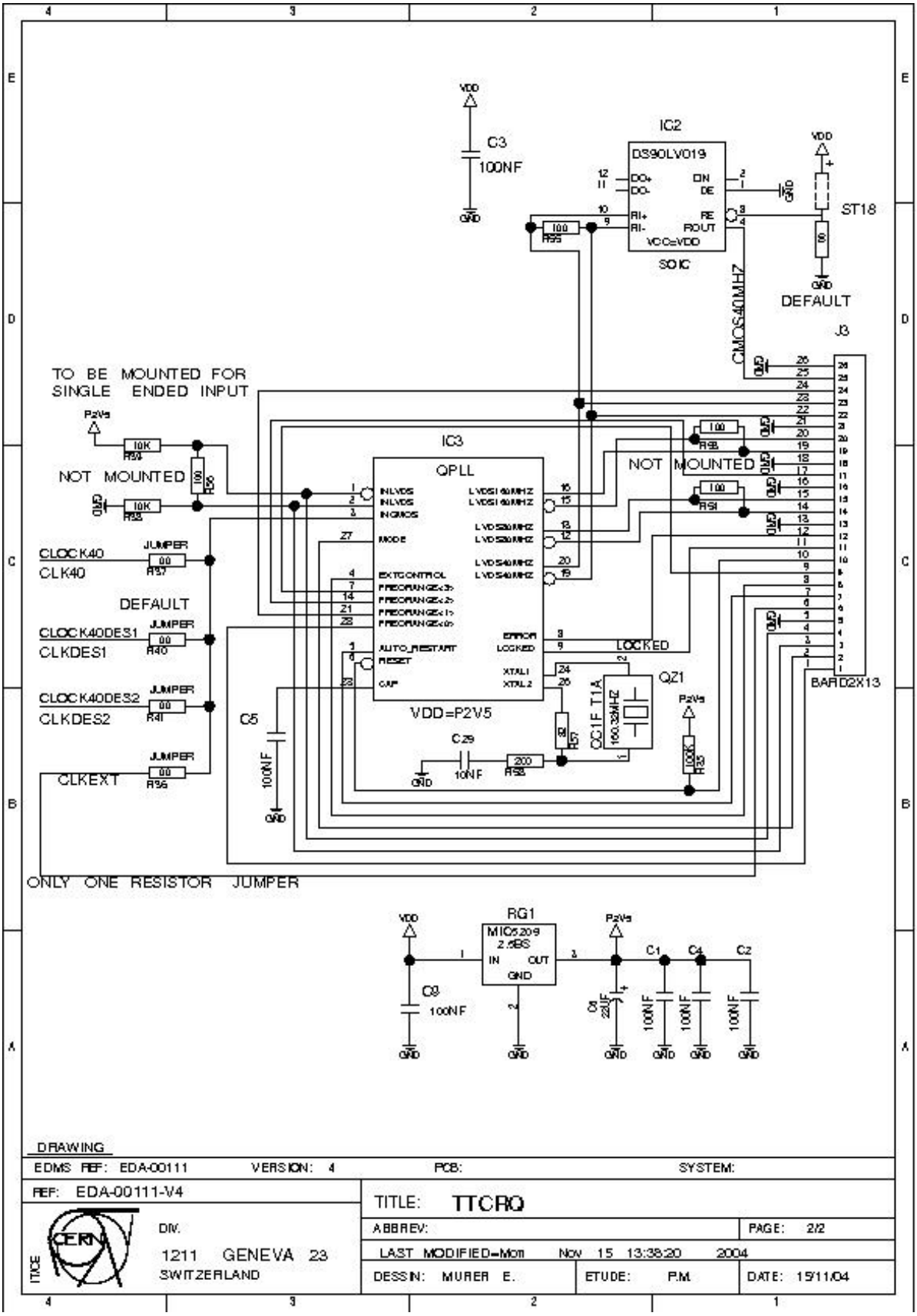
17	SubAddr<6>	17	BCnt<6>	17	f_0Select<2>
18	SubAddr<7>	18	BCnt<7>	18	gnd
19	DQ<0>	19	BCnt<8>	19	lvds160MHz+
20	DQ<1>	20	BCnt<9>	20	lvds160MHz-
21	DQ<2>	21	BCnt<10>	21	gnd
22	DQ<3>	22	BCnt<11>	22	lvds40MHz-
23	DoutStr	23	JTAGTMS	23	lvds40MHz+
24	GND	24	JTAGTRST_b	24	f_0Select<1>
25	Dout<0>	25	JTAGTCK	25	cmos40MHz
26	Dout<1>	26	JTAGTDO	26	gnd
27	Dout<2>	27	SDA		
28	Dout<3>	28	JTAGTDI		
29	Dout<4>	29	BCntStr		
30	Dout<5>	30	Serial_B_Channel		
31	Dout<6>	31	GND		
32	Dout<7>	32	GND		
33	Reset_b	33	GND		
34	TTCReady	34	GND		
35	GND	35	PIN_Preamp_VCC		
36	GND	36	PIN_Preamp_VCC		
37	GND	37	PIN_Preamp_VCC		
38	GND	38	PIN_Preamp_VCC		
39	GND	39	QPLL power (2.5 V)		
40	GND	40	SCL		
41	GND	41	GND		
42	GND	42	GND		
43	GND	43	TTCrx_VDD		
44	GND	44	TTCrx_VDD		
45	GND	45	TTCrx_VDD		
46	GND	46	TTCrx_VDD		
47	GND	47	GND		
48	GND	48	GND		
49	GND	49	GND		
50	GND	50	GND		

TTCrq schematics

Note: These schematics can also be obtained for the QPLL site:

http://www.cern.ch/proj-qpll




IC2
DS90LV019
C3
100NF
ST18
DEFAULT
CMOS40MHZ
J3
BARD2X13
TO BE MOUNTED FOR
SINGLE ENDED INPUT
NOT MOUNTED
NOT MOUNTED
IC3
QPLL
CLOCK40
CLK40
DEFAULT
CLOCK40DES1
CLKDES1
CLOCK40DES2
CLKDES2
CLKEXT
JUMPER
C5
100NF
C29
10NF
QZ1
VDD=P2V5
LOCKED
ONLY ONE RESISTOR JUMPER
RG1
MIC5209
2.5BS
C9
100NF
C1
C4
C2
DRAWING
EDMS REF: EDA-00111
VERSION: 4
PCB:
SYSTEM:
REF: EDA-00111-V4
TITLE: TTCRQ
ABBREV:
PAGE: 2/2
LAST MODIFIED=Mon Nov 15 13:38:20 2004
DESSIN: MURER E.
ETUDE: P.M.
DATE: 15/11/04
DIV.
1211 GENEVA 23
SWITZERLAND
ITCE

TTCrq footprint

For layout purposes a footprint of the TTCrq was defined and is available for Allegro (Cadence) through the CERN components library. The library name is CNSPECIAL and the symbol name is TTCRQ_MEZZ.

TTCrq configuration

The TTCrq is setup by soldering SMD jumpers and resistors on the appropriate locations. For each jumper two positions are possible, these are indicated in the PCB silk layer by a “+” and a “-“ sign. The following tables describe the purpose of these jumpers and resistors and their default configurations:

ADRESS selection and Master modes

Jumper	+	-	Default	Function
ST1	PROM	Data bus	Not mounted	ID<8>
ST2	PROM	Data bus	Not mounted	ID<9>
ST3	PROM	Data bus	Not mounted	ID<10>
ST4	PROM	Data bus	Not mounted	ID<11>
ST5	PROM	Data bus	Not mounted	ID<12>
ST6	PROM	Data bus	Not mounted	ID<13>
ST7	PROM	Data bus	“-“	MN0 (No change allowed)
ST8	PROM	Data bus	“-“	MN1 (No change allowed)
ST9	PROM	Data bus	Not mounted	ID<0>
ST10	PROM	Data bus	Not mounted	ID<1>
ST11	PROM	Data bus	Not mounted	ID<2>
ST12	PROM	Data bus	Not mounted	ID<3>
ST13	PROM	Data bus	Not mounted	ID<4>
ST14	PROM	Data bus	Not mounted	ID<5>
ST15	PROM	Data bus	Not mounted	ID<6>
ST16	PROM	Data bus	Not mounted	ID<7>

PROM selection

Jumper	+	-	Default	Function
ST17	PROM	Data bus	“-“	TTCrx initialization method

J1 output clock selection

Jumper	+	-	Default	Function
ST19	TTCrx	QPLL	“-“	Clock source for clock pin 2 on J1

J3 CMOS clock output enable

Jumper	+	-	Default	Function
ST18	Disabled	Enabled	"-"	QPLL CMOS clock output enable

QPLL clock source selection

Resistor	Mounted	Value	Default	Function
R36	External	0 Ω	Not mounted	QPLL clock input[1,2,3]
R37	Clock40	0 Ω	Not mounted	QPLL clock input[1,2,3]
R38	Single ended clock input	10 kΩ	Mounted	Disables the LVDS clock input[2,3]
R39	Single ended clock input	10 kΩ	Mounted	Disables the LVDS clock input[2,3]
R40	Clock40Des1	0 Ω	Mounted	QPLL clock input[1,2,3]
R41	Clock40Des2	0 Ω	Not mounted	QPLL clock input[1,2,3]

Note 1: Only one of R36, R37, R40 and R41 can be mounted at a time.

Note2: To use the external LVDS clock input the resistors R36, R37, R38, R39, R40 and R41 must be all unmounted.

Note 3: to use the QPLL single ended input resistors R38 and R39 must be mounted.

J2 2.5V power

Resistor	Mounted	Value	Default	Function
R59	External Power	0 Ω	Not mounted	On board regulator provides the QPLL power[4]

Note 4: If the 2.5V power is provided from pin J2 – 39 the onboard regulator must not be assembled on the board.

I2C terminations

Resistor	Mounted	Value	Default	Function
R46	onboard termination	12 kΩ	Mounted	I2C SDA pull up
R47	onboard termination	12 kΩ	Mounted	I2C SCL pull up

LVDS terminations

Resistor	Mounted	Value	Default	Function
R53	onboard termination	100 Ω	Not mounted	LVDS 160 MHz clock output termination
R54	onboard termination	100 Ω	Not mounted	LVDS 80 MHz clock output termination
R55	onboard	100 Ω	Mounted	LVDS 40 MHz clock output

	termination			termination
R56	onboard termination	100 Ω	Not mounted	LVDS 40 MHz clock input termination

Timing

As illustrated in Figure 3, in the TTCrq, phase offsets exist between the reference clock fed to the QPLL and the QPLL clock signals. Since in the TTCrq the QPLL clock reference can be any of the TTCrx clocks (*Clock40*, *Clock40Des1* and *Clock40Des2*) in Figure 3 these signals are represented by the generic name of "*TTCrx Clock*". The timing of the signal "*Cmos40MHz*" depends not only on the QPLL but as well on the LVDS/CMOS translator. For further details on the timing of that device please see: http://cache.national.com/ds/DS/DS90LV019.pdf.

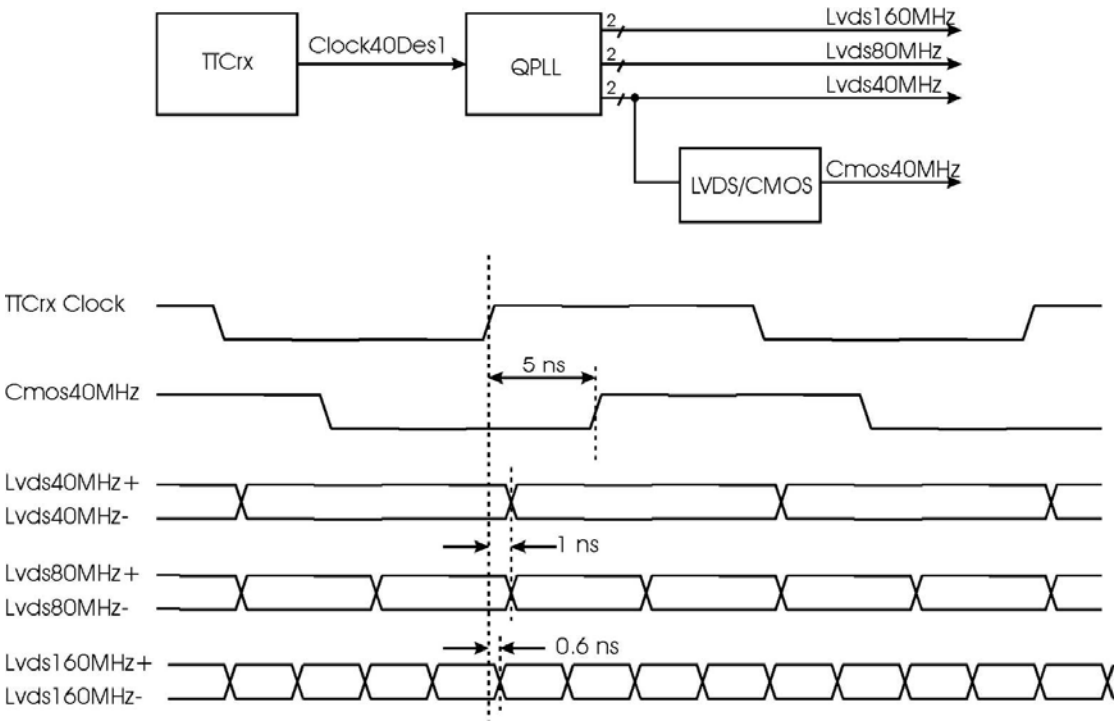


Figure 3 TTCrq timing