Irradiation Test of the Altera Programmable Devices at the CMS Muon Endcap Clock and Control Board

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Introduction

The Clock and Control Board (CCB) [1] is the main interface unit between Timing, Trigger and Control (TTC) System [2] of the CMS Experiment and the Cathode Strip Chamber (CSC) EMU peripheral electronics [3]. The CCB (Fig.1) is a 9U*400 mm VME board which carries a TTCrx [2] card and a mezzanine card with the Altera EPF10K100 PLD [4] and EPC2 serial EPROM [5]. The TTCrx card is based on radiation-hard ASIC designed at CERN that converts an optical data stream from the TTC system into parallel form (this board is not shown on Fig.1). The PLD performs all the main CCB functions. Its configuration information is stored in EPROM. The CCB will be located in the middle of the VME crate. 60 such crates for the whole CSC system will be mounted on the periphery of the return yoke of the CMS detector. The goal of our test was to determine how well the Altera PLD and EPROM are able to tolerate the radiation environment and the integrated dose expected in this area during 10 years of LHC operation. Specifically, the potential for Single Event Upsets (SEU) and Single Event Latch-ups (SEL) in these programmable CMOS devices due to the high flux of secondary neutrons is of concern. An important note is that both DUT are not qualified by the vendor for applications in a radiation environment.

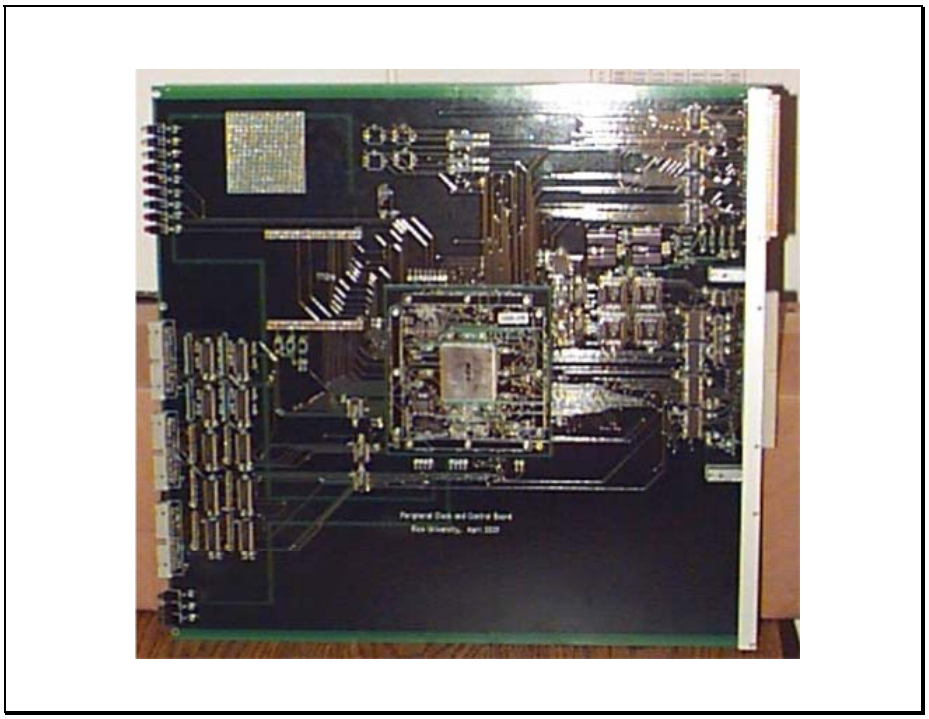

Fig.1. Clock and Control Board

1. Radiation Environment and Devices Under Test

Based on simulation results [6]-[7], the Total Ionizing Dose (TID) for the inner CSC chambers during 10 years of operation is below 10 kRad and the neutron fluence (for $E > 100$ KeV) is below 10^{12} cm^{-2}. On the periphery of the return yoke (where the CCB will be located) these numbers are approximately one order in magnitude less, including a safety factor of 3-5 [8]. The SEU cross-section is quite independent of the neutron energy above about 100 MeV. While the expected energy distribution at the LHC has a sizable population below this level, we chose a convenient beam energy of 63 MeV to simulate the effect of the neutron environment at the LHC. Our tests were conducted with a 63 MeV proton beam at the Crocker Nuclear Laboratory cyclotron at the University of California, Davis (UCD).

The main Device Under Test (DUT) is Altera EPF10K100ABC356 PLD based on Altera FLEX architecture that uses look-up tables (LUT) to implement logic functions and static RAM configuration elements that require configuration data to be loaded every time the PLD powers up. This PLD is fabricated using 0.30 um CMOS process, has ~100K typical gates and packaged into 356-pin Ball Grid Array package. A configuration file (~147K bytes in size) is stored in the EPC2 that is our second DUT. EPC2 itself has a reprogrammable (over JTAG interface) FLASH memory. At any time an EPC2 content can be read back to PC over JTAG and checked by Altera Max+Plus II software against the original file. Unfortunately, the read back feature for the PLD is not supported by Altera, so there is no direct way to check how many configuration elements are corrupted during irradiation.

2. Experimental Setup and Designs Under Test

The CCB is generally a complex command decoder operating at 40Mhz. It decodes various TTC and VME signals and transmits decoded commands to modules in a peripheral VME crate over custom backplane. These functions utilize almost all PLD input/output pins and require ~26% of the PLD internal resources. The most important test would be to check the PLD functioning in a dynamic mode at 40Mhz operating frequency. Since neither TTC, nor VME systems were involved in our irradiation test, a special circuitry was added to PLD firmware. This circuitry (Fig.2) comprises two 16-bit pseudo-random bit stream (PRBS) generators, two registered pipelines (~100-bit deep), comparator and error detection scheme, all running at 40Mhz from the on-board quartz oscillator. These elements occupy ~65% of the PLD resources. They are very sensitive to SEU. In case of any SEU in a switching flip-flop (FF) chain an error detection scheme detects error and generates 25-ns pulse coming out of the CCB board. This signal can be counted by the external counter. Upon error detection both PRBS generators and pipeline chains are automatically set into initial state and the scheme is ready to detect another SEU.

During irradiation the CCB board was positioned perpendicular to the beam which was focused to irradiate only the PLD or EPROM at a time. Since the distance between irradiation area and control room is ~15m, we have developed an extender of the JTAG cable that connected our mezzanine card and the Altera ByteBlaster [9] plugged into PC's parallel port. All JTAG signals as well as an "Error" signal from the CCB were transmitted using LVDS logic levels. From the Altera Max+Plus II environment we were able to check remotely a content of the EPROM, reprogram it (if necessary) with a new design file and reconfigure the PLD from EPROM upon special JTAG command. An Agilent 53132A Universal Counter was used to count errors.

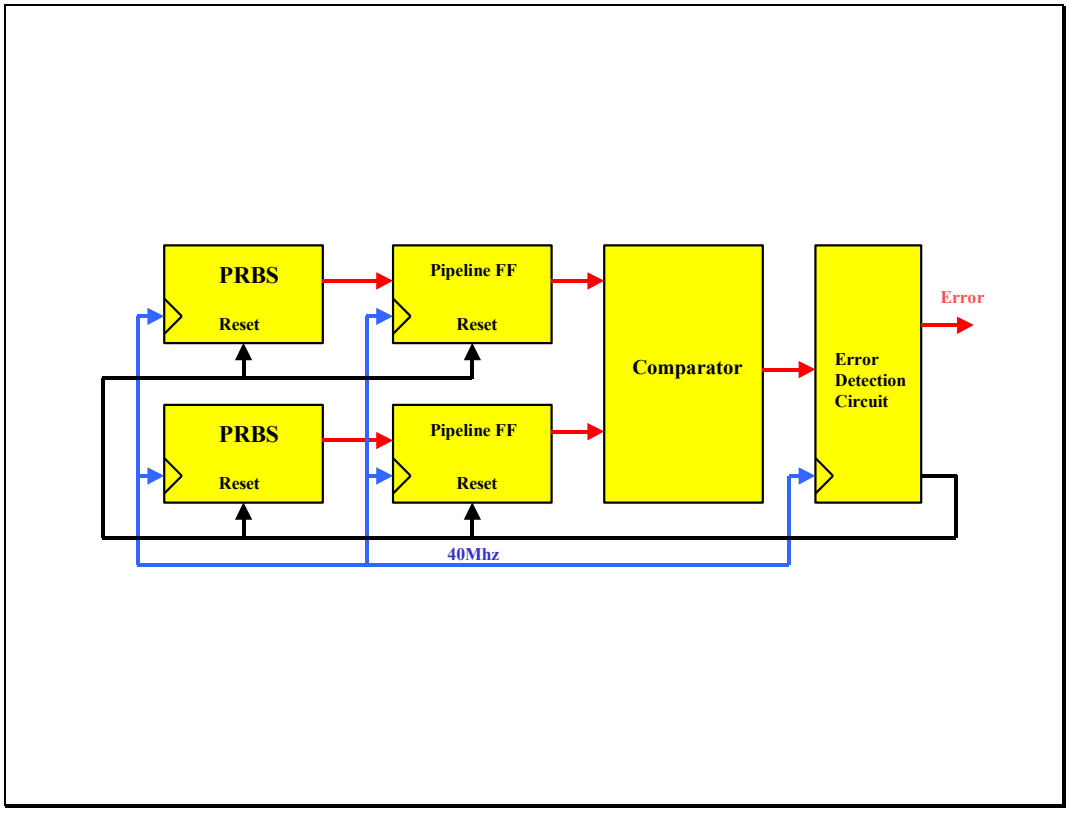

Fig.2. Block Diagram of the Test Design

Two common types of SEU can be distinguished for the SRAM-based programmable devices: SEU due to errors in a user's logic and SEU in a configuration data. Measurement of errors in user's logic in a dynamic mode is especially important, but the resulting cross-section is design dependent. Errors of this type for our design can be unambiguously linked to events when an external counter increments by 1. This corresponds to SEU in a flip-flop chain or PRBS generators running at 40Mhz. Errors of the second type can be associated with those events when an external counter starts counting continuously. This could be, for example, a sign of broken pipeline chain. Such errors are not recoverable until the PLD is reconfigured. A separate type of upsets related to control logic of the programmable device (JTAG controller, configuration control logic etc) are architectural upsets. Usually they are less frequent and can be measured often only indirectly. Our simple setup and design did not allow to distinguish these errors from errors in a configuration memory.

3. Results of the Irradiation Test

For the 63 MeV proton beam at UC Davis facility, 1 Rad = 8×10^6 protons/cm^{-2}. The first irradiation procedure for PLD was to irradiate it with a current of 20 pA for a dose of up to 1 kRad. Assuming strong isospin symmetry for SEU's, 1 kRad is equivalent to 8×10^9 cm^{-2} neutron fluence. 20 errors of the second type were observed for the design described above, with the average dose needed to get an error of ~50 Rad. This number corresponds to **cross section of SEU of 2.5×10^{-9} cm^2**. All observed errors did not produce latch-ups and were recoverable by reconfiguration from EPROM. This result is consistent with the one obtained during irradiation test of the ALCT card [10] designed at UCLA. Comparing to results reported by OSU group [11],

the cross section of SEU for Altera EPF10K100 PLD **is about one order of magnitude larger** than ones obtained for the selected Xilinx Spartan and Virtex FPGA.

The second irradiation procedure was done with modified firmware, when the depth of registered pipeline was reduced to only one bit. Such a circuitry occupies only 1% of the PLD resources. The device was irradiated with a beam current of 100 pA up to a dose of 2 kRad. Only one error of the first type (self-recoverable) was observed at 1.1 kRad. Comparing results of the first and second procedures and taking into account the fact that the measured cross sections of two different designs in a dynamic mode (ours and ALCT [10]) are very close, we would conclude that SEU in a SRAM configuration memory or embedded LUT that implement combinational logic is the dominant effect during irradiation of the Altera EPF10K100 PLD. This is in agreement with an independent irradiation test reported in [12].

During the next irradiation test the content of our second DUT, EPC2 was periodically read back and checked against the original file. No errors were observed up to a total dose of 25.6 kRad. At 25.6 kRad, the error check showed 145 mismatches in FLASH memory (0.1%) and at 25.8 kRad – 74505 mismatches (70.3%). This result is also consistent with [10] and close to the dose when errors were observed for Xilinx EPROM [11]. Above 26 kRad the device stopped responding over JTAG.

Assuming that the PLD is the only source of SEU on a CCB, the worst case SEU rate would be **0.5×10^{-5}** per second (2.5×10^{-9} cm^2 x 10^{11} neutrons/cm^{-2} / 5×10^7 sec), or one SEU in about 60 hours. For 60 crates in a system, this means approximately one error every hour of operation at full luminosity.

Conclusion

From the results of our test, an EPC2 EPROM appears to be radiation resistant up to 25.6 kRad and can be used on the periphery of the CSC EMU system. Altera PLD showed to be relatively sensitive to radiation. The damage of the configuration data seems to be the primary effect during irradiation. One way to reduce a malfunctioning because of this would be to reconfigure PLD from EPROM periodically. Another technique, a Triple Module Redundancy (TMR), could limit the impact of SEU in a user's flip-flop and combinatorial logic. Both TMR and periodical reconfiguration may be efficiently used together. In case of the CSC EMU system a command for such a reconfiguration would arrive to CCB from the TTC system. This means that the CCB will not be able to operate properly during the reconfiguration (which takes 120 milliseconds), i.e. the reliability of the whole peripheral crate could be compromised. An alternative and more favorable solution would be to eliminate the possibility of configuration errors and design the main CCB logic inside one-time programmable device, for example, anti-fuse FPGA. Such a change would require a redesign of the mezzanine card only. Our current preference is Actel A54SX32 anti-fuse FPGA. This device was extensively tested by several groups for HEP and airspace applications (see, for example, [13]-[14]). The cross section of SEU, reported in [14] is below 2.9×10^{-12} cm^2, or about three orders in magnitude less than for Altera 10K100 PLD and two orders in magnitude less than for selected Xilinx FPGAs. The frequency of SEU based on estimate [14] per one CCB would be about one SEU in 5 years of operation, or one SEU in one month of LHC operation at full luminosity per system comprising 60 CCBs. The main disadvantage of this approach it that the mezzanine card with anti-fuse device won't be programmable.

References

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