Jitter Measurements with a TTCrx ASIC

Rice University

March 18, 2002

1. Introduction

Two TTCrx mezzanine cards, (an ECP 680-1102-610B with an old TTCrx ASIC and an ECP680-1102-630C with a new TTCrx ASIC 3.1 (CERN 12/2001) [1]) were tested. The goal of the test was to measure TTCrx mezzanine card Clock40Des1 output jitter and determine its influence on data transmission thru Texas Instruments TLK2501 gigabit transceivers at 80.00 Mhz.

2. Testing Setup and Jitter Measurements

The TTCrx mezzanine card was installed on the Clock and Control Board [2] and connected to a TTCvx module via a 100 m optical cable. The TTCvx provided the 40.00 Mhz clock source for the TTCvi module. Measurements were conducted while repeatedly transmitting two broadcast (BC) commands over channel B and L1 Accept over channel A (case 1) and then again without the BC commands / L1 Accepts (case 2). Both mezzanine cards had their HFBR-2316T fiber optic receiver powered from +5.0V.

The Clock40Des1 clock (1st measurement point) output from the TTCrx is distributed from the CCB over a custom backplane using LVDS levels to all modules in a peripheral crate. This signal was taken thru a 1 m twisted pair cable to our TLK2501 transceiver evaluation optoboard [3] where it was converted to TTL levels. An ICS9170 clock multiplier was used to derive the Clock80_TTL 80.00 Mhz signal (2nd measurement point).

Peak-to-peak jitter measurements at points 1-2 were done using an HP Infinium Oscilloscope (1.5 GHz, 8GSa/s) in Histogram mode at 25 ns after trigger. Results are summarized in Table 1. Two pictures are shown on Figures 1 and 2.

Table 1

Mezzanine Card	ECP680-1102-630C		ECP 680-1102-610B
TTCrx ASIC operating voltage	+5.0V	+3.3V	+5.0V
Clock40Des1 jitter, ps (no BC, no L1A)	153	170	330
Clock40Des1 jitter, ps (BC commands + L1A)	183	215	360
Clock80_TTL jitter, ps (no BC, no L1A)	257	237	-
Clock80_TTL jitter, ps (BC commands + L1A)	272	253	-

Some measurements were repeated for a short (~5 m) optical cable between TTCvx and the new TTCrx ASIC. Results are shown in Table 2.

Table 2

Mezzanine Card	ECP680-1102-630C			
TTCrx ASIC operating voltage and type of cable between TTCvx and TTCrx boards	+5.0V, long cable	+5.0V, short cable	+3.3V, long cable	+3.3V, short cable
Clock40Des1 jitter, ps (no BC, no LA1)	153	142	170	183
Clock40Des1 jitter, ps (BC commands + L1A)	183	187	215	227

3. Optoboard Test

The TLK2501 serializer on one optoboard was clocked at 80.00MHz from the ICS9170 multiplier. A second optoboard residing in the same VME 6U crate was connected to the first one with a 100 m optical cable (Figure 3). A reference clock for the TLK2501 deserializer was provided by an on-board 80.00Mhz quartz oscillator. Two broadcast commands and L1 Accepts were repeatedly sent from TTCvi to TTCrx. The TLK2501 serializer was set to transmit 8-bit pseudo-random bit stream (PRBS) test patterns which were checked by the deserializer at the receiver end. Errors were observed on an HP 53132A universal counter connected to the frame strobed deserializer error signal. The test was done with a new TTCrx ASIC powered from either +3.3V or +5.0V and also with an old ASIC. Each test was run for ~20 hours with no errors observed. Based on these tests, the bit error rate is better than 10^{-12} s^{-1}.

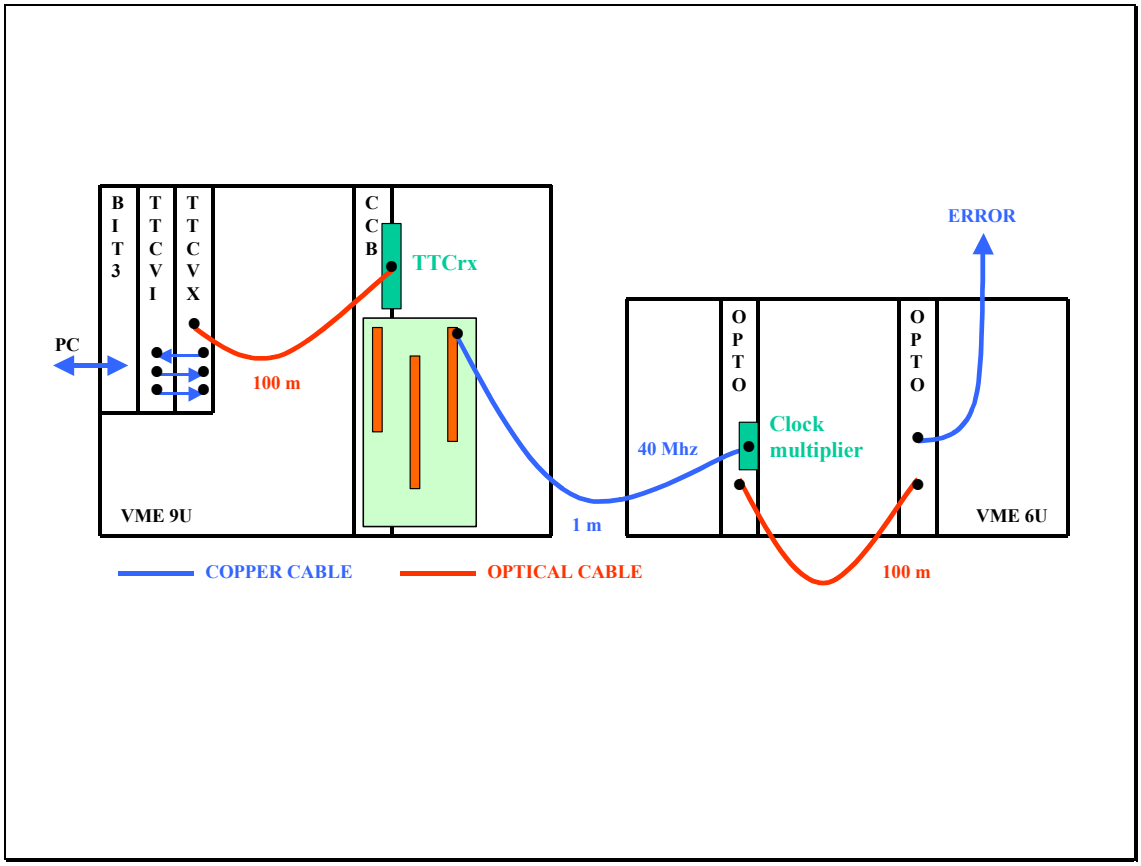

Figure 3: Block Diagram of the Testing Setup

4. Conclusion

1. Jitter values for Clock40Des1 clock output are lower for the latest TTCrx ASIC (ver.3.1) than for previous one.
2. Jitter on Clock40Des1 output increases if the broadcast commands and L1 Accept are transmitted from the TTCvi/TTCvx modules.
3. Jitter distribution for the latest TTCrx ASIC (ver.3.1) is close to gaussian (Fig.1). Jitter distribution for the previous version of ASIC looks differently (Fig. 2, note several peaks).
4. For the TTCrx ASIC ver.3.1. the Clock40Des1 output clock jitter is lower if ASIC is powered from +5.0V.
5. Jitter introduced by any of two available TTCrx ASICs and other components in the clock distribution circuitry at our testing setup is tolerable for TLK2501 transceivers operating at 80.00Mhz.

5. References

[1]. http://ttc.web.cern.ch/TTC/intro.html
[2]. http://bonner-ntserver.rice.edu/cms/CCB'2001.pdf
[3]. M.Matveev, T.Nussbaum, P.Padley, J.Roberts, M.Trapathi. Optical Link Evaluation for the CSC Muon Trigger at CMS. Published in Proceedings of the Seventh Workshop on Electronics for LHC Experiments. Pp. 379-382. Stokholm, Sweden, 10-14 September 2001. CERN 2001-005 CERN/LHCC/2001-034. 22 October 2001.

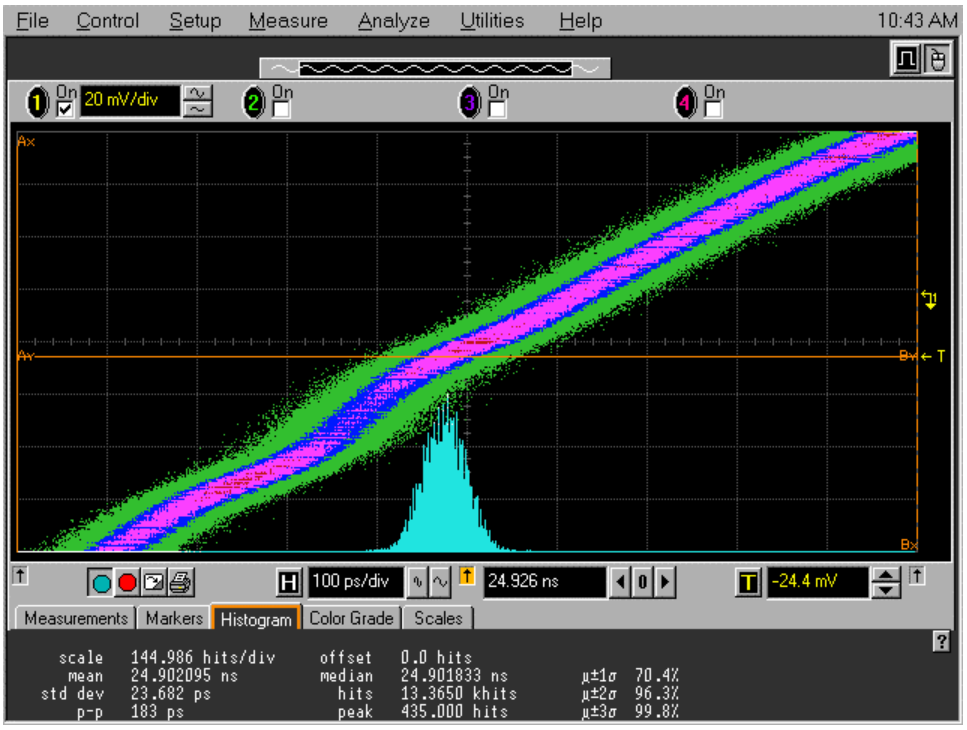

Figure 1: Clock40Des1 jitter, new mezzanine card, +5.0V power

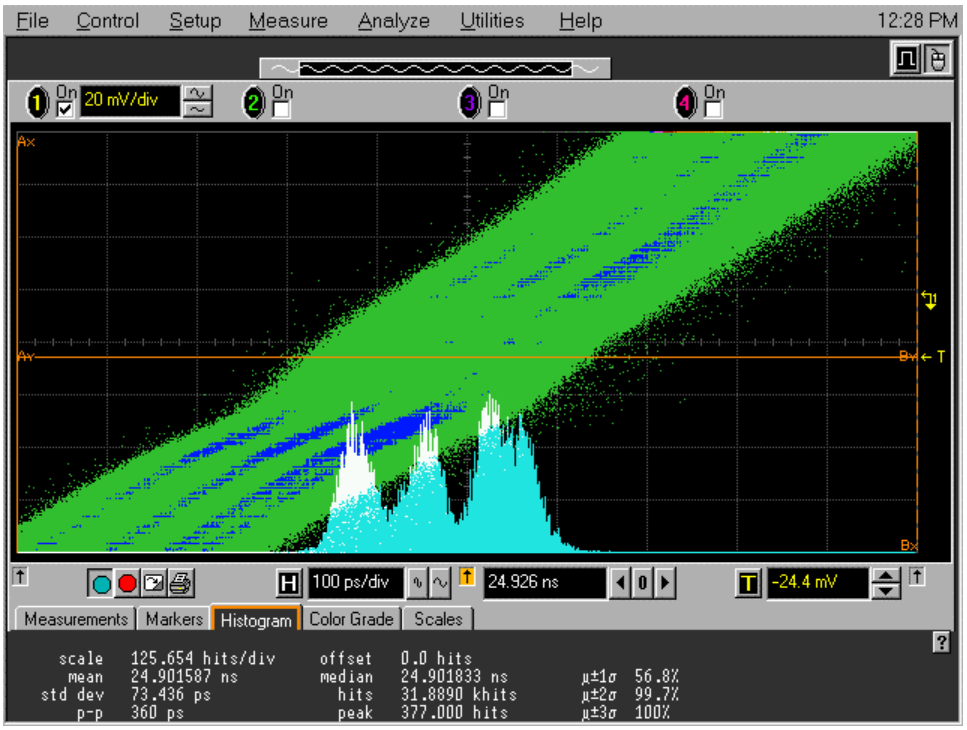

Figure 2: Clock40Des1 jitter, old mezzanine card, +5.0V power