Optoboard160 Specification

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Abstract

This document describes the functionality of the 6U VME module called the Optoboard160 and intended for the evaluation of optical links based on Texas Instruments TLK3101 gigabit transceivers [1] and Small Form Factor Pluggable (SFP) optical transceivers compatible with the SFP Multi-Sourcing Agreement (MSA). The primary goal is an evaluation of optical links operating at 160Mhz.

Introduction

A block diagram of the Optoboard160 is shown on Fig.1. It comprises:

- Two optical links based on Texas Instruments TLK3101 gigabit serializers and Finisar FTRJ8524P2xNy optical transceivers [2];
- Xilinx XC2V250-4FG456 FPGA that performs the VME A24D16 Slave functions as well as an overall control of both optical links;
- TTCrq mezzanine board [3] that provides the 40Mhz, 80Mhz and 160Mhz clock signals for the optical links and FPGA.

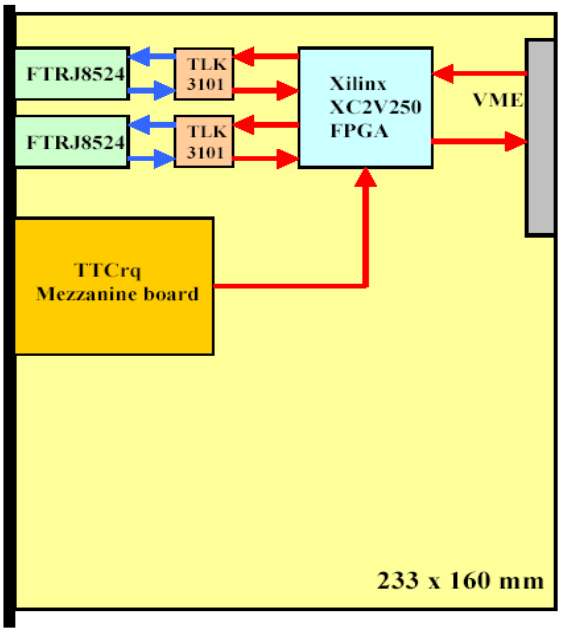

Figure 1: Block Diagram of the Oproboard160

1. Optical Links

Both optical links implemented on the Optoboard160 are identical, independent, bidirectional and fully controlled via theVME. Simplified block diagram of the optolink control is shown on Fig.2. For each link the 16-bit data patterns can be loaded into FIFO_A buffer inside the FPGA and sent out to TLK3101 TXD[15..0] lines on VME command. An 18-bit patterns after serial-to-parallel conversion from RXD[15..0], RX_ER, RX_DV lines are latched into the FIFO_B on recovered RX_CLK signal individually for each link. In the original (2006) version of firmware the RXD[0] bit acts as a « Write_Enable » signal for the FIFO_B buffers. In the modified (September 16, 2013) version the FIFO_B buffers are loaded on a TTC command = 30h (see more details in the CCB manual http://padley.rice.edu/cms/ccb2004p_102110.pdf). FIFO_A buffers can be written over VME. FIFO_B are available for read from the VME; for details see Section 4. Each FIFO buffer is 16-bit wide and 511-bit deep.

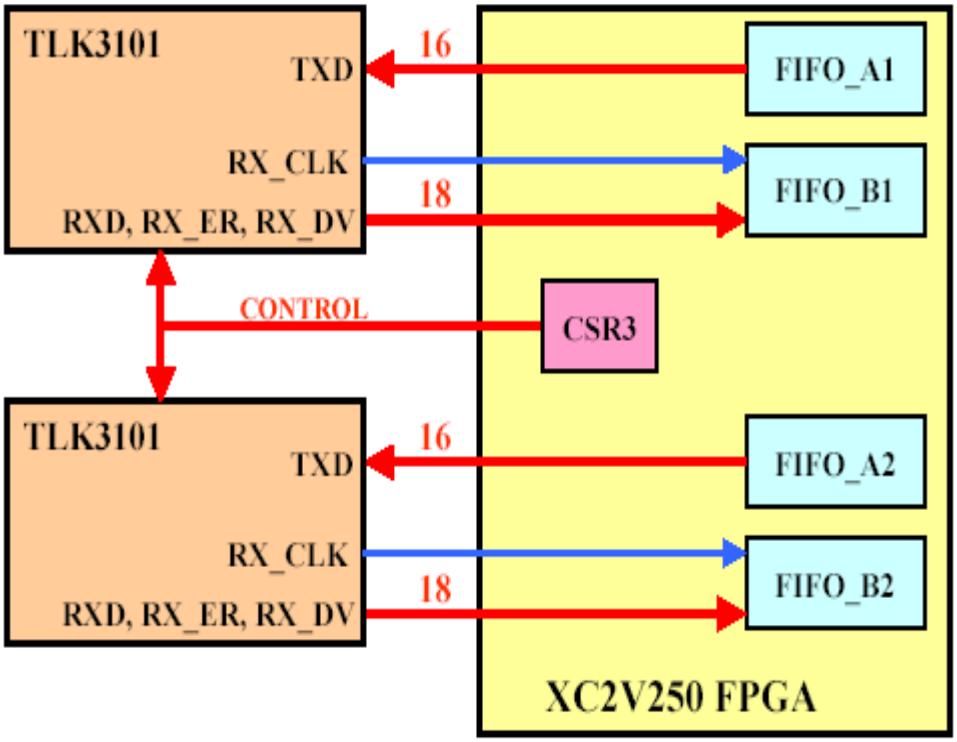

Figure 2: Control of the optolinks from the FPGA

2. TTCrq Mezzanine Board

A list of signals provided by the TTCrq mezzanine and pin assignment of the mezzanine connectors are listed in Tables 1 and 2 respectively. The signals received by the FPGA on Optoboard160 are marked blue in both tables. They can be used in future, if the TTC control of optolinks will be required.

Table 1: Interface signals to/from TTC mezzanine card

Signal	Bits	Short Description
Signals to/from two 50-pin connectors backward compatible with TTCrm mezzanine card		
BCntRes	1	Bunch Counter Reset signal
BCntStr	1	Bunch Counter Strobe. Indicates that a bunch number is present on the output BCnt<11:0> bus
Brcst<7:2>	6	Broadcast commands/data output bus
BrcstStr<2:1>	2	Broadcast messages strobes
Clock40Des1	1	LHC 40.08 MHz deskewed reference clock signal
DbErStr	1	Indicates that a double error or a frame error has occurred
Dout<7:0>	8	Data bus. Normally used to output the data content of an individually-addressed commands/data
DQ<3:0>	4	Data qualifier bits. Indicate the type of data on the data bus register
BCnt<11..0>	12	Bunch or Event counter outputs
DoutStr	1	Data out strobe. Indicates valid data on the data bus
EvCntHStr	1	Event counter high word strobe
EvCntLStr	1	Event counter low word strobe
EvCntRes	1	Event counter reset signal
L1Accept	1	First level trigger accept signal
Reset_b	1	Reset TTCrx ASIC, active “low”
SinErrStr	1	Single error strobe
SubAddr<7:0>	8	Subaddress bus. Used to output the subaddress content of an individually address commands/data
TTCReady	1	Indicates that TTCrx ASIC is ready for normal operation
SDA	1	Data Line of I2C interface
SCL	1	Clock Line of I2C interface
Total	54	
Signals to/from an additional 26-pin connector (TTCrq mezzanine only)		
FoSelect<3..0>	4	Control inputs for the VCXO free running oscillation frequency (QPLL only)
Mode	1	QPLL multiplication mode control input
Restart	1	Enable/disable automatic restart of the PLL (control input for the QPLL)
ExternalControl	1	Control input for the VCXO (QPLL only)
Locked	1	QPLL output status signal
40Mhz clock	2	LVDS clock outputs
80Mhz clock	2	LVDS clock outputs
160Mhz clock	2	LVDS clock outputs
40Mhz_CMOS	1	CMOS 40Mhz clock output
~Reset	1	QPLL control input, active “low”
Error	1	QPLL status output
Total	17	

Table 2: Pin assignment of the TTCmr/TTCrq mezzanine connectors

Connector J1			Connector J2			Connector J3		
Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	Clock40	Output	1	BrcstStr2	Output	1	F0Select<0>	Input
2	Clock40Des1	Output	2	ClockL1Accept	Output	2	Mode	Input
3	Brcst<5>	Output	3	Brcst<6>	Output	3	InLVDS+	Input
4	Brcst<4>	Output	4	Brcst<7>	Output	4	InLVDS-	Input
5	Brcst<3>	Output	5	EvCntRes	Output	5	GND	Power
6	Brcst<2>	Output	6	L1Accept	Output	6	ExternalClock	Input
7	Clock40Des2	Output	7	EvCntLStr	Output	7	AutoRestart	Input
8	BrcstStr1	Output	8	EvCntHStr	Output	8	ExternalContr	Input
9	DbErrStr	Output	9	BcntRes	Output	9	F0Select<3>	Input

10	SinErrStr	Output	10	GND	Power	10	~Reset	Input
11	SubAdd<0>	Bidir	11	BCnt<0>	Output	11	Locked	Output
12	SubAdd<1>	Bidir	12	BCnt<1>	Output	12	Error	Output
13	SubAdd<2>	Bidir	13	BCnt<2>	Output	13	GND	Power
14	SubAdd<3>	Bidir	14	BCnt<3>	Output	14	Lvds80Mhz-	Output
15	SubAdd<4>	Bidir	15	BCnt<4>	Output	15	Lvds80Mhz+	Output
16	SubAdd<5>	Bidir	16	BCnt<5>	Output	16	GND	Power
17	SubAdd<6>	Bidir	17	BCnt<6>	Output	17	F0Select<2>	Input
18	SubAdd<7>	Bidir	18	BCnt<7>	Output	18	GND	Power
19	DQ<0>	Output	19	BCnt<8>	Output	19	Lvds160Mhz+	Output
20	DQ<1>	Output	20	BCnt<9>	Output	20	Lvds160Mhz-	Output
21	DQ<2>	Output	21	BCnt<10>	Output	21	GND	Power
22	DQ<3>	Output	22	BCnt<11>	Output	22	Lvds40Mhz-	Output
23	DoutStr	Output	23	JTAGTMS	Input	23	Lvds40Mhz+	Output
24	GND	Power	24	JTAGTRST_b	Input	24	F0Select<1>	Input
25	Dout<0>	Bidir	25	JTAGTCK	Input	25	Cmos40Mhz	Output
26	Dout<1>	Bidir	26	JTAGTDO	Output	26	GND	Power
27	Dout<2>	Bidir	27	SDA	Bidir			
28	Dout<3>	Bidir	28	JTAGTDI	Input			
29	Dout<4>	Bidir	29	BCntStr	Output			
30	Dout<5>	Bidir	30	Serial_B_Chan	Output			
31	Dout<6>	Bidir	31	GND	Power			
32	Dout<7>	Bidir	32	GND	Power			
33	Reset_b	Input	33	GND	Power			
34	TTCReady	Output	34	GND	Power			
35	GND	Power	35	+5V	Power			
36	GND	Power	36	+5V	Power			
37	GND	Power	37	+5V	Power			
38	GND	Power	38	+5V	Power			
39	GND	Power	39	QPLL power	Passive			
40	GND	Power	40	SCL	Input			
41	GND	Power	41	GND	Power			
42	GND	Power	42	GND	Power			
43	GND	Power	43	+5V	Power			
44	GND	Power	44	+5V	Power			
45	GND	Power	45	+5V	Power			
46	GND	Power	46	+5V	Power			
47	GND	Power	47	GND	Power			
48	GND	Power	48	GND	Power			
49	GND	Power	49	GND	Power			
50	GND	Power	50	GND	Power			

3. **Clock Distribution**

The 40Mhz and 80Mhz clock signals from the QPLL on TTCrq mezzanine board are connected to FPGA clock inputs. 80Mhz clock is required for the correct operation of the FPGA. There are three sources of 160Mhz signal provided for the FPGA and both TLK3101 transceivers:

- 160Mhz clock output from the TTCrq mezzanine;
- External oscillator U15 with the LVDS outputs (jumper JP1 should be installed)

- External source connected to TP8 near U11, CMOS level or TTL level (jumper JP2 should be installed).

A recovered 160Mhz clock from each of the TLK3101 transceivers is connected to FPGA and used for data clocking into the FIFO_B buffers.

4. VME Interface and Control and Status Registers (CSR)

The Optoboard160 can be accessed in the VME crate using geographical addressing that utilizes the address pins GA<4-0> available on the VME64x backplane. In this mode the board recognizes its address space when the code on address lines A<23-19> is equal to the 5-bit geographical code of its slot. If a conventional VME backplane with 3-row 96-pin connectors is used, the value of upper five address bits A[23..19] for decoding can be selected by an on-board switch S1-1..5. Address bits A[18..8]=0. Address bits A[7..1] are decoded inside the FPGA (Table 3). The board recognizes an AM codes 39(hex), 3D(hex) and supports A24D16 slave operations. It does not respond to byte-addressing modes, so all valid addresses must be even numbers. The Optoboard160 does not use a J2 VME connector.

Table 3

Address (hex)	Function
Base + 0 (R/W)	FIFO_A1; output 16-bit FIFO for optolink1 (TLK3101 U2); bits TXD[15..0]
Base + 2 (R/W)	FIFO_A2 ; output 16-bit FIFO for optolink2 (TLK3101 U6); bits TXD[15..0]
Base + 4 (R)	FIFO_B11; input 16-bit FIFO for optolink1 (TLK3101 U2); bits RXD[15..0]
Base + 6 (R)	FIFO_B12; input 16-bit FIFO for optolink1 (TLK3101 U2); FIFO_B12[0]=RX_ER; FIFO_B12[1]=RX_DV; FIFO_B12[15..2]=0
Base + 8 (R)	FIFO_B21; input 16-bit FIFO for optolink2 (TLK3101 U6); bits RXD[15..0]
Base + A (R)	FIFO_B22; input 16-bit FIFO for optolink2 (TLK3101 U6); FIFO_B22[0]=RX_ER; FIFO_B22[1]=RX_DV; FIFO_B22[15..2]=0
Base + C (R/W)	CSR0; General purpose 16-bit register
Base + E (R)	CSR1; Status of the TTCrq outputs (see Section 4.1); Read only.
Base + 10 (R)	CSR4; QPLL Status register (see Section 4.4); Read only.
Base + 12 (W)	Send data out of FIFO_A1; Write only; Dataless.
Base + 14 (W)	Send data out of FIFO_A2; Write only; Dataless.
Base + 16 (W)	
Base + 18 (W)	
Base + 1A	
Base + 1C (W)	Reset all FIFO buffers; Write only; Dataless.
Base + 1E (W)	
Base + 20 (R/W)	CSR3; Optolink1 and Optolink2 control bits (see Section 4.2).
Base + 22 (R)	CSR5; Data of the firmware revision (see Section 4.5); Read only.
Base + 24 (R)	CSR2; FIFO status register (see Section 4.2); Read only.
Base + 26 (W)	
Base + 28 (W)	
Base + 2A (W)	Reset PRBS error counter for Link 1
Base + 2C (W)	Reset PRBS error counter for Link 2
Base + 2E (R)	Link 1PRBS error counter content, 16-bit
Base + 30 (R)	Link 2PRBS error counter content, 16-bit

4.1. CSR0 (general purpose register)

CSR0 can be used to verify the VME access to the optoboard.

4.2. CSR1 (status of the TTCrq outputs)

Bit	Access	Function
0	R	BRCSRSTR1
1	R	BRCSTSTR2
2	R	BCBTRES
3	R	EVCNTRES
4	R	BRCST2
5	R	BRCST3
6	R	BRCST4
7	R	BRCST5
8	R	BRCST6
9	R	BRCST7
10	R	L1ACC
11	R	DQ0
12	R	DQ1
13	R	DQ2
14	R	DQ3
15	R	TTCREADY

4.3. CSR2 (FIFO status)

Bit	Access	Function
0	R	FIFO_A1 full (active « 1 »)
1	R	FIFO_A1 empty (active « 1 »)
2	R	FIFO_A2 full (active « 1 »)
3	R	FIFO_A2 empty (active « 1 »)
4	R	(FIFO_B11 and FIFO_B12) full (active « 1 »)
5	R	(FIFO_B11 and FIFO_B12) empty (active « 1 »)
6	R	(FIFO_B21 and FIFO_B22) full (active « 1 »)
7	R	(FIFO_B21 and FIFO_B22) empty (active « 1 »)
8	R	« 0 »
9	R	« 0 »
10	R	« 0 »
11	R	« 0 »
12	R	« 0 »
13	R	« 0 »
14	R	« 0 »
15	R	« 0 »

4.4. CSR3 (Optolink control)

Bit	Access	Function
0	W/R	ENABLE ; Optolink1 (TLK3101 U2)
1	W/R	LCKREFN ; Optolink1 (TLK3101 U2)
2	W/R	LOOPEN ; Optolink1 (TLK3101 U2)
3	W/R	PRBSEN ; Optolink1 (TLK3101 U2)
4	W/R	TX_EN ; Optolink1 (TLK3101 U2)
5	W/R	TX_ER ; Optolink1 (TLK3101 U2)
6	W/R	/ENABLE of EXTERNAL CLOCK for the FPGA and both optolinks; (active « 0 »)

7	W/R	RATE ; Optolink1 (Finisar FTRJ8524 P3)
8	W/R	ENABLE ; Optolink2 (TLK3101 U6)
9	W/R	LCKREFN ; Optolink2 (TLK3101 U6)
10	W/R	LOOPEN ; Optolink2 (TLK3101 U6)
11	W/R	PRBSEN ; Optolink2 (TLK3101 U6)
12	W/R	TX_EN ; Optolink2 (TLK3101 U6)
13	W/R	TX_ER ; Optolink2 (TLK3101 U6)
14	W/R	-
15	W/R	RATE ; Optolink2 (Finisar FTRJ8524 P6)

4.4. CSR4 (QPLL status)

Bit	Access	Function
0	R	« 0 »
1	R	« 0 »
2	R	« 0 »
3	R	« 0 »
4	R	« 0 »
5	R	« 0 »
6	R	« 0 »
7	R	« 0 »
8	R	« 0 »
9	R	« 0 »
10	R	« 0 »
11	R	« 0 »
12	R	« 0 »
13	R	« 0 »
14	R	QPLL_ERR
15	R	QPLL_LOCK

4.5. CSR5 (Date of the firmware revision)

Bit	Access	Function
0	R	Day (LSB)
1	R	Day
2	R	Day
3	R	Day
4	R	Day (MSB)
5	R	Month (LSB)
6	R	Month
7	R	Month
8	R	Month (MSB)
9	R	Year (LSB) *
10	R	Year *
11	R	Year (MSB) *
12	R	« 0 »
13	R	« 0 »
14	R	« 0 »
15	R	« 0 »

* add to 2000 to obtain a year

5. JTAG Access to FPGA and EPROM

One Xilinx XC2V250-4FG456 FPGA that requires one XC18V02 EPROM is used on Optoboard160. Both FPGA and EPROM can be accessed over JTAG. The first device in JTAG chain is the EPROM, and the second device is the FPGA. A 14-pin JTAG connector compatible with the Xilinx Parallel Cable IV is located near front panel.

6. Fuses

Fuse F4 is required at any time to provide a +5V power from the VME backplane (any type) for three on-board voltage regulators U23, U24 and U25. Fuse F1 is needed at any time to provide a +1.5V for the FPGA core from the on-board voltage regulator U23. Fuse F3 is also required at any time to provide a +2.5V power for the TLK3101 transceivers from on-board voltage regulator U24. Output value of the U24 can be adjusted with the potentiometer R52. Fuse F2 is needed to provide +3.3V power for on-board devices if VME64x backplane is used. Fuse F5 is needed to provide a +3.3V power from on-board voltage regulator U25 when a conventional VME backplane is used. Only one (either F2 or F5) should be installed at a time.

7. Front Panel

There are 28 LEDs on the front panel:

- "+3.3" from VME64x backplane (if F2 is installed) or from on-board voltage regulator U25 (if F5 is installed) (green, D21)
- "+5.0" from VME backplane (green, D22)
- "+1.5" for FPGA core, from on-board voltage regulator U23 (green, D19)
- "+2.5" for TLK3101 transceivers, from on-board voltage regulator U24 (green, D20)
- "FA1FL" FIFO_A1 full (red, D10)
- "FA1EM" FIFO_A1 empty (red, D11)
- "FA2FL" FIFO_A2 full (red, D12)
- "FA2EM" FIFO_A2 empty (red, D13)
- "FB1FL" FIFO_B11 and FIFO_B12 full (red, D14)
- "FB1EM" FIFO_B11 and FIFO_B12 empty (red, D15)
- "FB2FL" FIFO_B21 and FIFO_B22 full (red, D16)
- "FB2EM" FIFO_B21 and FIFO_B22 empty (red, D17)
- "CLK40" indicates that 40Mhz clock from the TTCrq is active (green, output of the counter running at ~10Hz, D4)
- "CLK80" indicates that 80Mhz clock from the TTCrq is active (green, output of the counter running at ~10Hz, D5)
- "CLK160" indicates that 160Mhz clock from the TTCrq or external source is active (green, output of the counter running at ~10Hz, D6)
- "CLKVME" indicates that the VME system clock is active (green, output of the counter running at ~10Hz, D18)
- "CLK160A" indicates that the recovered 160Mhz clock from optolink 1 is active (green, output of the counter running at ~10Hz, D27)

- "CLK160B" indicates that the recovered 160Mhz clock from optolink 2 is active (green, output of the counter running at ~10Hz, D28)
- "LOS1" LOS output of the FTRJ8524 transceiver (optolink1, P3; red, D2)
- "LOS2" LOS output of the FTRJ8524 transceiver (optolink2, P6; red, D3)
- "DACK" indicates VME access to Optoboard160 (yellow, with one-shot, D7)
- "RUNA" indicates that the data was sent from FIFO_A1 (with one-shot, red, D8)
- "RUNB" indicates that the data was sent from FIFO_A2 (with one-shot, red, D9)
- "RXERA" indicates the state of RX_ER pin of TLK3101 U2 (optolink 1, red, D29)
- "RXDVA" indicates the state of RX_DV pin of TLK3101 U2 (optolink 1, red, D30)
- "RXERB" indicates the state of RX_ER pin of TLK3101 U6 (optolink 2, red, D31)
- "RXDVB" indicates the state of RX_DV pin of TLK3101 U6 (optolink 2, red, D32)
- "DONE" configuration of the Xilinx FPGA from its EPROM was done successfully (green, D1).

Both Finisar optical modules, as well as JTAG P4 connector and optical connector on TTCrq mezzanine board are facing the front panel as well.

References

[1]. TLK3101 2.5 Gbps to 3.125 Gbps Transceiver Datasheet. Available at http://focus.ti.com/lit/ds/symlink/tlk3101.pdf
[2]. Finisar 4.25Gb/s Short-Wavelength SFP Transceiver FTRJ8524P2xNy Product Specification. Available at http://www.finisar.com/optics/documents/FTRJ8524P2xNySpecRevH.pdf
[3]. J.Christiansen, A.Marchioro, P.Moreira and T.Toifl. TTCrx Reference Manual. August 2005. Version 3.10. CERN-ECP/MIC, Geneva, Switzerland. Available at http://bonner-ntserver.rice.edu/cms/TTCrx_manual3.10.pdf
[4]. Xilinx Virtex-2 Platform FPGA User Guide. Available at http://direct.xilinx.com/bvdocs/userguides/ug002.pdf

History

12/14/2005: Initial release
01/11/2006: Update.
02/09/2006: DCM1 and DCM2 were removed from the design.
09/16/2013: Update on FIFO_B write (in red, section 1).