Optical Link Evaluation Board for the CSC Muon Trigger at CMS

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User's Manual

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Abstract

The main goal of the design was to evaluate a data link based on Texas Instruments TLK2501 gigabit transceiver and Finisar FTRJ-8519-1-2.5 optical module as a possible choice for data transmission from the CSC peripheral electronics to counting room at the CMS experiment.

I. DATA SERIALIZER AND OPTICAL MODULE

Among several high speed data serializers available on the market, Texas Instruments TLK2501 [1] is one of the most attractive. It is a member of the family of TI multigigabit transceivers and performs both serial-to-parallel and parallel-to-serial data conversion. The transmitter latches 16-bit parallel data at a rate of the reference clock and internally encodes it into 20-bit using an 8B/10B encoding format. The resulting 20-bit word is transmitted differentially at 20 times the reference clock. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel word to the extracted reference clock and applying 8B/10B decoding. The frequency range of the reference clock is 80MHz to 125MHz that allows us to use a transmission at 80.16Mhz, or at a double frequency of LHC operation of 40.08Mhz..

The TLK2501 transceiver has a built in 8-bit pseudo-random bit stream (PRBS) generator and some other useful functions such as a loss of signal detection circuit and power down mode. The device is powered from +2.5V and consumes less than 325mW typically. Parallel data, control and status pins are 3.3V compatible. The device is available in a 64-pin VQFP package and characterized for operation from –40C to +85C.

Finisar FTRJ-8519-1-2.5 [2] 2x5 pinned small form factor (SFF) transceiver was chosen as an optical module. It provides a bidirectional communications at a data rates up to 2.125Gbps (1.6Gbps is required in our case). Transmitter type is 850 nm multimode laser, fiber length (50um MMF) is up to 300 m. The transceiver operates at extended voltage (3.15V to 3.60V) and temperature (-10C to +85C) ranges and dissipates less than 750mW. One advantage of the FTRJ-8519-1-2.5 module over similar optical transceivers available from other vendors is a metal enclosure for lower EMI.

II. BOARD FUNCTIONALITY

A simplified block diagram of the evaluation board is shown on Figure 1. It comprises two TLK2501 serializers, two optical modules and control logic based on

Altera EP20K100EQC240 PLD. This PLD provides an access to 16-bit receiver and transmitter data busses of both TLK2501 serializers from VMEbus. In addition to VME A24D16 slave interface it consists of an input and output 256-bit deep FIFO buffers, two delay FIFO buffers, 16-bit pseudo random bit stream (PRBS) generator and 2 16-bit error counters. There are three modes of board operation. In mode 1 every serializer can generate a PRBS from its own generator, check data at a receiver end and count errors. In mode 2 a 16-bit PRBS is generated from the PLD to both TLK2501 transmitters simultaneously. Two delay buffers with adjustable depth (using variable switch on the front panel) allow to delay the PRBS stream and compare it against a stream from one or two receivers. A separate error counters in this mode are also available for reading from VME.

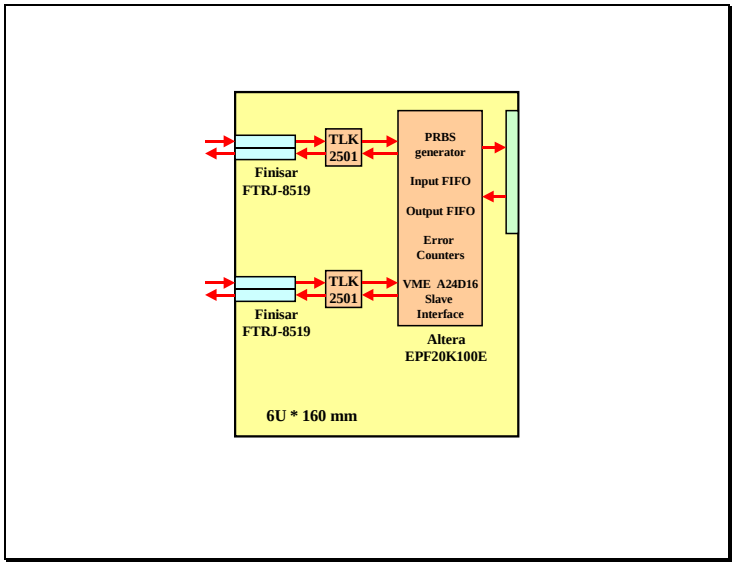

Figure 1: Evaluation Board Block Diagram

In mode 3 a random data (up to 256 16-bit words) can be loaded into source FIFO buffer and then upon a specific VME write command be sent at 80Mhz to both "A" and "B" TLK2501 transmitter sections. The data from both receivers can be stored into two input (destination) FIFO buffers which are available for VME read. This mode would allow to send data representing one muon at 80Mhz for future test of the next Sector Processor prototype.

III. PLD AND EPROM CONFIGURING

The main PLD EPF20K100EQC240 can be configured in a three different ways. The first one is a configuration scheme that uses an Altera EPC2LC20 EPROM. If this EPROM is installed in a socket, then configuration starts upon power on. In this case the configuration time is about 100 ms. The second scheme assumes configuration over Altera Bit- or ByteBlaster downloading cable which should be connected to P4. Switch S3 2-3 should be "on". The third scheme uses configuration from the SCANPSC100 [3] JTAG controller under VME control. This controller is used as an optional channel for PLD configuration. Switch S3 2-3 should be "off". In order to configure the PLD in this

mode, an executable file jam.exe available from [4] should be installed. The command line is:

Jam.exe –v –aCONFIGURE –b(addreess) filename.jbc

where (address) is the base address of the SCANPSC100 controller in VME address space in decimal format. During testing the base address is 780020(hex) and (address)=7864320(dec). Filename is a name of the configuration file which should be produced by Altera Quartus software. Downloading takes ~1sec. In addition to PLD, an EPROM itself can be programmed in modes 2 and 3 as well. To do this, switches S4 1-4 should be "on" S4 2-3 "off", S5 1-4 "on" and S5 2-3 "off". For PLD configuring, S4 1-4 should be "off", S4 2-3 "on", S5 1-4 "off" and S5 2-3 "on".

In all three cases, as soon as PLD configuration was done successfully, the LED D5 is "off".

IV. VME INTERFACE

Evaluation board performs A24D16 Slave functions. It can be addressed in a VME crate using either logical or geographical (in case of VME64 backplane) addressing. If S3 1-4 is "on", then the mode is a logical addressing. If S3 1-4 is "off", then the geographical mode is in effect. The board decodes AM=3E(hex), 3D(hex), 3A(hea) and 39(hex) codes. Block transfers are not supported. Base address 780000(hex) is used for initial board testing. The board is addressed if the code on lines A<23-19> is equal to a geographical position GA<4-0> of the board in a crate. VME decoding is performed by the socket-mounted EPM7128ALC84 EEPROM-based PLD. This PLD also controls the SCANPSC100 operations. The main EPF20K100EQC240 PLD decodes its own addresses and produces DTACK reply. VME addresses decoded by the board are listed in Table 1.

Table 1

Address(hex)	Access	Function
Base + 20	Read/Write	CSR1
Base + 22	Read/Write	Source FIFO, 16-bit wide and 256-bit deep
Base + 24	Write	Start transmission of 256 words at 80Mhz from the Source FIFO
Base + 24	Read	Read Destination FIFO_A, data word
Base + 26	Write	Reset both "A" and "B" TLK2501 chips
Base + 26	Read	Read Destination FIFO_A, status word D<0> represents the RX_ER output of TLK2501 D<1> represents the RX_DV/LOS output of TLK2501 D<15..2>=0
Base + 28	Write	Reset PRBS generator built-in into PLD
Base + 28	Read	Read Destination FIFO_B, data word
Base + 2a	Write	-
Base + 2a	Read	Read Destination FIFO_B, status word D<0> represents the RX_ER output of TLK2501 D<1> represents the RX_DV/LOS output of TLK2501 D<15..2>=0
Base + 2c	Write	Reset all error counters
Base + 2c	Read	Read "A" Error Counters

		D<15..8> Error Counter if PLD-based PRBS is used D<7..0> Error Counter if TLK2501 PRBS is used
Base + 2e	Write	-
Base + 2e	Read	Read "B" Error Counters D<15..8> Error Counter if PLD-based PRBS is used D<7..0> Error Counter if TLK2501 PRBS is used
Base + 10	Write	Reset SCANPSC100 controller
Base + 0…Base + e	Read/Write	SCANPSC100 internal registers, see [3]

V. Control and Status Register and On-board Jumpers

CSR1<0> controls the "A" TX_EN input if 2-3 of JP13 are connected. If 1-2 of JP13 are connected, then TX_EN=0 (see Table 1 in [1]). If all pins are open, TX_EN=1

CSR1<1> controls the "A" TX_ERR input if 2-3 of JP8 are connected. If 1-2 of JP8 are connected, then TX_ERR=0 (see Table 1 in [1]) or if all open, TX_ERR=1

CSR1<2> controls the "A" LOOPEN input if 2-3 of JP3 are connected. If 1-2 of JP3 are connected, then LOOPEN=0 and internal loopback path is disabled or enabled if all pins open.

CSR1<3> controls the "A" LOCKREFN input if 2-3 of JP10 are connected. If 1-2 of JP10 are connected, then LOCKREFN=0 and receiver clock is frequency locked to GTX_CLK (receiver is not tracking the data). This setting is required to bypass the duplex handshaking sequence and allow simplex transmission to occur.

CSR1<4> controls the "A" PRBSEN input if 2-3 of JP1 are connected. If 1-2 of JP1 are connected, then PRBSEN=0 and internal PRBS mode is disabled or enabled if all pins are open.

CSR1<5> controls the source of data (PRBS generator or FIFO) for both TLK2501 if 2-3 of JP5 are connected. If 1-2 of JP5 are connected, then PLD PRBS is a source of data.

CSR1<6..7> - are not used. Not available for read/write.

CSR1<8> controls the "B" TX_EN input if 2-3 of JP9 are connected. If 1-2 of JP9 are connected, then TX_EN=0 (see Table 1 in [1]). If all pins are open, TX_EN =1

CSR1<9> controls the "B" TX_ERR input if 2-3 of JP7 are connected. If 1-2 of JP7 are connected, then TX_ERR=0 (see Table 1 in [1]) or if all open, TX_ERR=1.

CSR1<10> controls the "B" LOOPEN input if 2-3 of JP4 are connected. If 1-2 of JP4 are connected, then LOOPEN=0 and internal loopback path is disabled or enabled if all pins open.

CSR1<11> controls the "B" LOCKREFN input if 2-3 of JP14 are connected. If 1-2 of JP14 are connected, then LOCKREFN=0 and receiver clock is frequency locked to GTX_CLK (receiver is not tracking the data). This setting is required to bypass the duplex handshaking sequence and allow simplex transmission to occur.

CSR1<12> controls the "B" PRBSEN input if 2-3 of JP12 are connected. If 1-2 of JP12 are connected, then PRBSEN=0 and internal PRBS mode is disabled

CSR1<15..13> - are not used. Not available for read/write.

In addition to jumpers listed above, the JP6 and JP2 control the ENABLE pins of "A" and "B" channels respectively. If JP6 2-3 and JP2 2-3 are connected, then a reset pulse to ENABLE pins is generated upon write to (Base + 26) address. If JP6 1-2 and JP2 1-2 are connected, then ENABLE=0 and both devices are in power-down mode. See [1] for more details. If all are open, ENABLE=1 and TLK2501 will run after internal power up reset is completed.

JP11 is used to reset the PLD internal registers and counters. In normal mode JP11 2-3 should be connected. For a reset procedure, JP11 1-2 should be connected temporarily.

VI. Board Programming and External Connections

A few examples of board programming sequence are listed below. Corresponding jumpers (see Section V) must be installed. Particularly, for FIFO-to-FIFO tests 1 and 2 (below), 2-3 pins of J7, J9, J12, J4, J14, J2, J8, J13, J1, J3, J10, J6 jumpers should be installed.

1. Send data from source FIFO to destination FIFO "B"
   - write 820(hex) to (Base + 20) address to synchronize the link
   - write 921(hex) to (Base + 20) address
   - load 256 data patterns to source FIFO on write to (Base+22) address
   - start transmission on write any data (Base+24)
   - read and check data from (Base + 28) (patterns)
   - read and check data from (Base + 2a) (status)

The following external wire connections are needed in this mode (assuming that only U22 optical module is installed):

- J21 should be connected to J5
- J3 should be connected to J23
- J10 should be connected to J6
- J1 should be connected to J13

2. Send data from source FIFO to destination FIFO "A"
   - write 28(hex) to (Base + 20) address to synchronize the link
   - write 128(hex) to (Base + 20) address
   - load 256 data patterns to source FIFO on write to (Base + 22) address
   - start transmission on write any data (Base + 24)
   - read and check data from (Base + 24) (patterns)
   - read and check data from (Base + 26) (status)

The following external wire connections are needed in this mode (assuming that only U22 optical module is installed):

- J15 should be connected to J5
- J2 should be connected to J23
- J10 should be connected to J20
- J1 should be connected to J19

3. Send PLD PRBS data from channel "B" to "A" (external connections are the same as in 2)
   - write 08 (hex) to (Base + 20) address to synchronize the link
   - write 18 (hex) to (Base + 20) address

VII. FRONT PANEL

There are on the front panel:

- Variable switches S1 and S2 for adjusting of the Delay FIFO "A" and "B" depth respectively by observing ERRSIG_A, B outputs.
- Outputs Tzero, Azero & Bzero which = 1 when PLD PRBS transmitted or received data words = 0000 hex to allow determination of total latency
- Red LED D2 indicates a VME access to a main EPF20K100EQC240 PLD
- Red LED D3 indicates a VME access to the board
- Red LED D5 indicates a configuration status of the EPF20K100EQC240 PLD (see section III)
- Red LED D7 indicates a VME access to SCANPS100 controller
- Red D6 and D15 LEDs indicate "Signal Detect" output of optomodules U23 and U22 respectively. "On" means detected signal and normal operation of the optical link.

VIII. REFERENCES

[1]. http://www-s.ti.com/sc/psheets/slls427a/slls427a.pdf
[2]. http://www.finisar.com/pdf/2x5sff-2gig.pdf
[3]. http://www.national.com/pf/SC/SCANPSC100F.html
[4]. http://www.phys.ufl.edu/~madorsky/JTAG/