

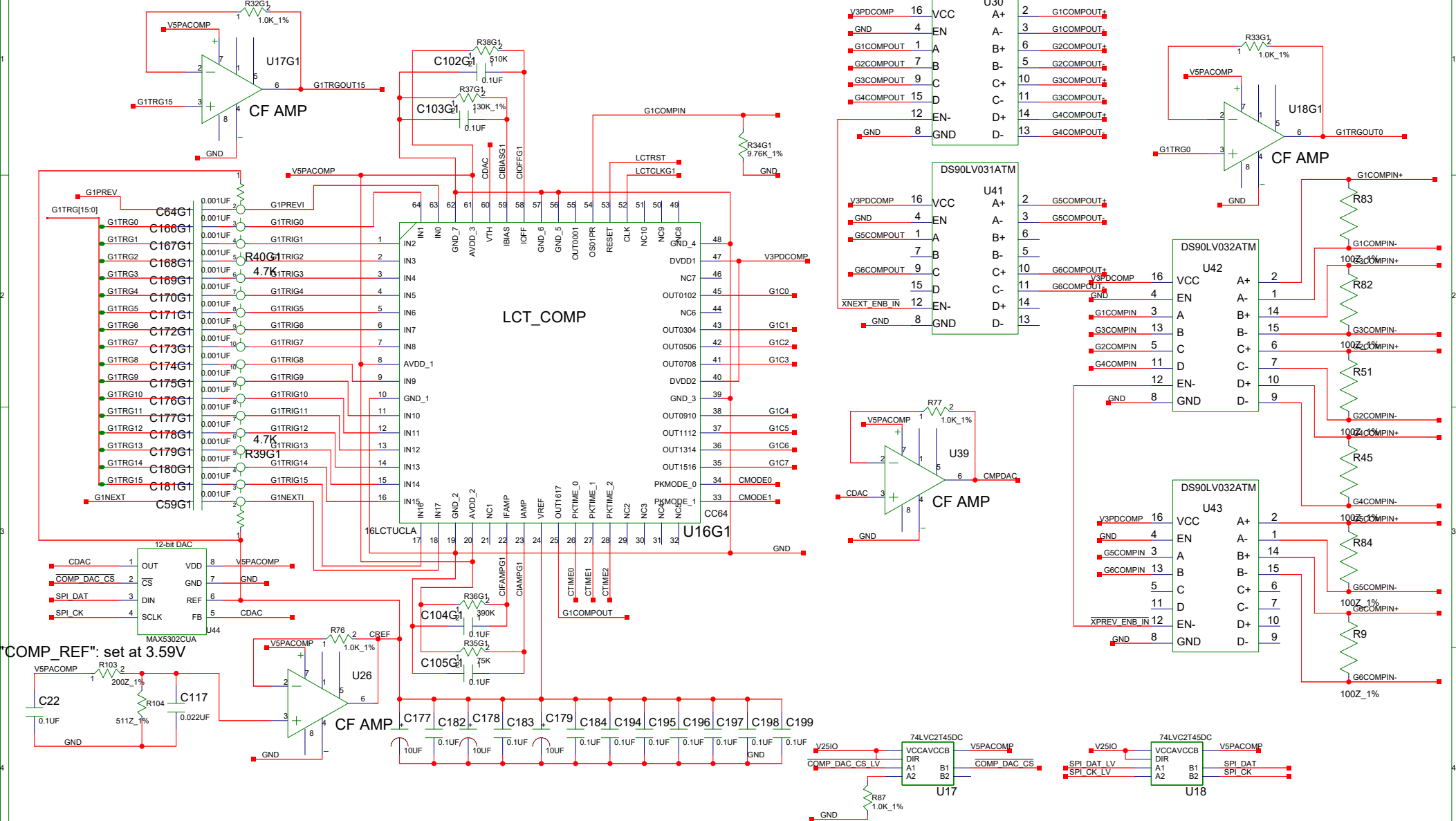
MEx/1 Digital Cathode Front-End Board xDCFEB Version 2a

January, 2018

xDCFEB second prototype
Modified front rails to add more connections to main board (added perf holes)

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COLUMBUS OHIO 43210

Put the op-amps near the branch point of the traces!



Group G1

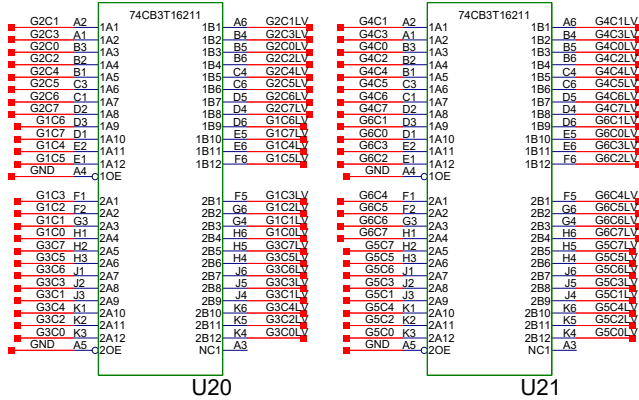
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE
Cathode Comparator System
Digital Cathode Front-End Board (DCFEb)
CMS CSC Electronics

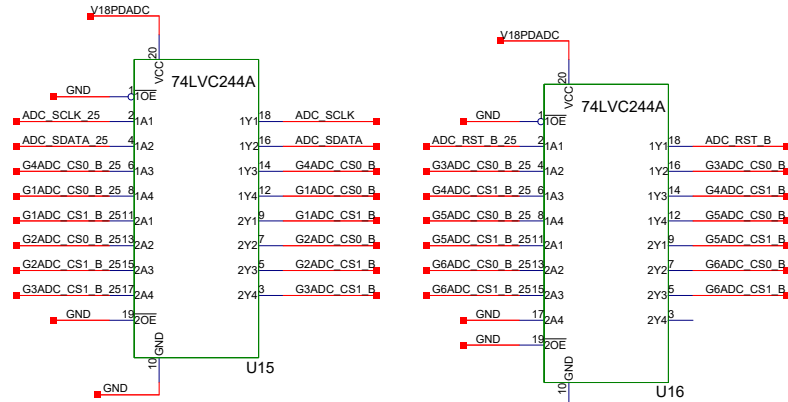
BY
bgb
DATE
24/01/2018:12:28

PROJECT
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FILE
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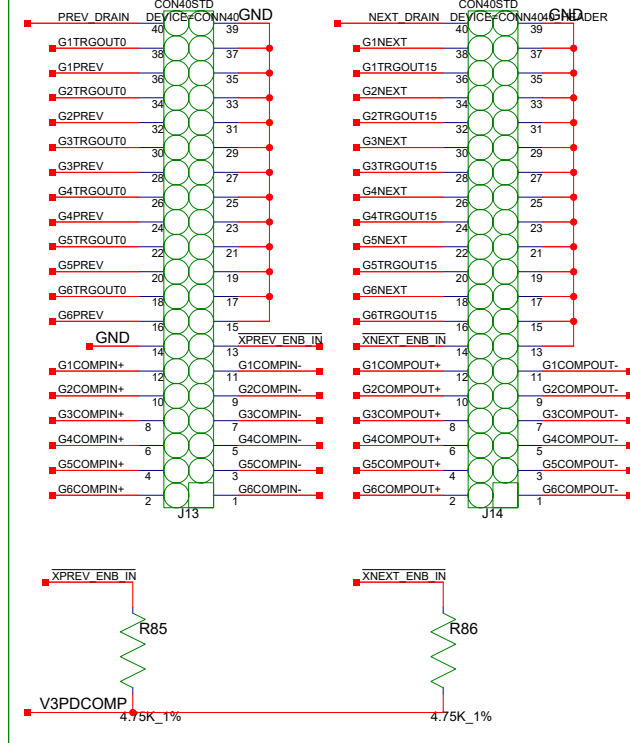
Comparator Level Shifters



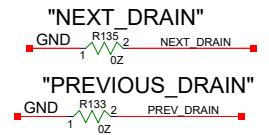
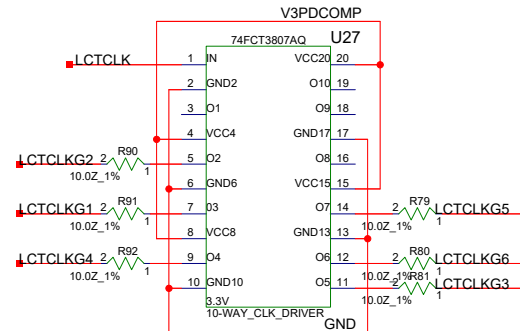
ADC Level Shifters



Comparator Connectors to neighbor CFEBs



Clock Driver for 40MHz Comparator clock



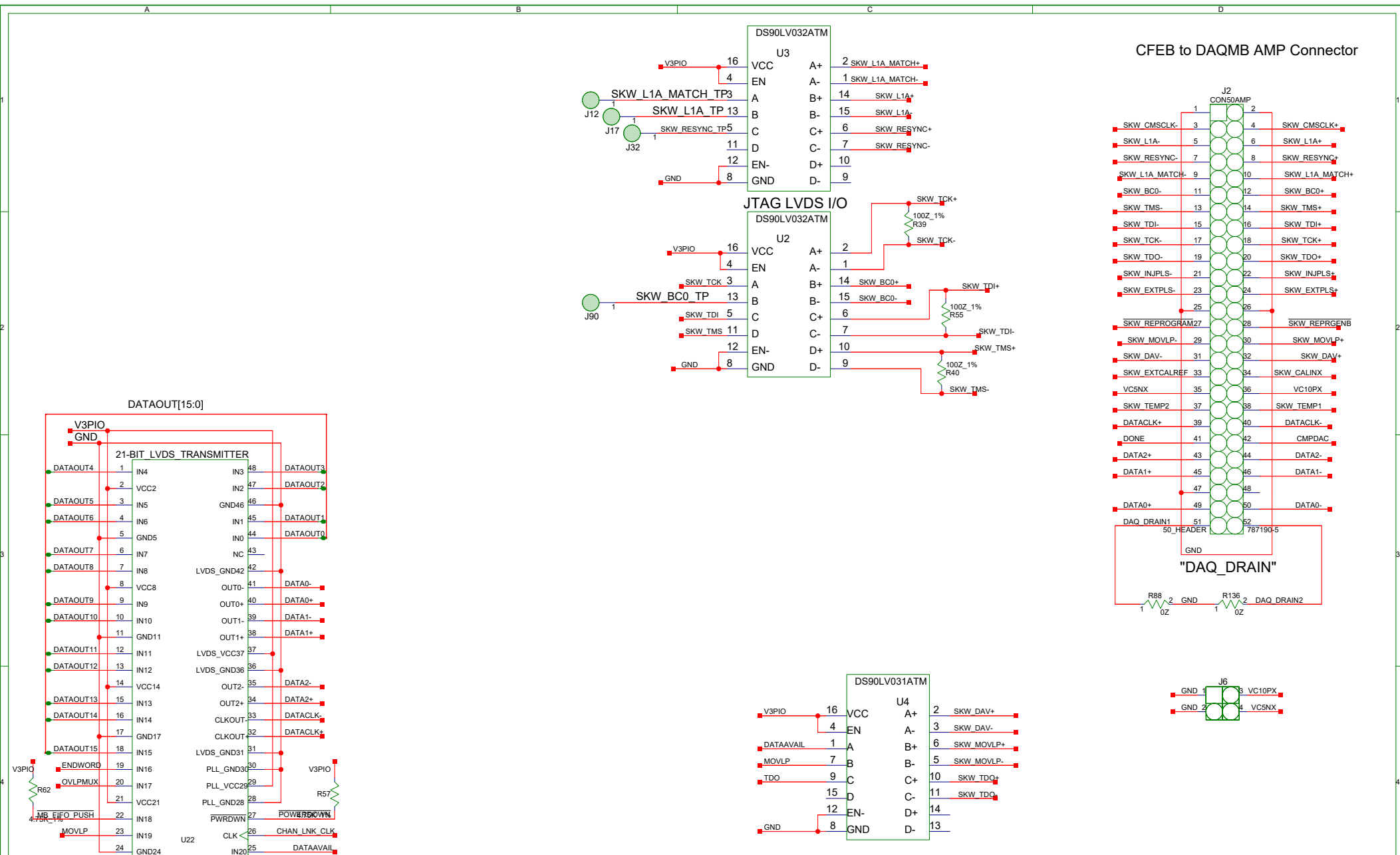
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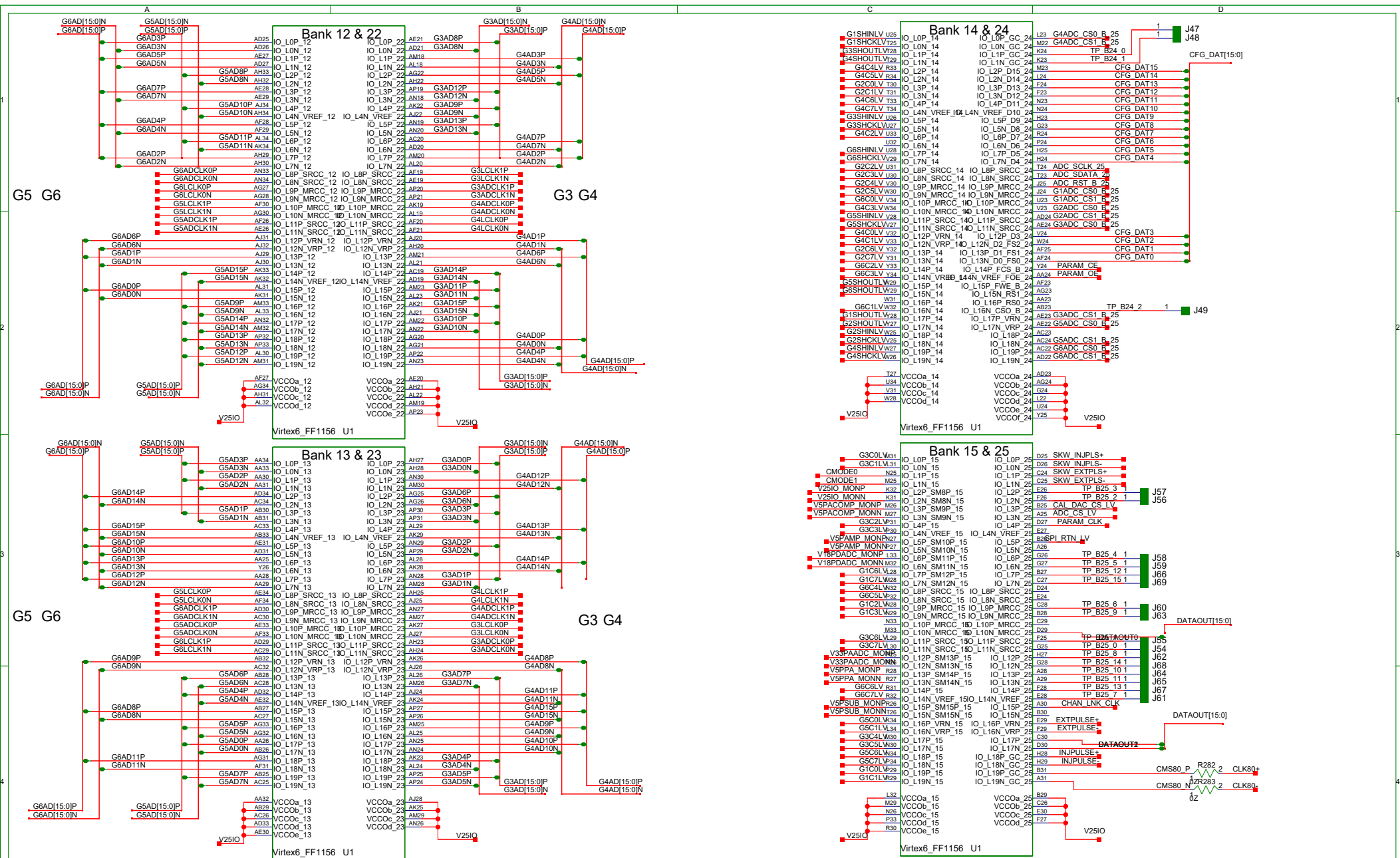
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
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TITLE
ADC and Comparator Interface
Digital Cathode Front-End Board (DCFE)
CMS CSC Electronics

BY
bgb
DATE
24/01/2018:12:28

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FILE
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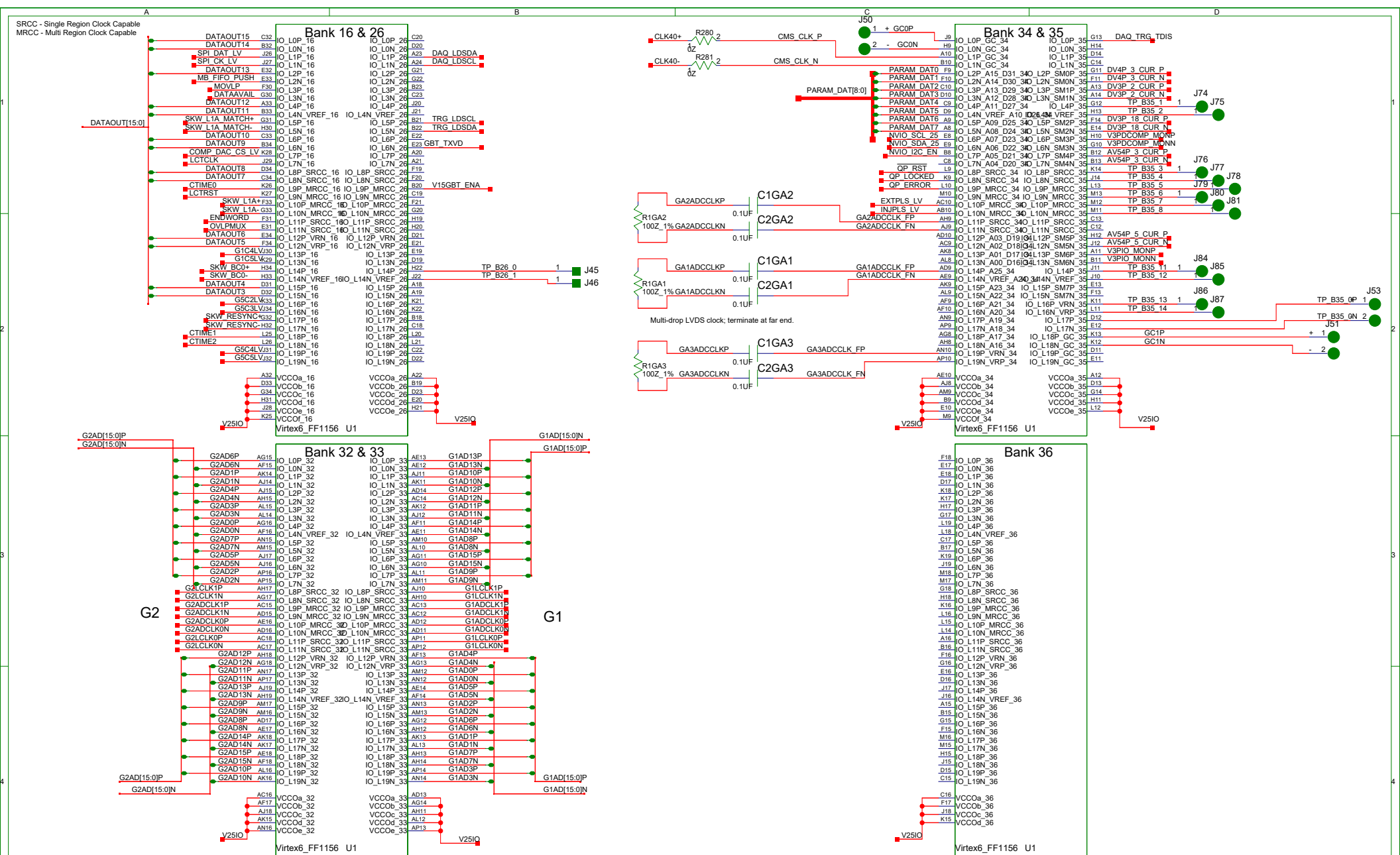
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
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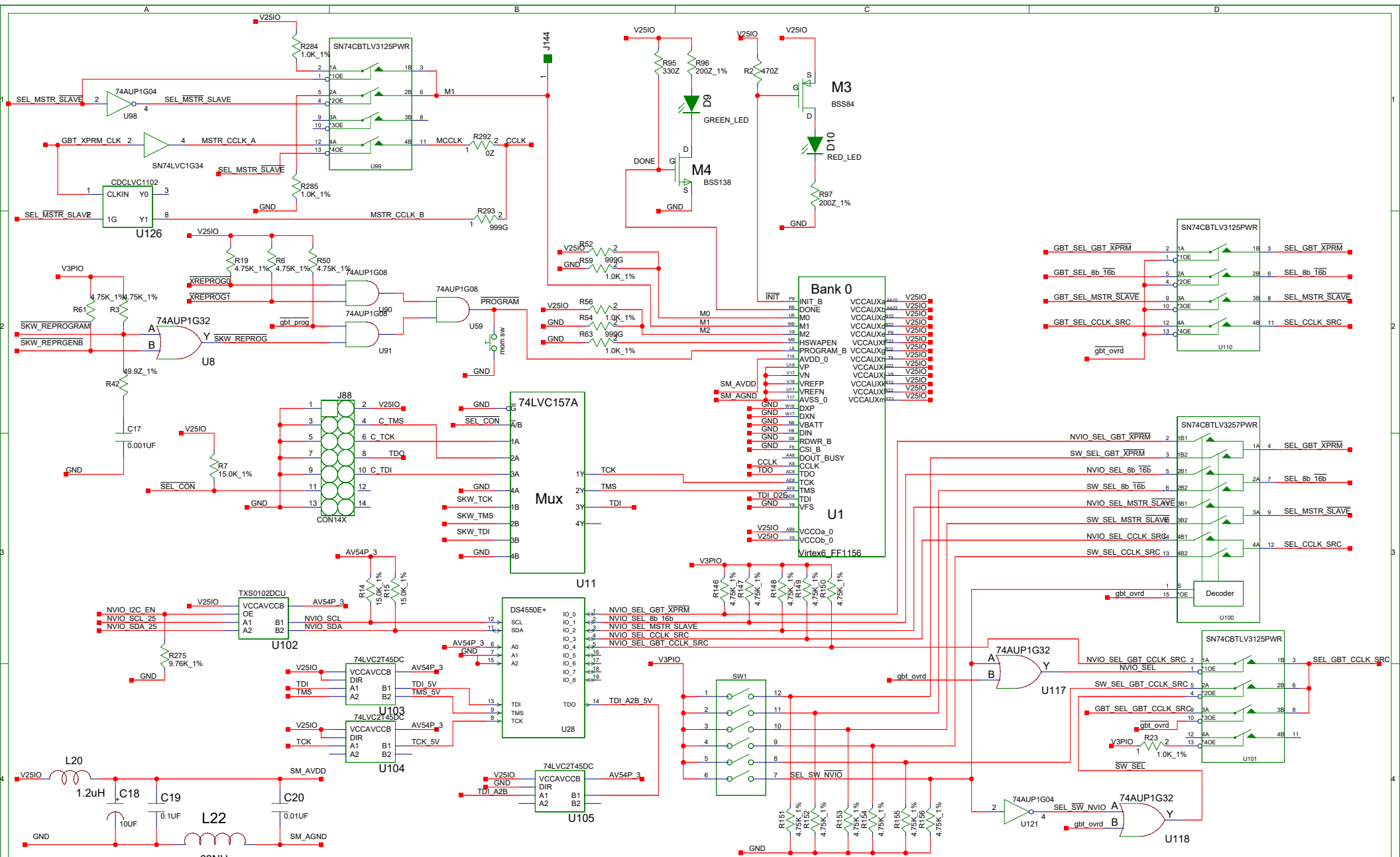
TITLE
Virtex 6 Control FPGA
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY **bgb** PARENT PAGE
DATE 08/02/2018:14:25

PROJECT
xDCFEB
FILE xdcfeb_v2a

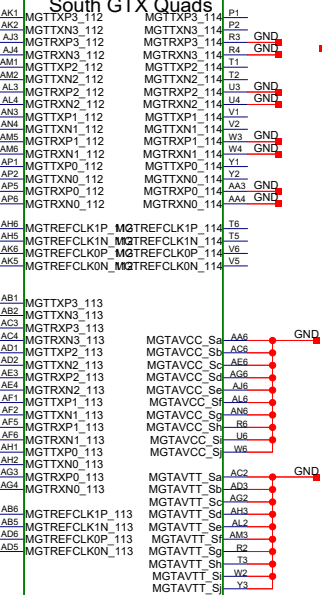
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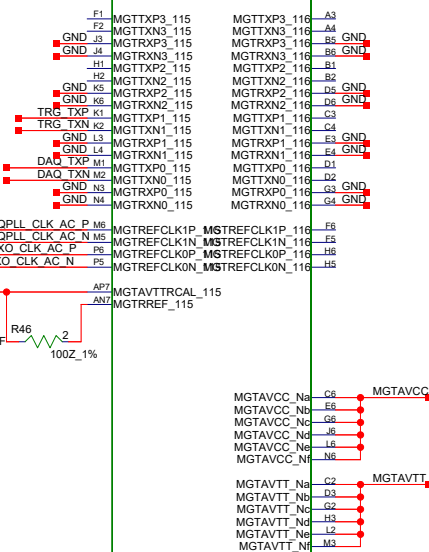
All South Quads Unused

South GTX Quads

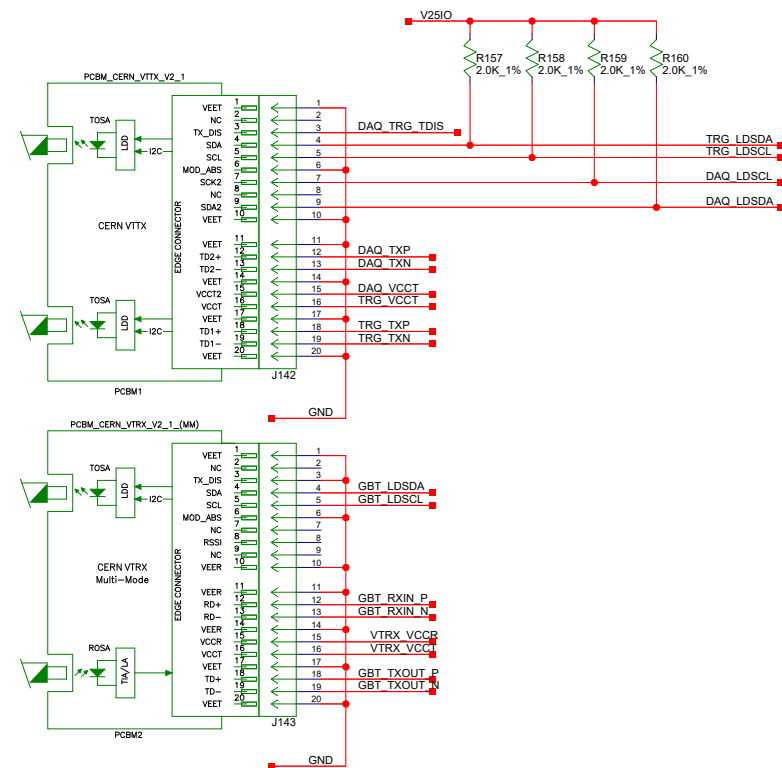


Virtex6_FF1156 U1

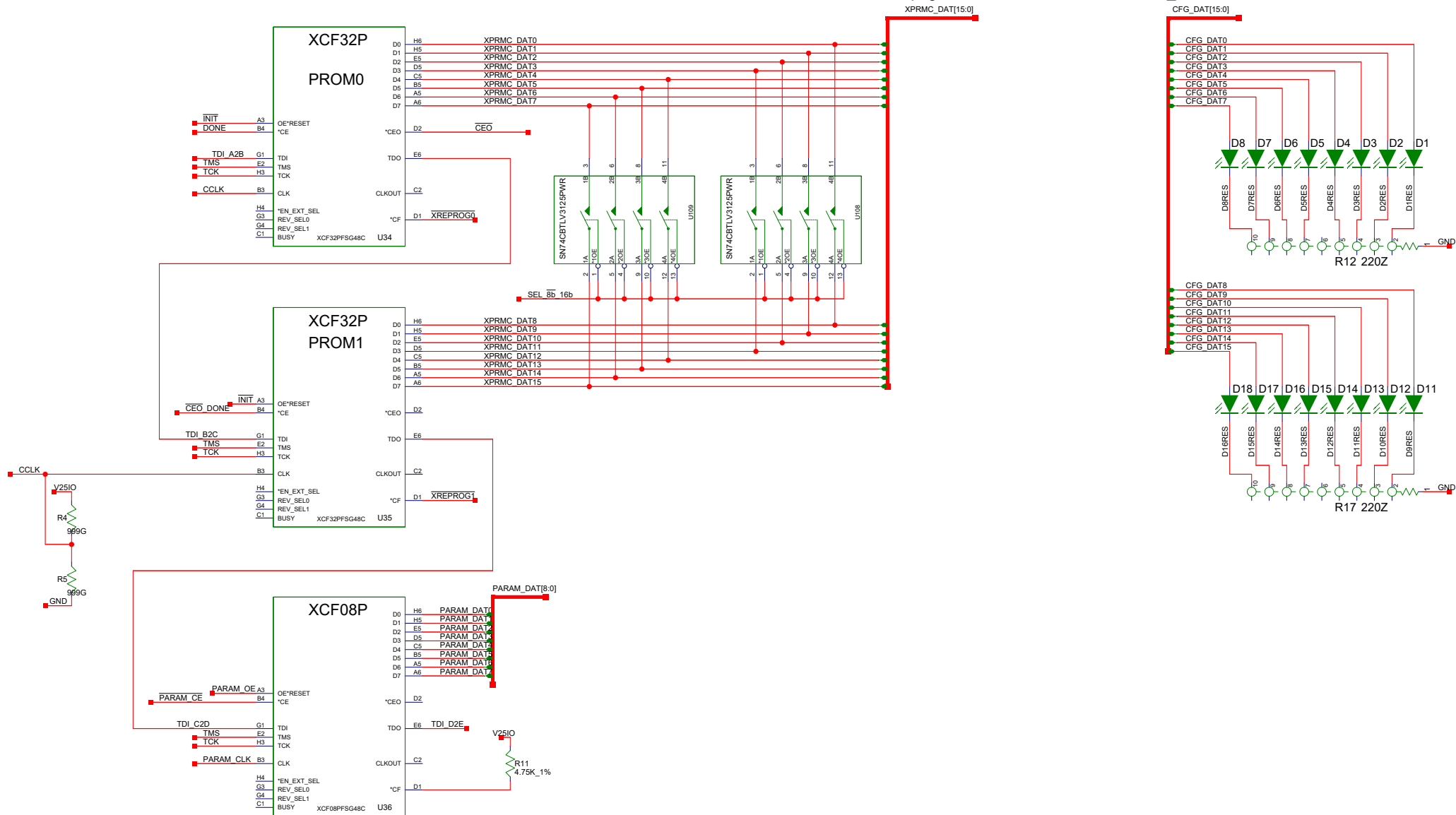
North GTX Quads

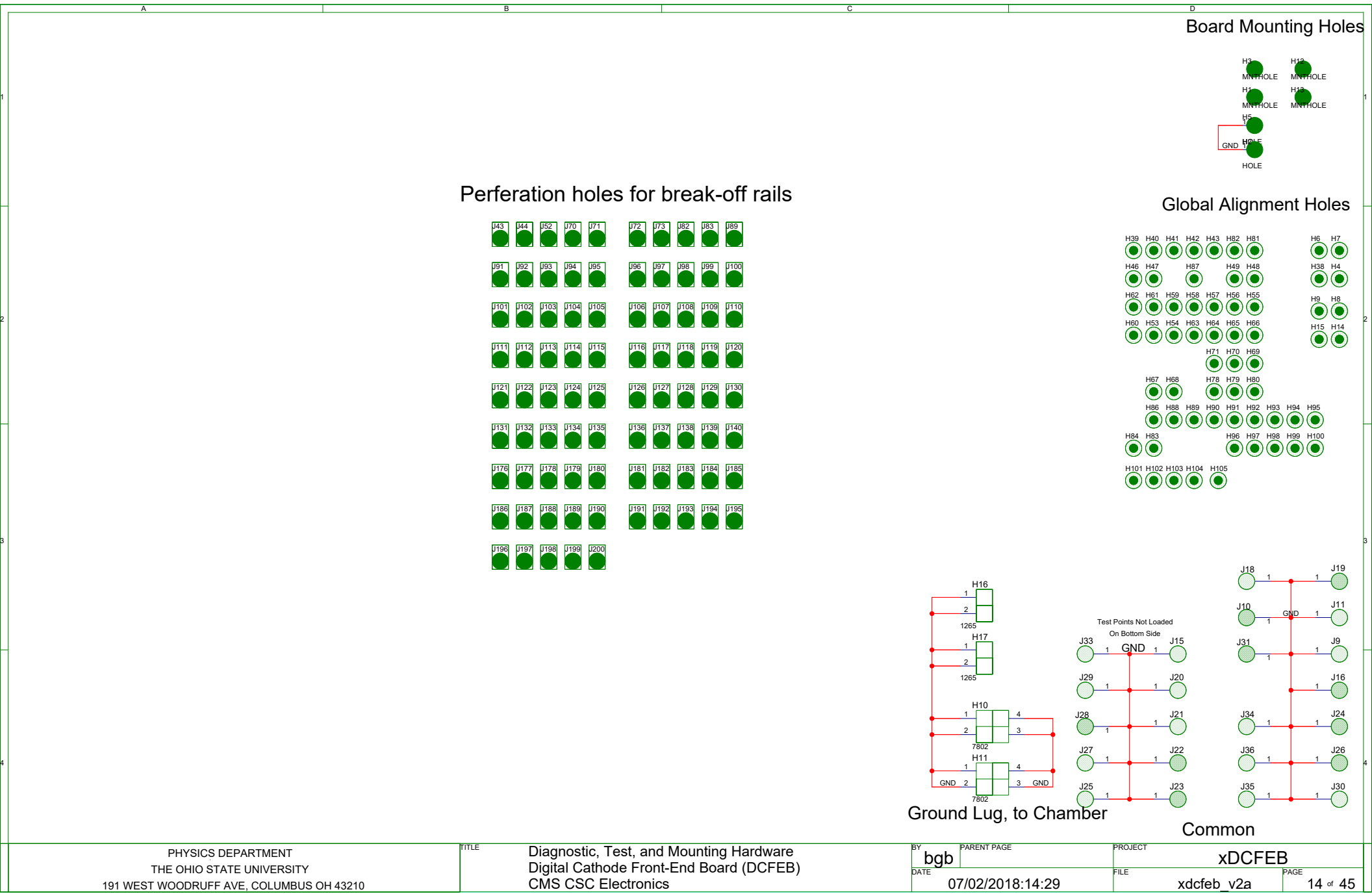


Virtex6_FF1156 U1



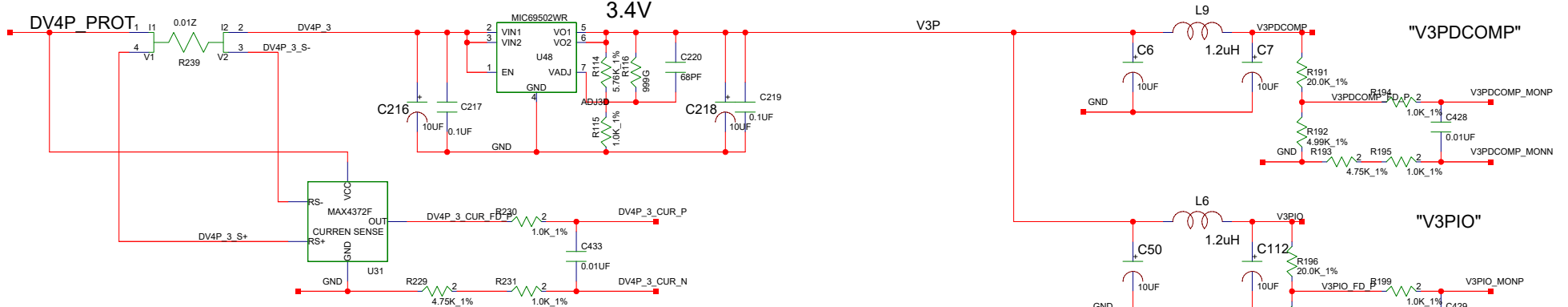
See page 45 for mux connections to CFG_DAT





$$V_o = V_{ref} (1 + R1/R2); V_{ref}=0.5$$

3.4V

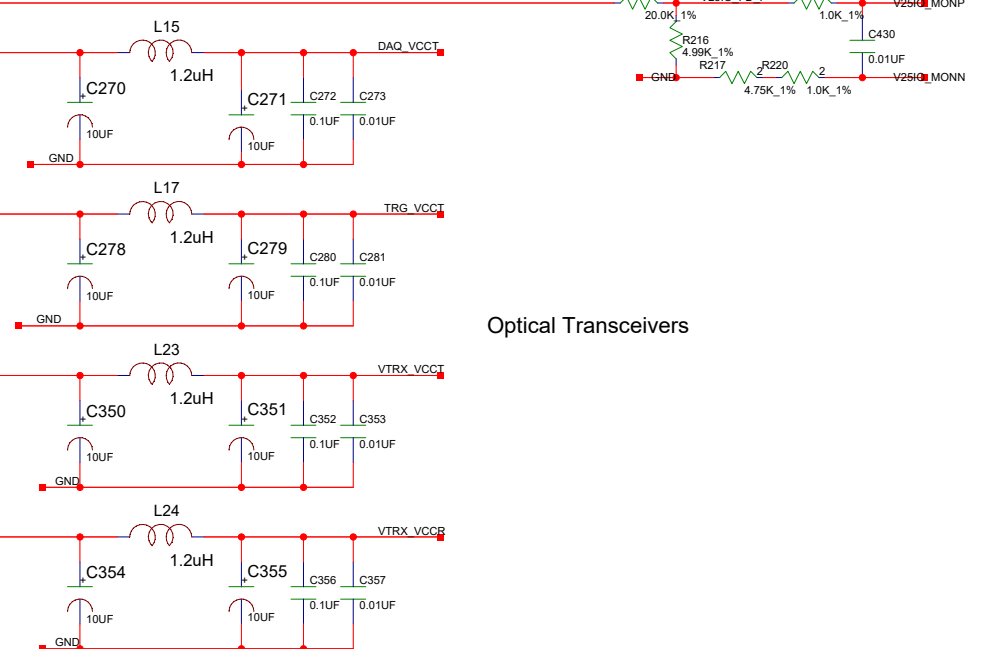


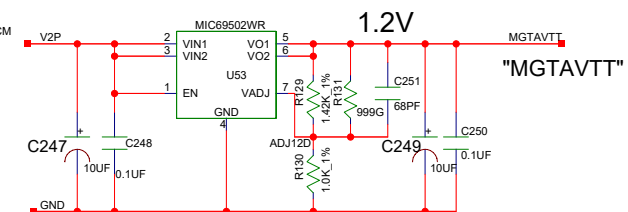
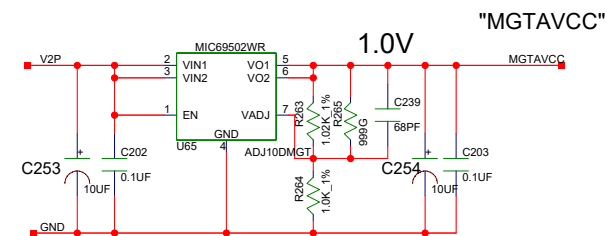
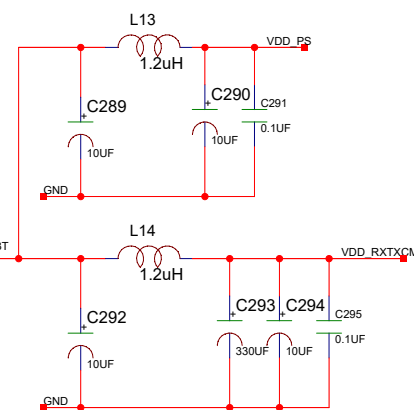
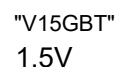
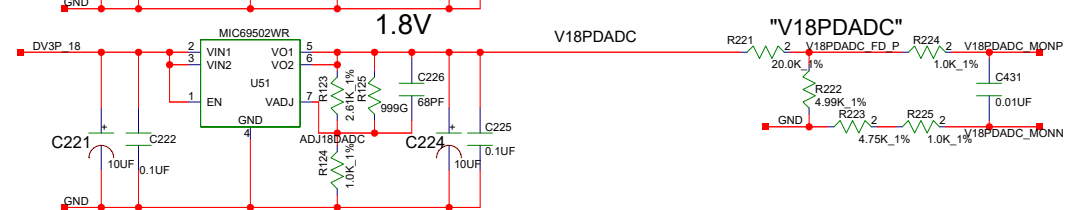
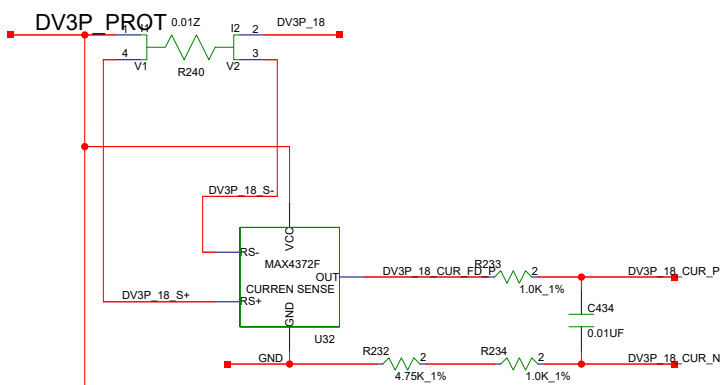
"V3PDCOMP"

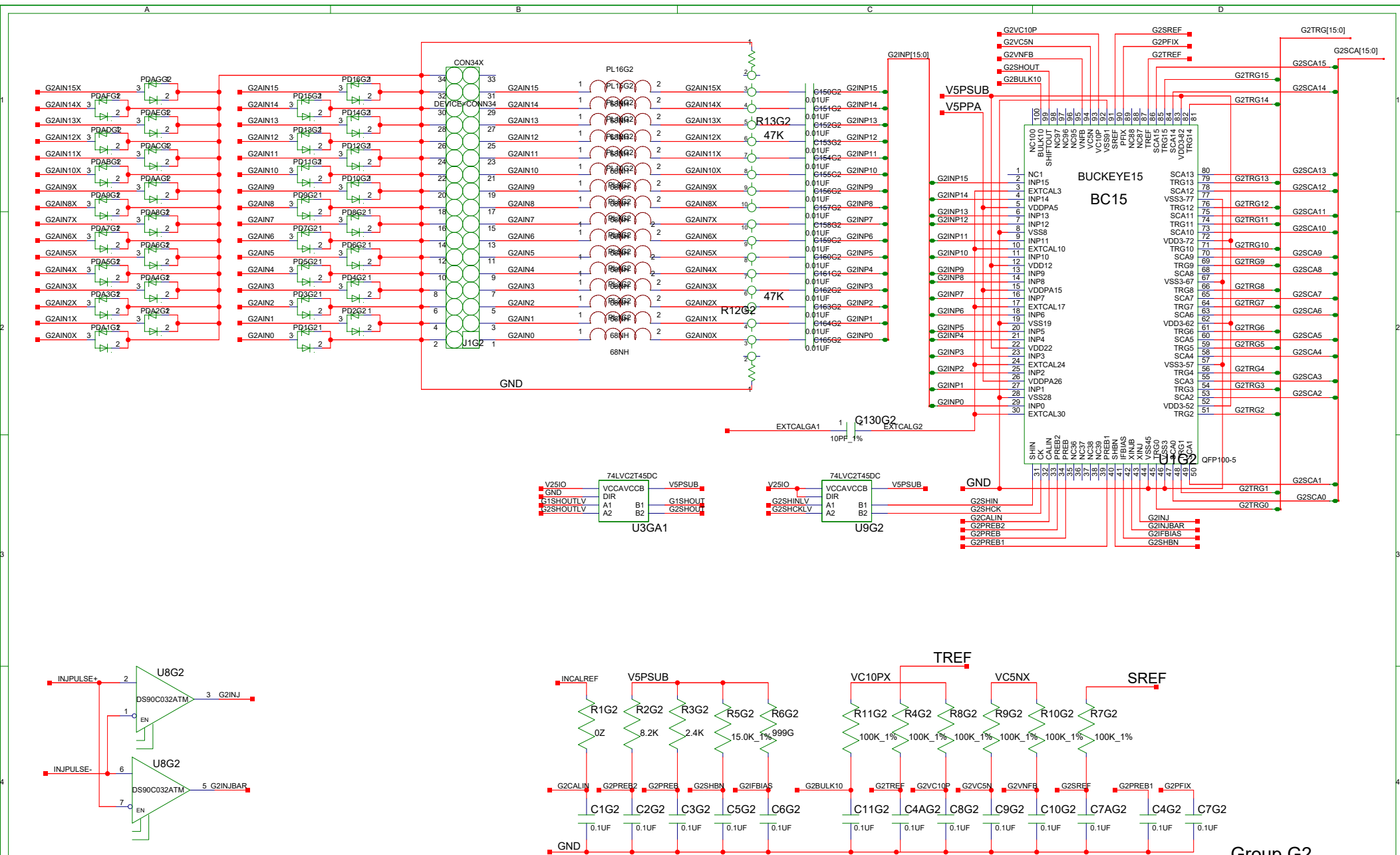
"V3PIO"

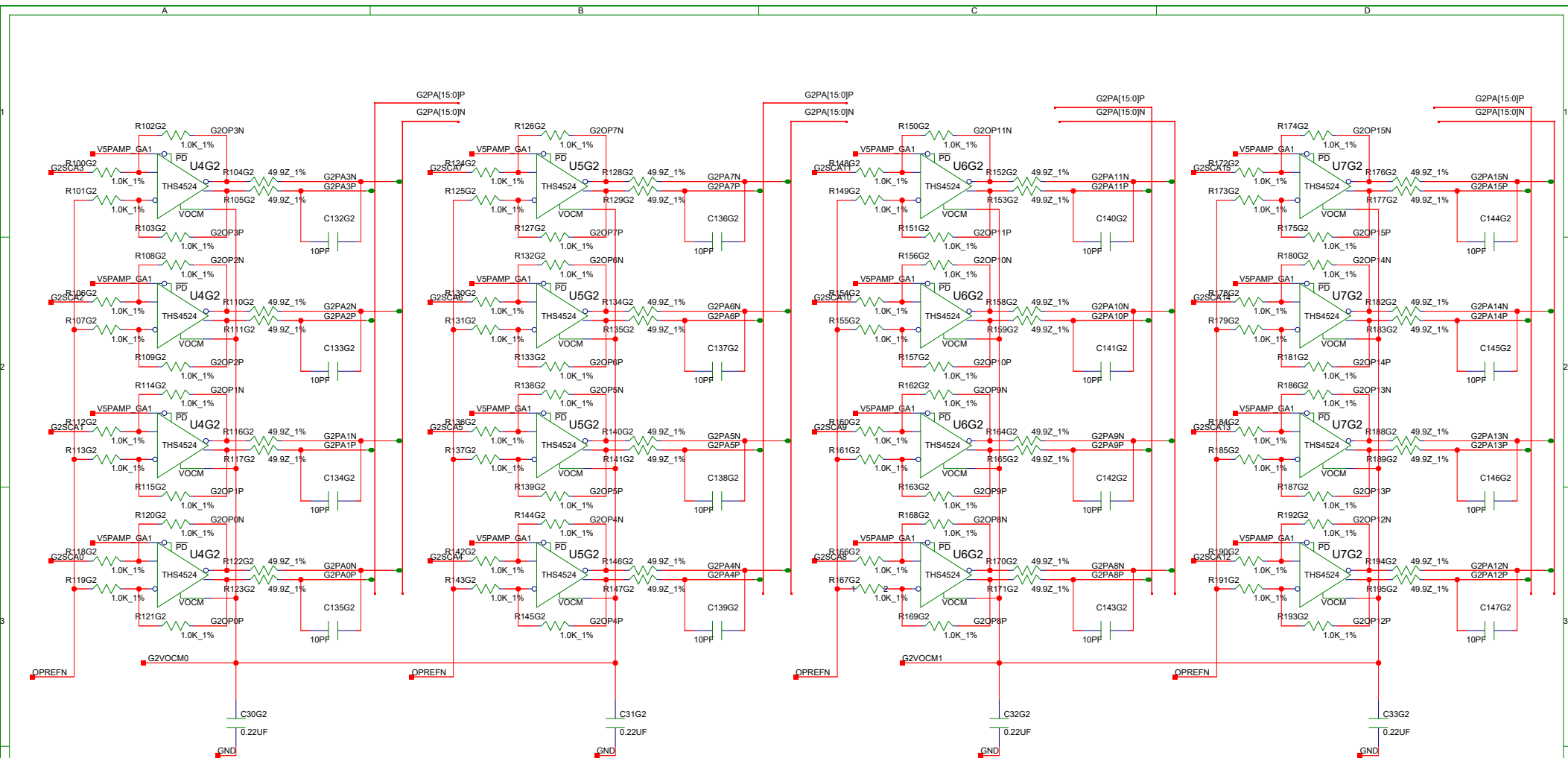
"V25IO also VCCAUX"
V25IO

Optical Transceivers









Group G2 (and GA1)

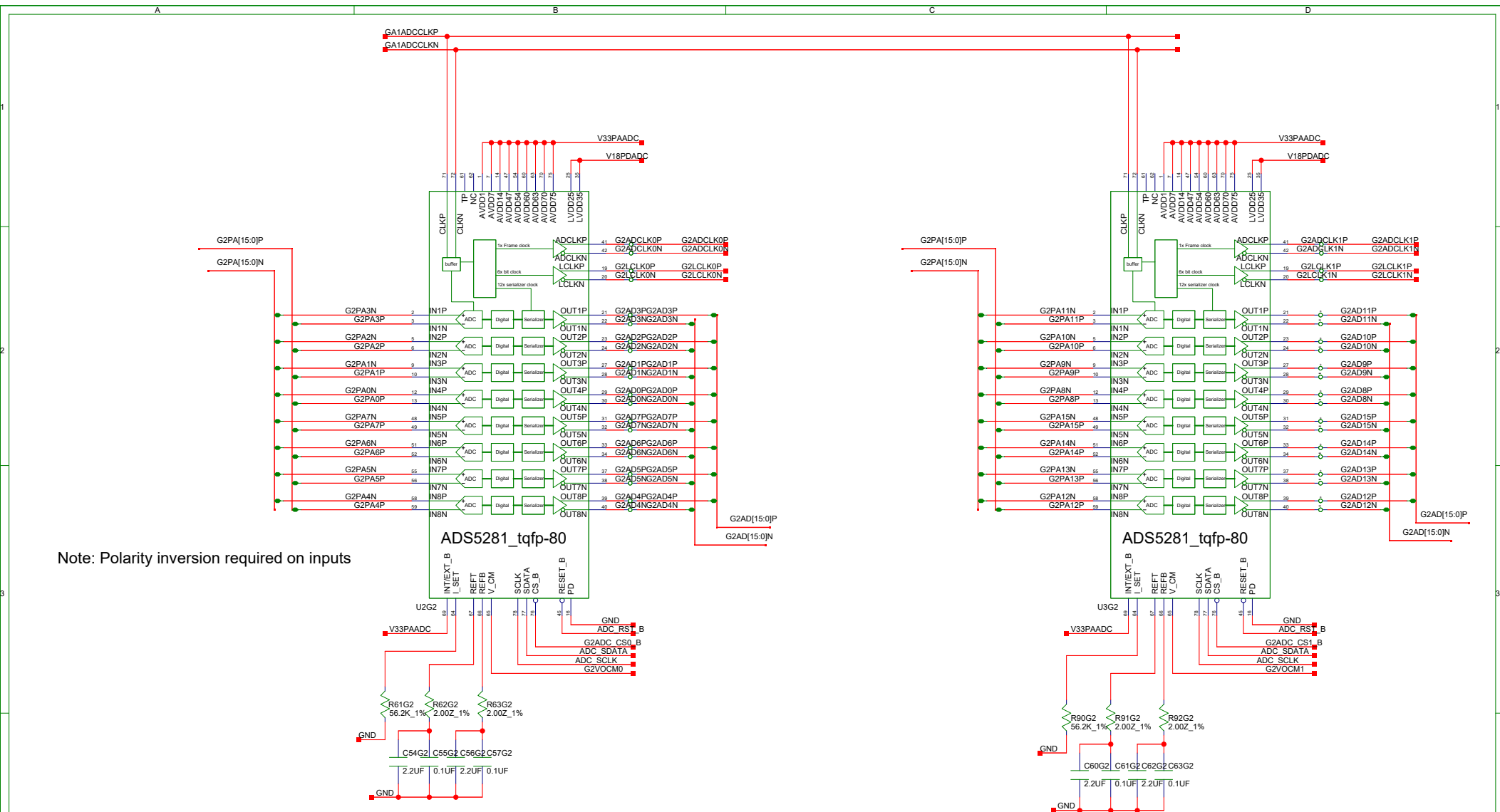
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE
Pre-Amp to ADC Interface
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY
bgb
DATE
24/01/2018:12:30

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xdcfeb_v2a.

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Group G2 (and GA1)

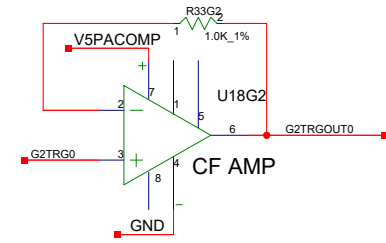
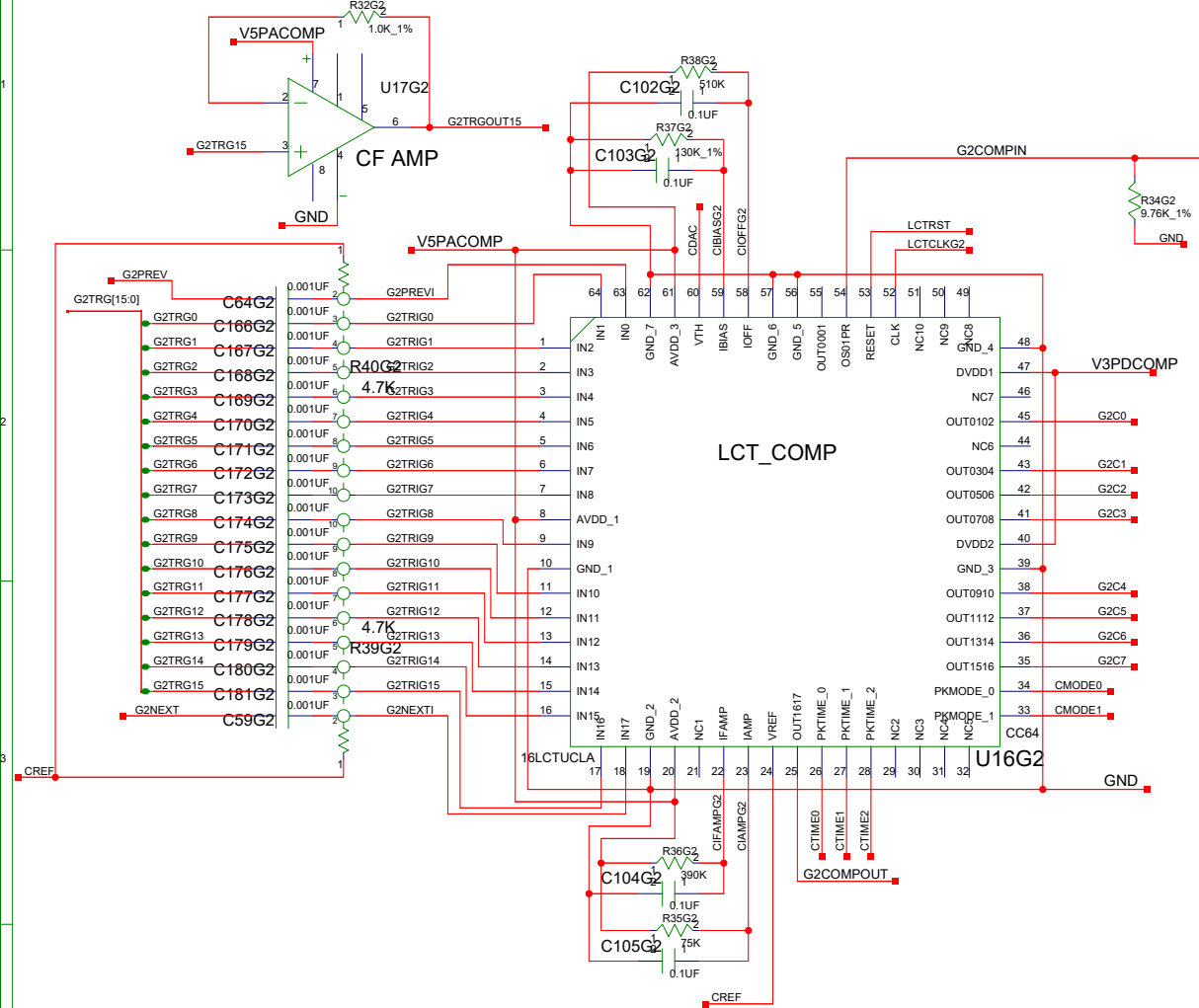
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE
ADC
Digital Cathode Front-End Board (DCFE)
CMS CSC Electronics

BY
bgb
DATE
24/01/2018:12:30

PROJECT
xDCFEb
FILE
xdcfeb_v2a
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Put the op-amps near the branch point of the traces!



Group G2

PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
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TITLE

Cathode Comparator System
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY

PARENT PAGE

bgb

DATE

24/01/2018:12:31

PROJECT

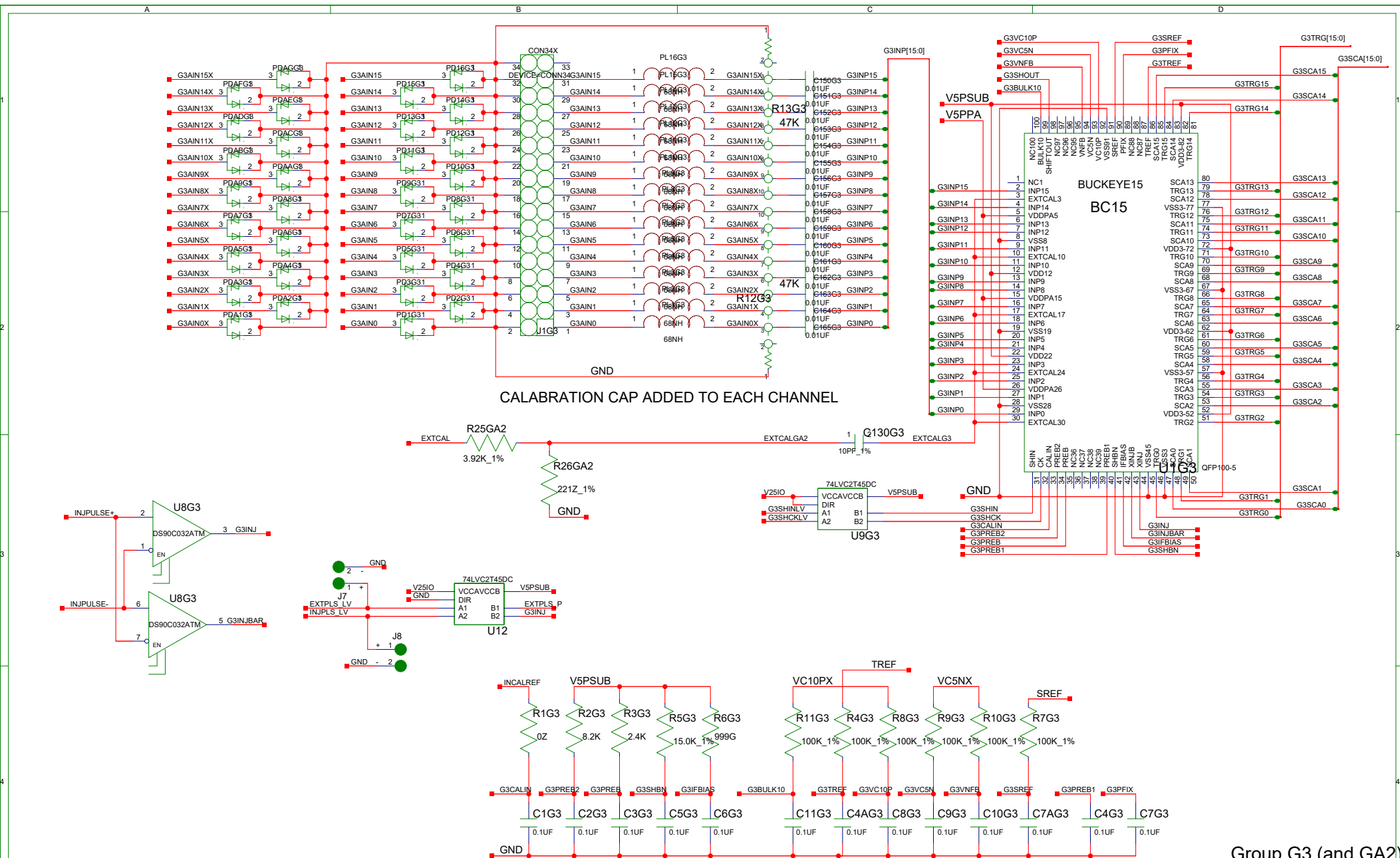
xDCFEB

FILE

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Group G3 (and GA2)

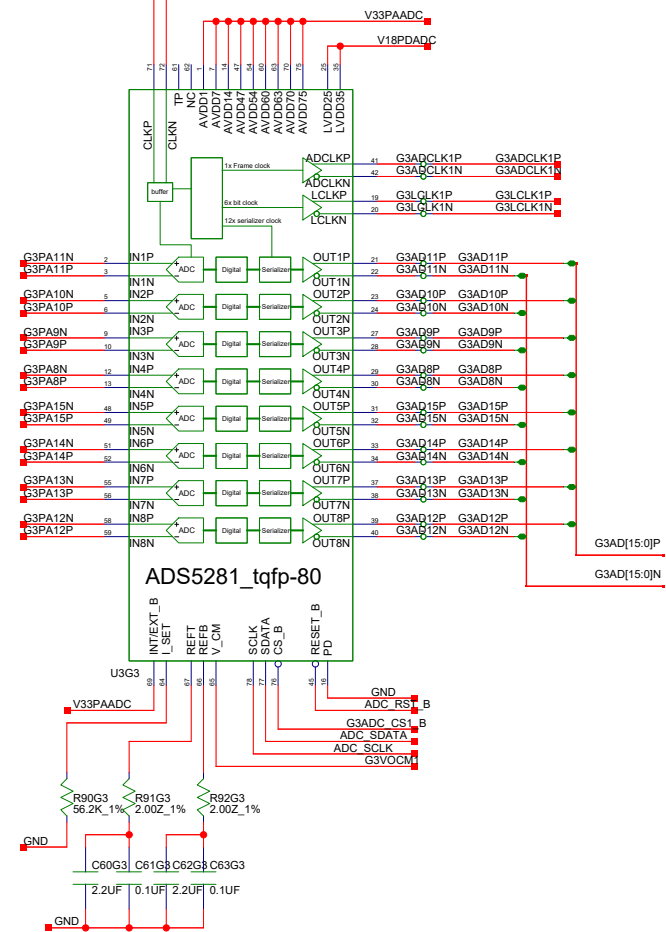
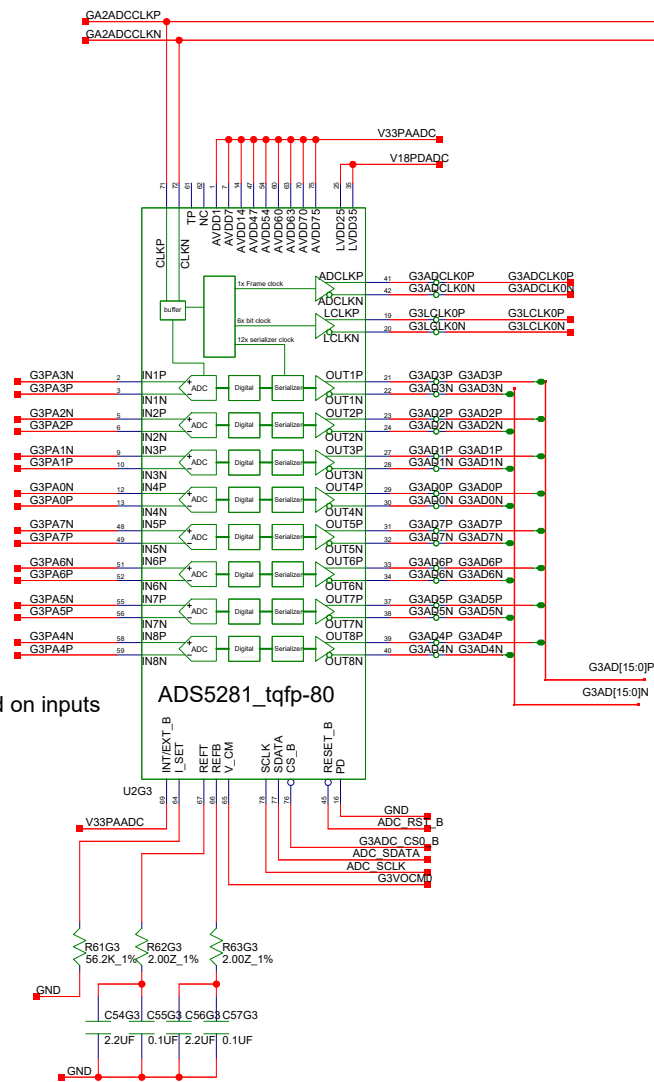
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE Buckeye Chip
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

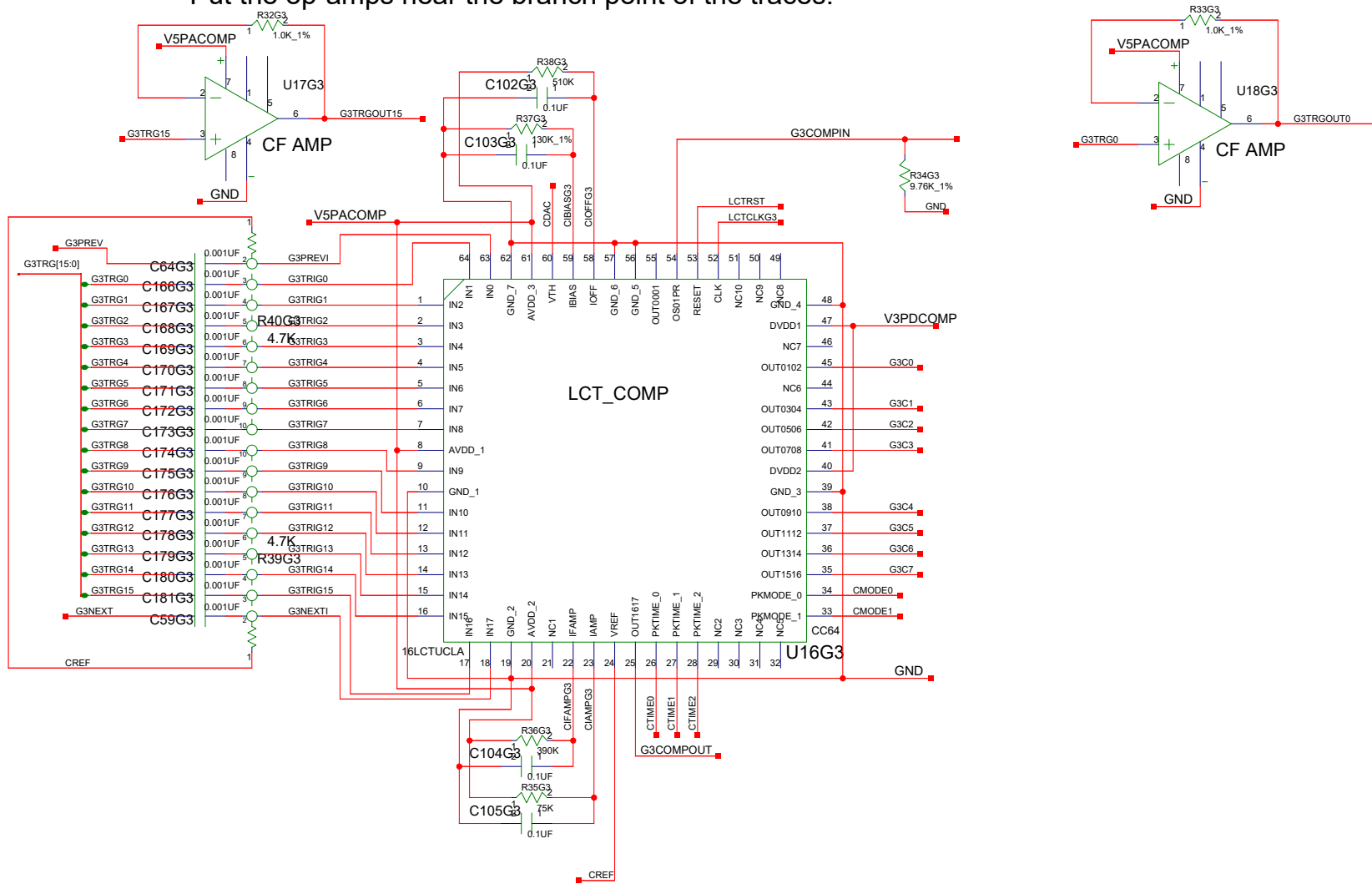
BY bbg
DATE 24/01/2018:12:31

PROJECT xDCFEB
FILE xdcfeb_v2a.

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Put the op-amps near the branch point of the traces!



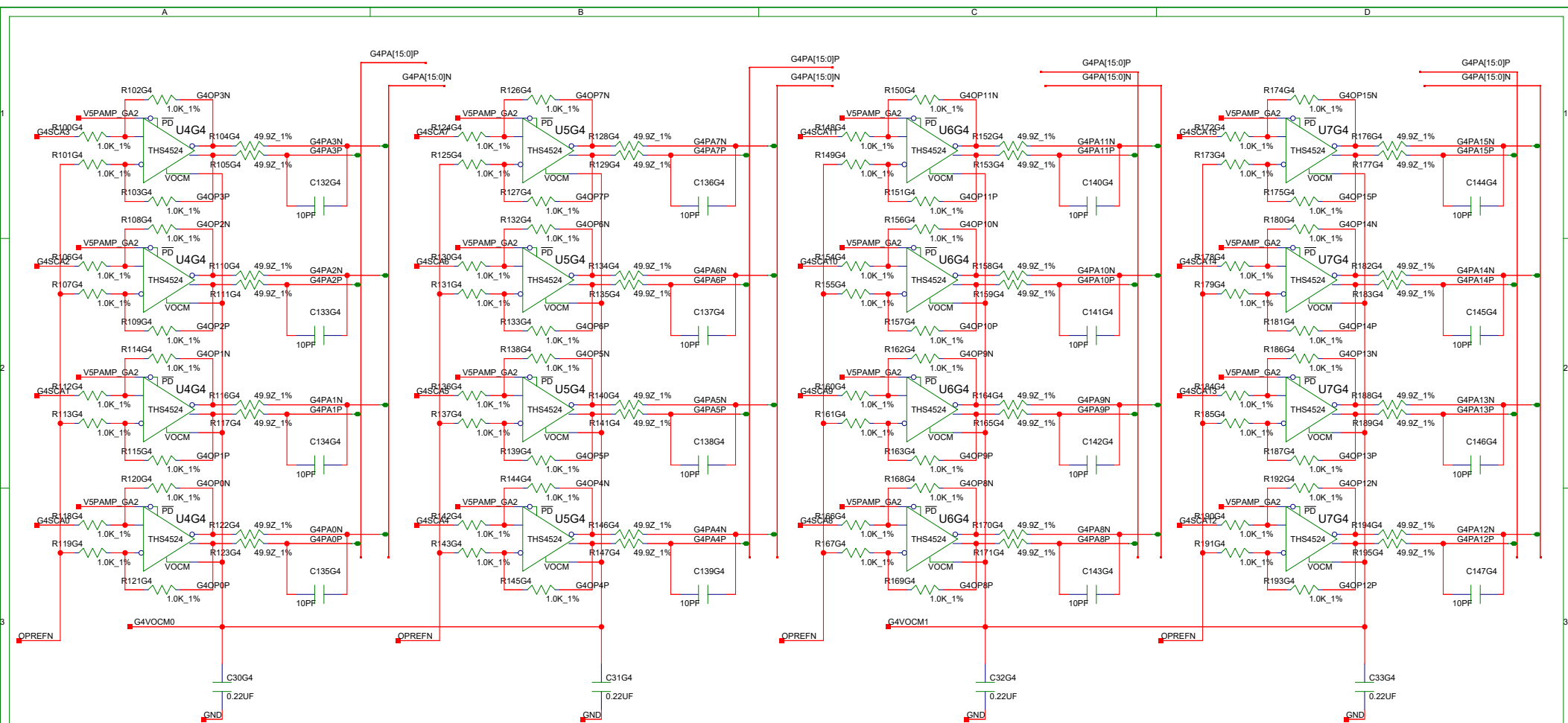
Group G3

PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
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TITLE
Cathode Comparator System
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

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bgb
DATE
24/01/2018:12:31

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Group G4 (and GA2)

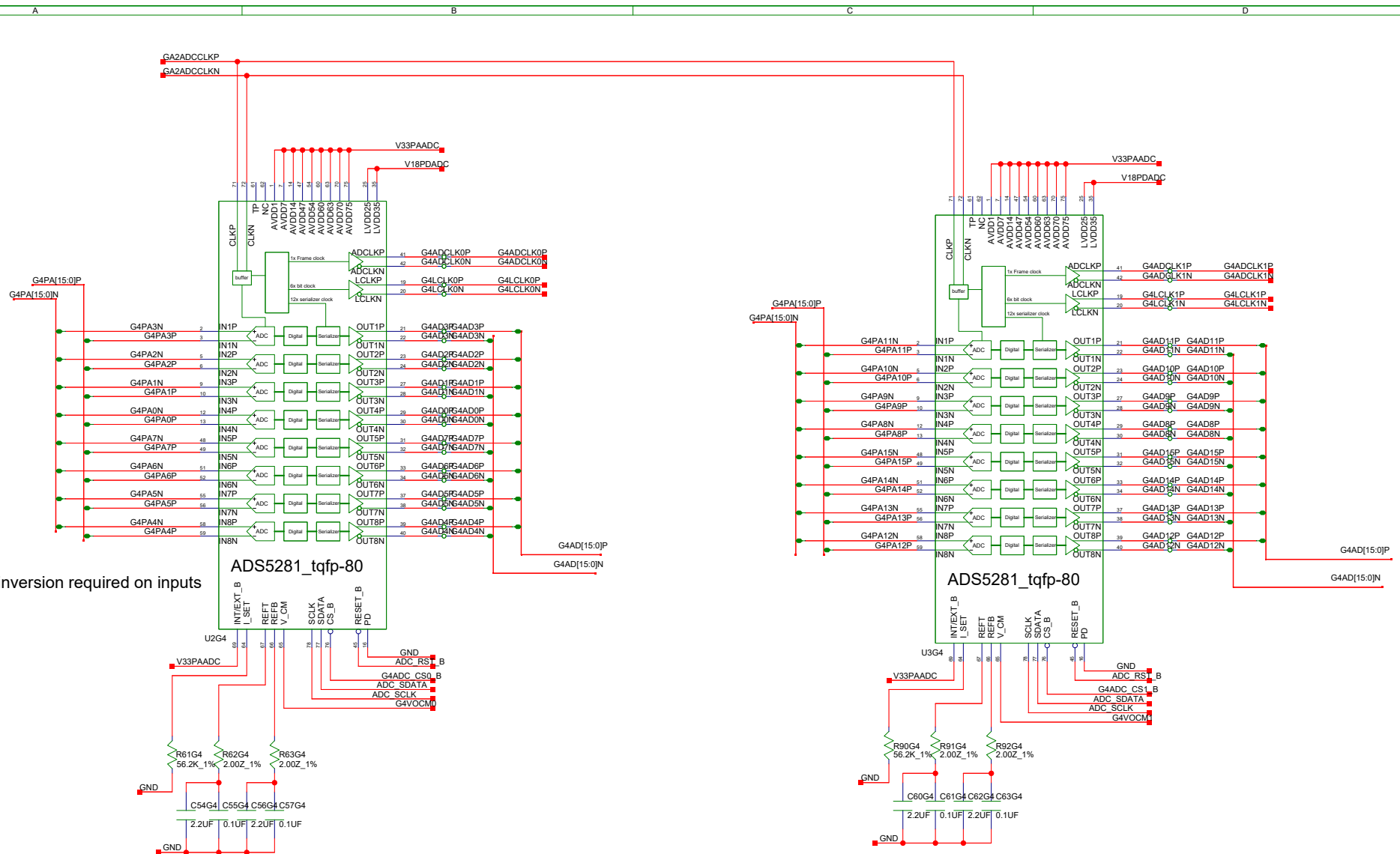
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE
Pre-Amp to ADC Interface
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY
bgb
DATE
30/01/2018:16:59

PROJECT
xDCFEB
FILE
xdcfeb_v2a

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Group G4 (and GA2)

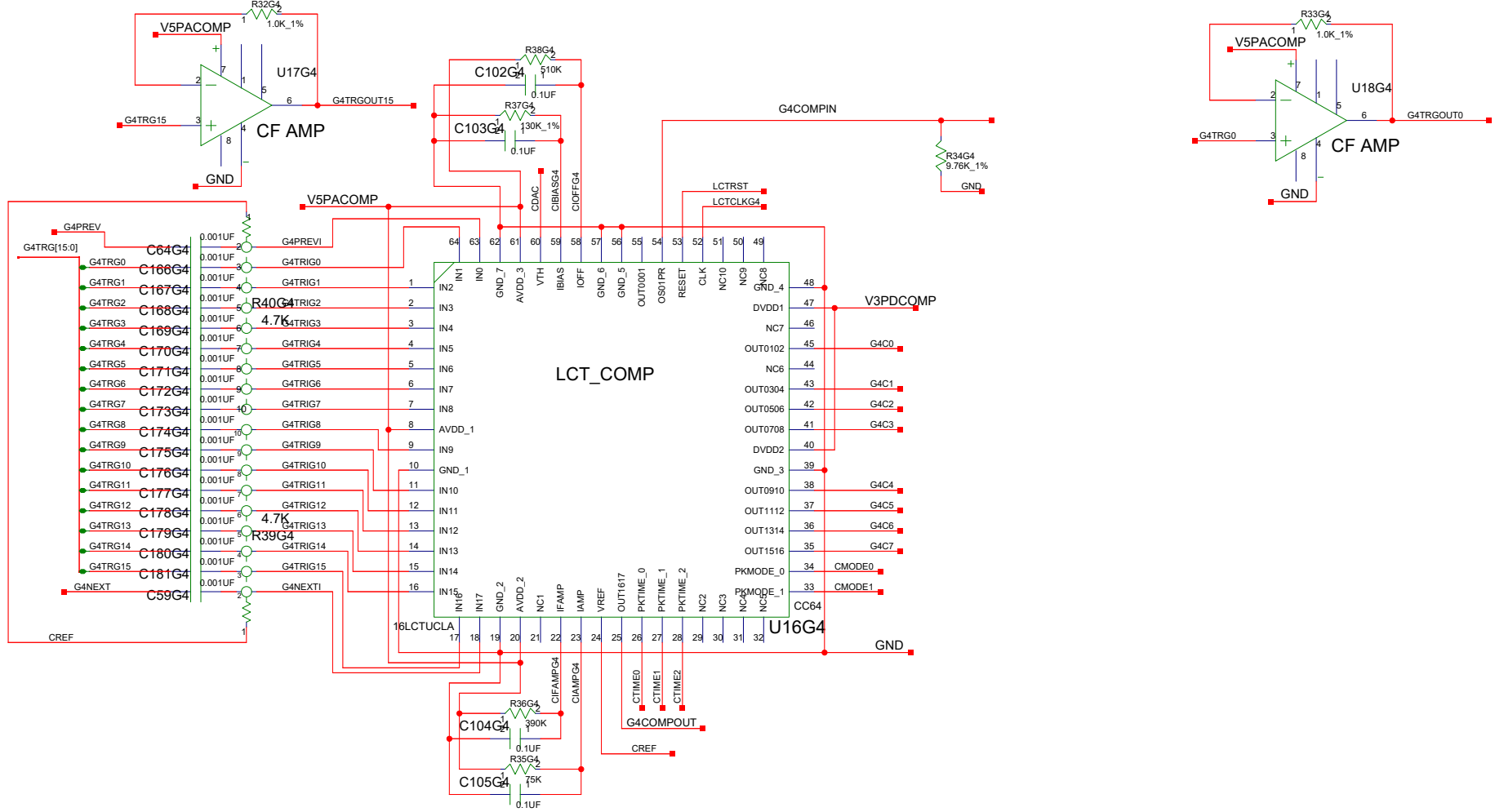
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE
ADC
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY
bgb
DATE
24/01/2018:12:32

PROJECT
xDCFEB
FILE
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Put the op-amps near the branch point of the traces!



Group G4

PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
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TITLE

Cathode Comparator System
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY

bgb

PARENT PAGE

DATE

24/01/2018:12:32

PROJECT

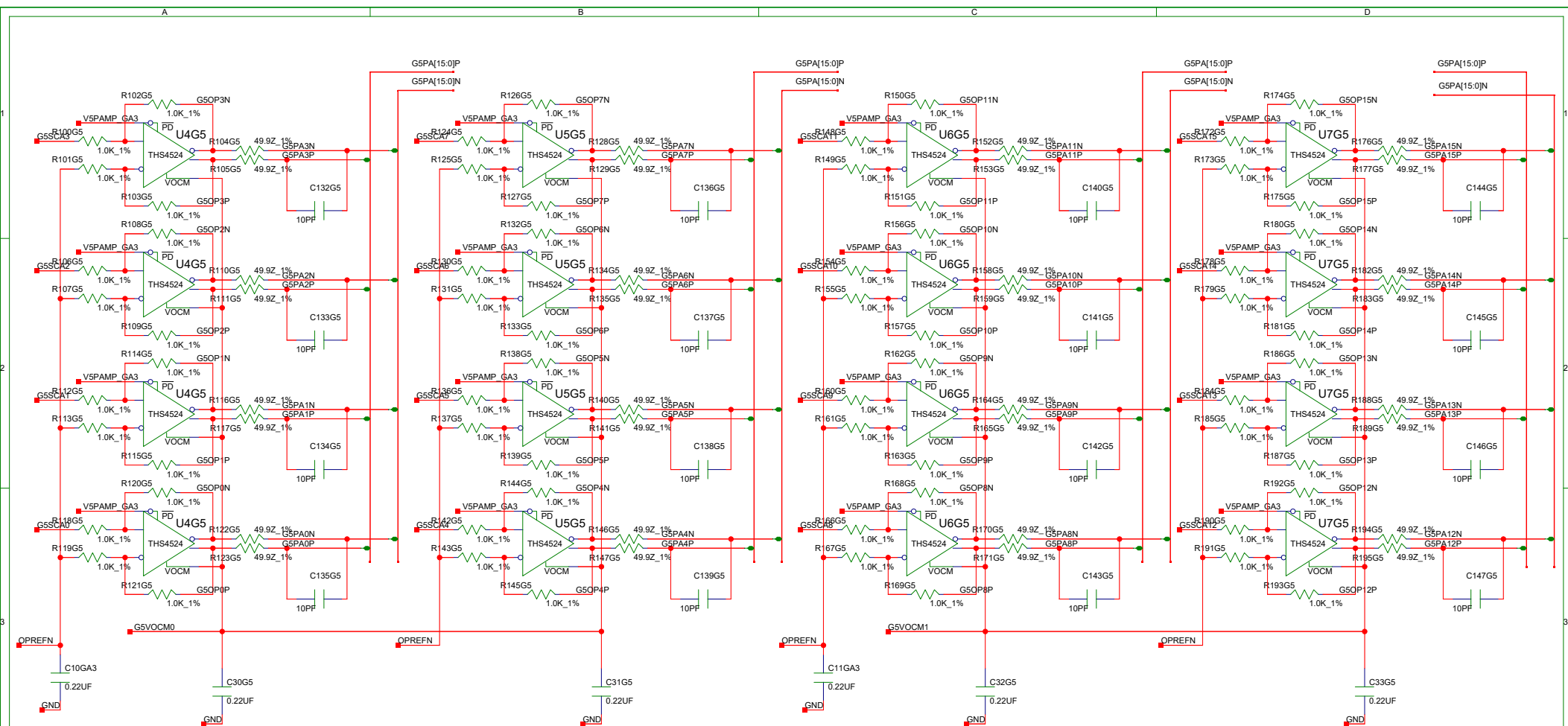
xDCFEB

FILE

xdcfcb_v2a.

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Substitute 887 ohm resistor in signal path to account for 110 ohm source impedance.

For balanced operation at baseline, set baseline to 1.15V and fixed - input to 1.85V

Group G5 (and GA3)

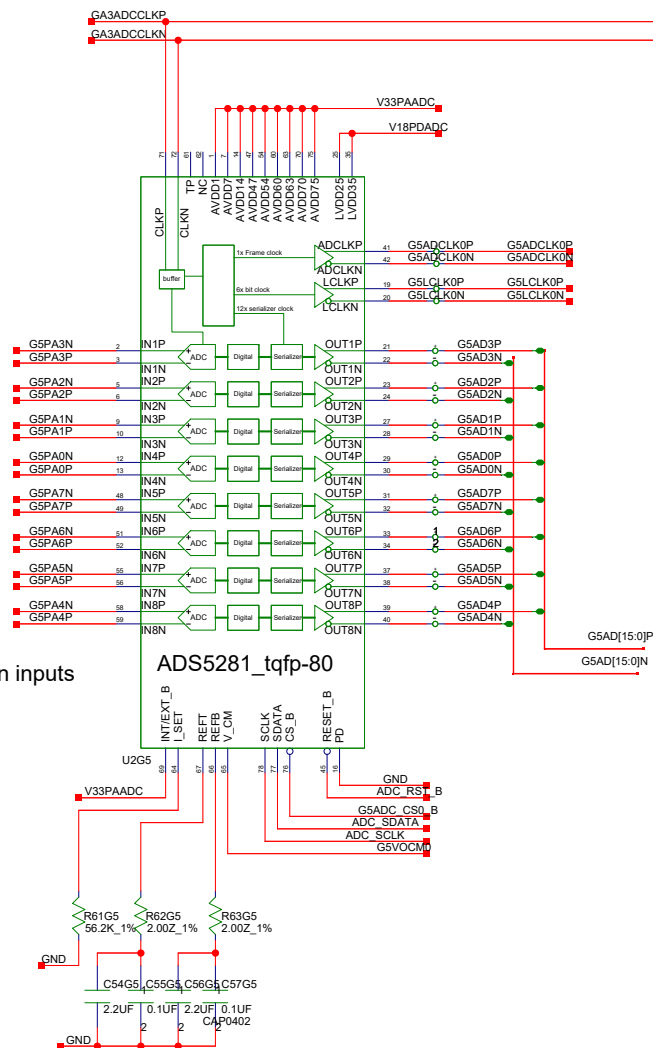
PHYSICS DEPARTMENT
THE OHIO STATE UNIVERSITY
191 WEST WOODRUFF AVE, COLUMBUS OH 43210

TITLE
Pre-Amp to ADC Interface
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

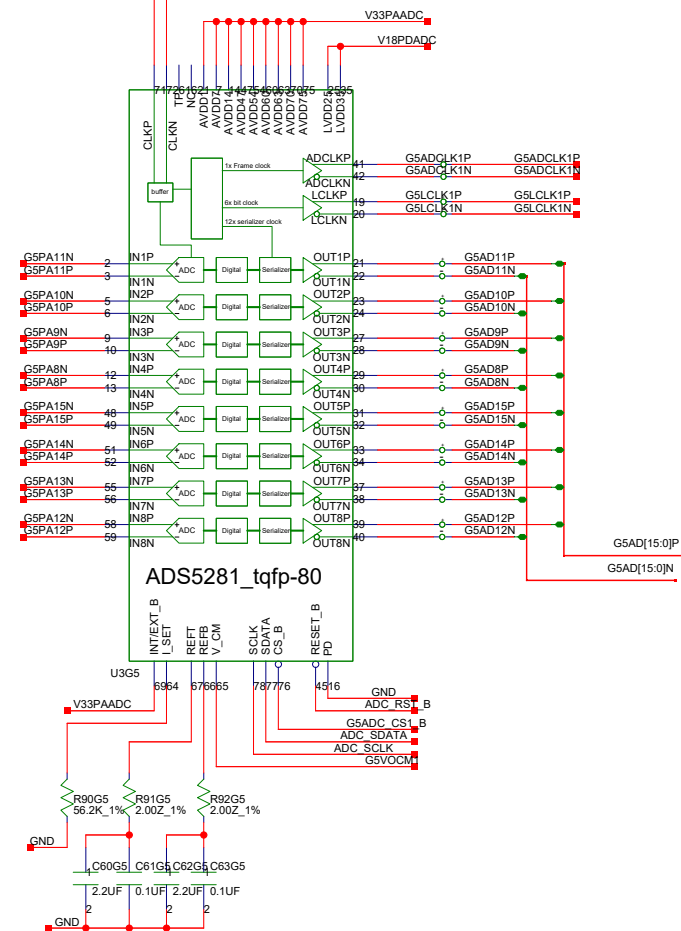
BY
bgb
DATE
24/01/2018:12:32

PROJECT
xDCFEB
FILE
xdcfeb_v2a.

PAGE
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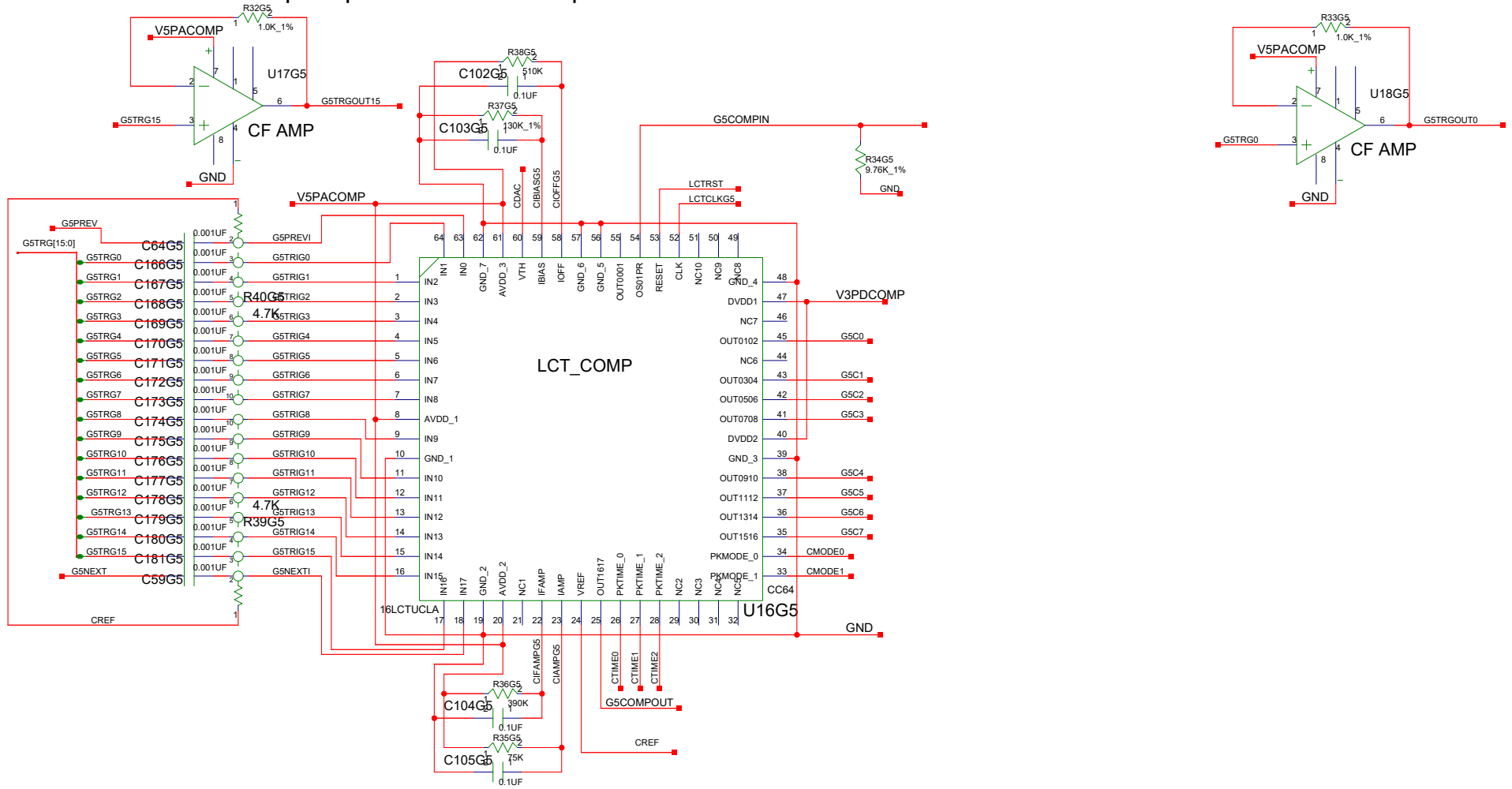


Note: Polarity inversion required on inputs



Group G5 (and GA3)

Put the op-amps near the branch point of the traces!



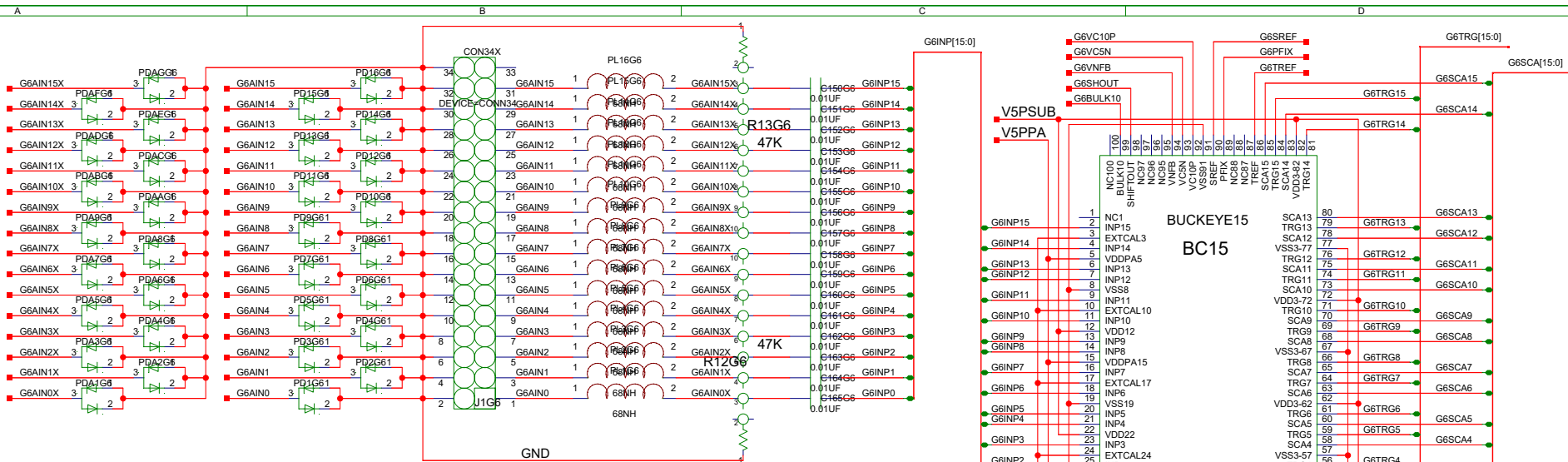
Group G5

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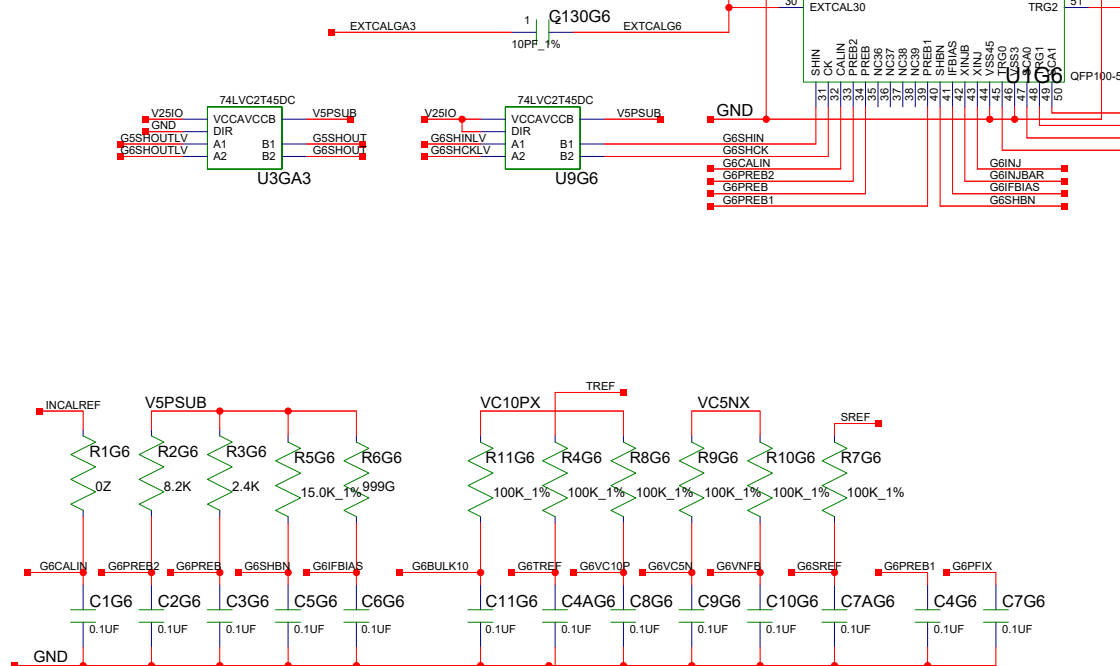
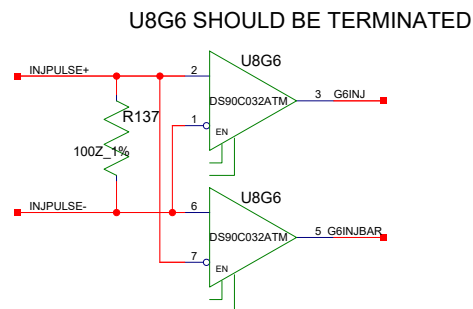
TITLE
Cathode Comparator System
Digital Cathode Front-End Board (DCFEB)
CMS CSC Electronics

BY bbg
DATE 24/01/2018:12:33

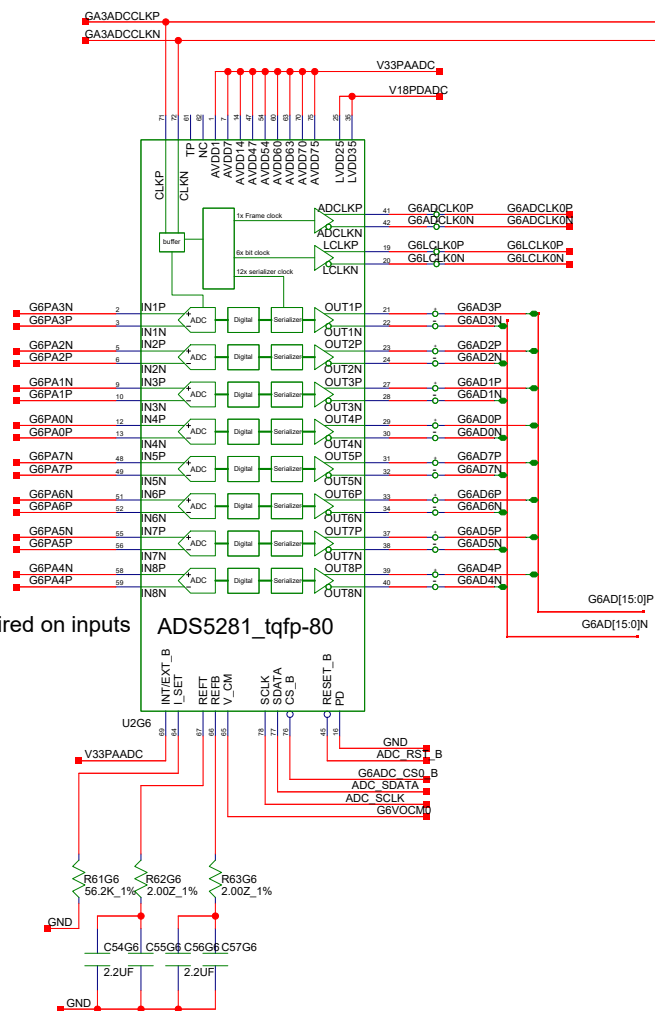
PROJECT xDCFEB
FILE xdcfeb_v2a.
PAGE 33 of 45



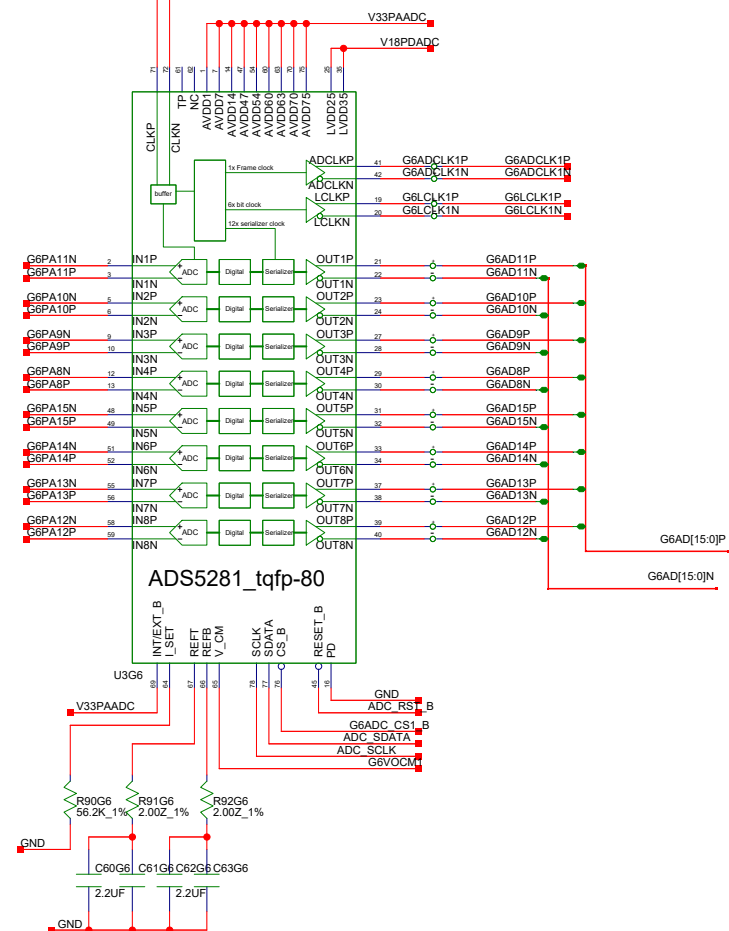
CALABRATION CAP ADDED TO EACH CHANNEL



Group G6
xDCFEB

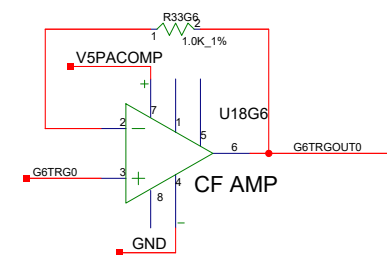
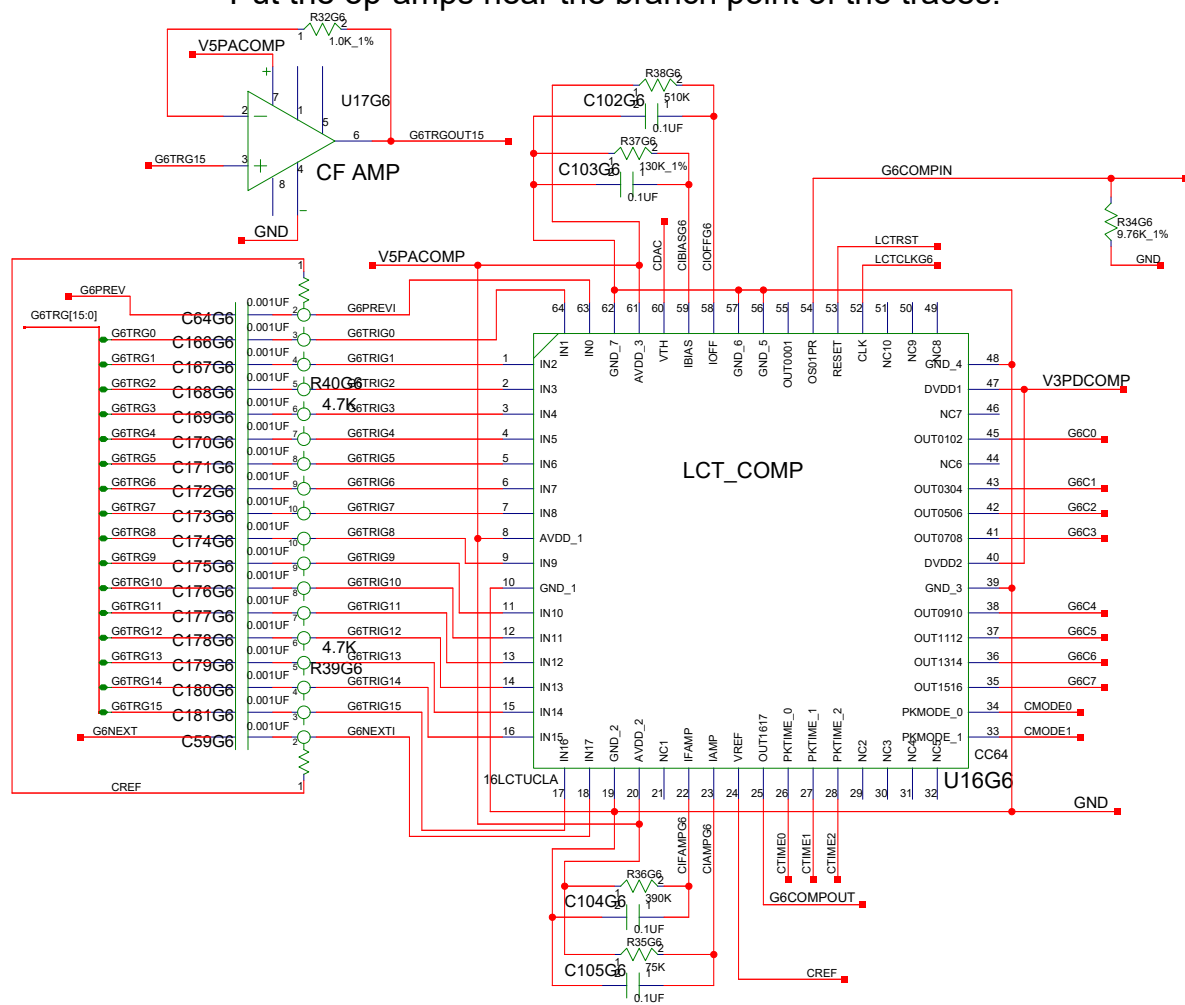


Note: Polarity inversion required on inputs



Group G6 (and GA3)

Put the op-amps near the branch point of the traces!



Group G6

One filter CAP per power pin, one TANT per chip.

Group

Input Amplifier

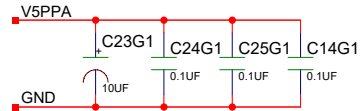
Shaper/Digital

Translators

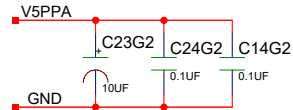
Translators

Group

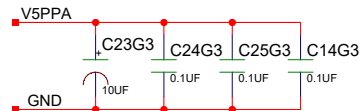
G1



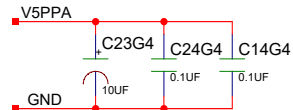
G2



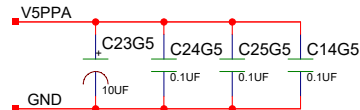
G3



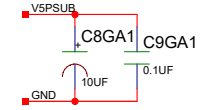
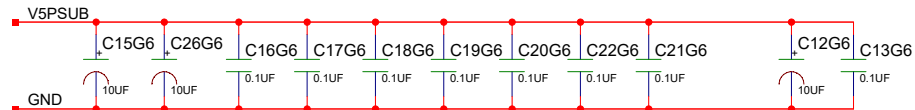
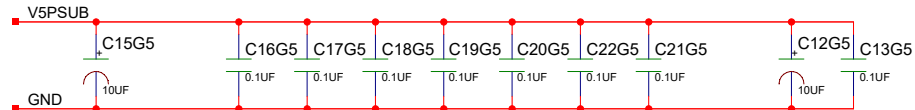
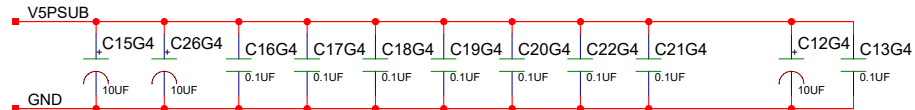
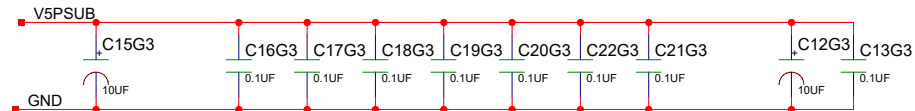
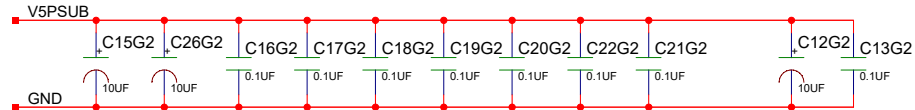
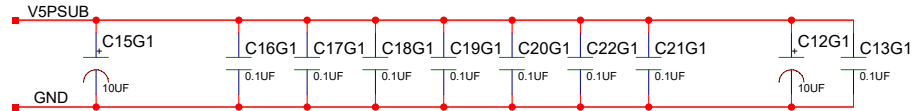
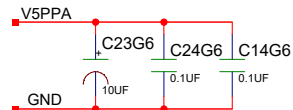
G4



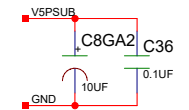
G5



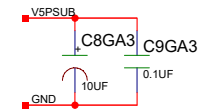
G6



GA1

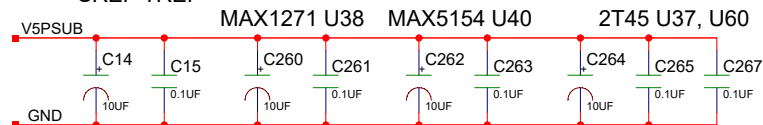


GA2

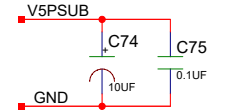


GA3

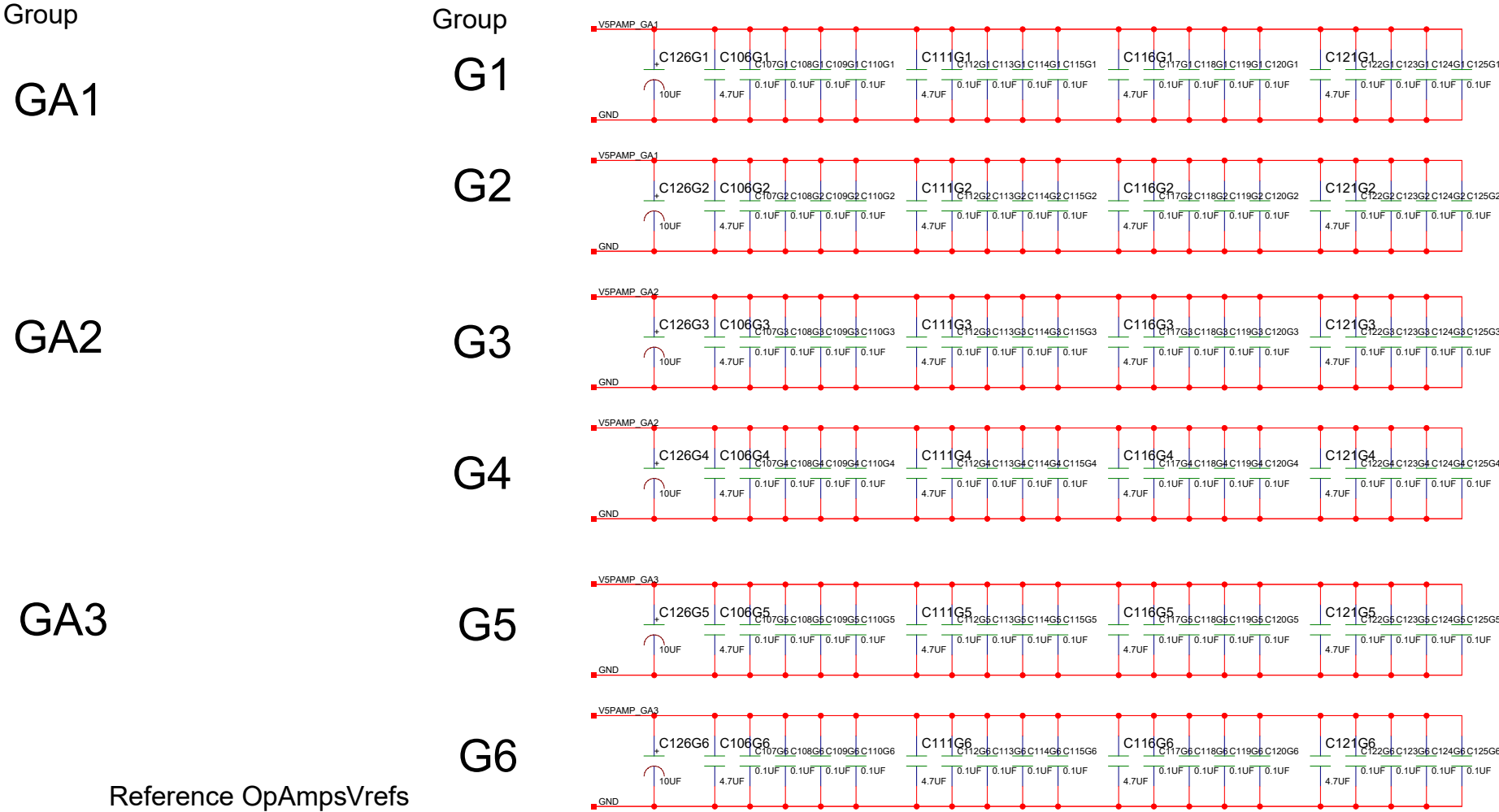
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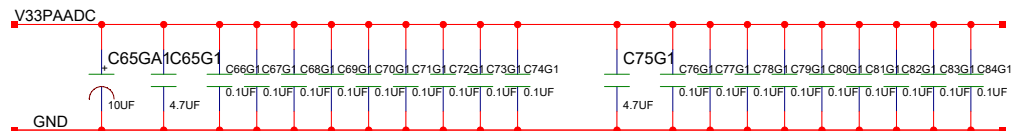
Translator U12



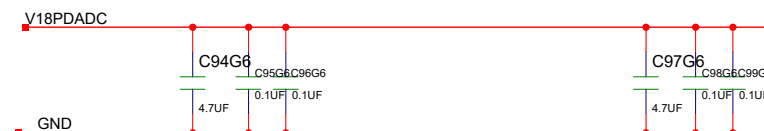
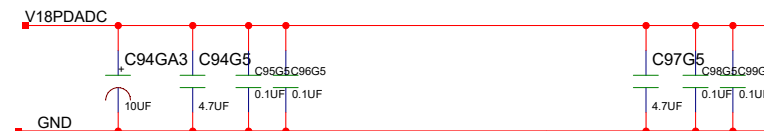
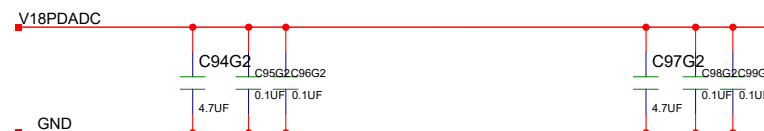
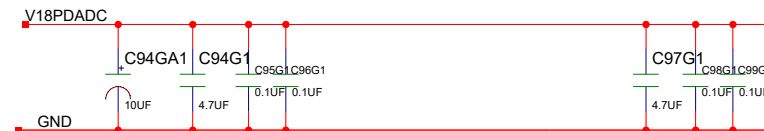
Differential OpAmps



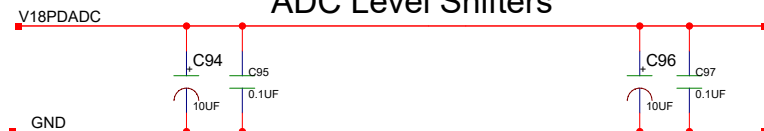
"V33PAADC"



"V18PDADC"



"ADC Level Shifters"

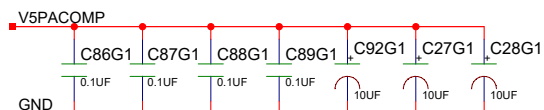


Group

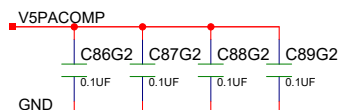
"V5PACOMP"

"V3PDCOMP"

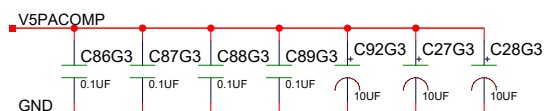
G1



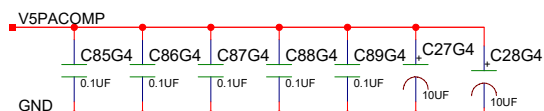
G2



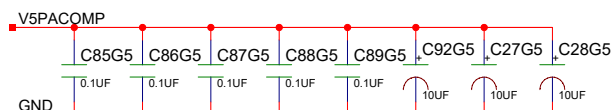
G3



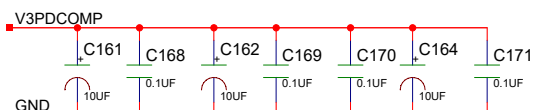
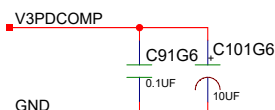
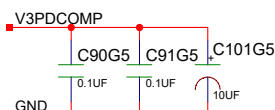
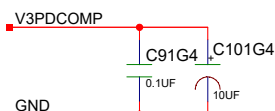
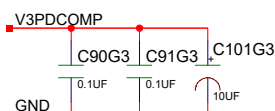
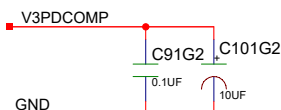
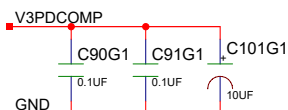
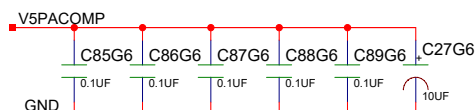
G4



G5

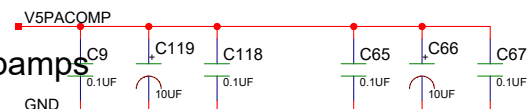


G6

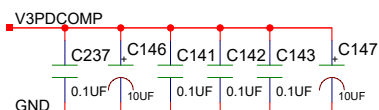
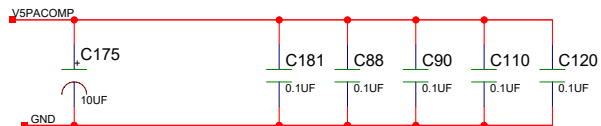


LVDS Rx/Tx

CREF and CMPDAC opamps



DAC



Clock driver



