VHDL Project

The goal of the project is to develop, implement and simulate a specific unit described below.

1. Development

The schematic implementation of the project is shown below.

![Schematic Diagram]

DFF35 and DFF4 are 35-bit and 4-bit D-type Flip-Flops respectively, operating on a rising edge of the CLOCKA signal. The function of the SELECTOR unit is the following:

- if the incoming 35-bit pattern contains all “1” (i.e. ‘111111111111111111111111111111111’), the 4-bit output is ‘1000’;
- if the incoming 35-bit pattern contains only one “0” (i.e. ‘111111111011111111111111111111111’ or any other of 34 possible cases), the 4-bit output is ‘0100’;
- if the incoming 35-bit pattern contains two “0” (i.e. ‘111111111011111111111111111111111’ or any other of 594 possible cases), the 4-bit output is ‘0010’;
- if the incoming 35-bit pattern contains three “0” (i.e. ‘111111111011111111111111111111111’ or any other of ???? possible cases), the 4-bit output is ‘0001’;
- if the incoming 35-bit pattern contains any other combination, the 4-bit output is ‘0000’.

2. Implementation

The top level design is a schematic (shown above). The three blocks DFF35, DFF4 and SELECTOR should be implemented in VHDL. The target device would be Xilinx XC2V250-5CS144 FPGA. The development system would be Xilinx ISE 6.03 or higher. The only timing constraint for this project would be the CLOCKA; try 15 ns as a clock period and decrease it if possible. Run the synthesis and implementation processes in ISE; their optimization strategies should be targeted to highest speed rather than area.

3. Simulation

Design a test bench file (also in VHDL) to be able to simulate various input patterns and add it to the project. Run the behavior and post place and route simulation using the ModelSim tools (coupled with the ISE) and make sure the results are as expected.